A 150V Monolithic Synchronous Gate Driver with Built-In ZVS Detection for Half-Bridge Converters

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***Abstract*— This paper presents a fully-integrated high-voltage (HV) synchronous gate driver for driving power switches in zero-voltage switching (ZVS) converters. The proposed gate driver monitors the drain-source voltage of both high-side and low-side power FETs and determines proper dead time to turn on the FETs under ZVS conditions. Compared with traditional off-chip ZVS detection scheme which typically requires an additional transformer winding, the proposed design incorporates ZVS detector into the monolithic gate driver to minimize the volume of magnetics and other external components, and reduce the detection delay from more than 60ns to 15ns. Implemented in a 0.7μm HV BCD process, the proposed 150V synchronous gate driver enables 2MHz ZVS operations in a 60W two-phase half-bridge converter with eGaN power FETs and offers at least 840mW saving in the full-load conditions compared with the traditional off-chip ZVS detection scheme.**

I. INTRODUCTION

Synchronous DC-DC converters with 10s-to-150V input and high switching frequency (100s of kHz) demonstrate wide applications in telecom systems and automotive electronics. Further increasing the switching frequency is highly desired for reducing the system cost and the converter volume. This however requires zero-voltage switching (ZVS) techniques to minimize the power loss related to the turn-on and/or turn-off of power FETs. A challenging control scheme in ZVS converters is to identify proper dead time to turn on the power FET right after zero-voltage switching is complete. If the dead time is set too short, the power FET is turned on with large drain-source voltage and thus large turn-on loss; if the dead time is set too long, reverse conduction of the power switch would increase the VI loss across the FET [1] – [3].

A zero-voltage switching (or valley switching) detection scheme, as shown in Fig. 1, has been reported in [4] – [7]. An auxiliary winding is used to convert the drain-source voltage of high-side FET (V_{dsH}) into a low-voltage signal (V_L). After the zero-cross point of V_L, the high-side FET is turned on with a delay equal to a quarter of resonant period (1/4 * T_R) such that, in ideal case, V_{dsH} equals zero during turn-on. Major limitations of this ZVS detection and dead time control scheme are as follows. (1) This structure requires an off-chip auxiliary winding that complicates the magnetic design; (2) the detected signal is first generated in the low-voltage domain and has to be up-shifted to V_{BT} domain with a high common-mode voltage, resulting in extra delay time; and (3) the resonant period is only an empirical value, which varies with voltage and temperature in practical environment, resulting in an inaccurate control of the dead time of power FETs.

This paper proposes an on-chip synchronous gate driver that integrates the function of ZVS detection and dynamic dead time control to solve the traditional limitations. By comparing the drain-source voltage directly with an on-chip sensor in the proposed design, high-side and low-side power FETs can be turned on after ZVS operation finishes with minimal delays. Section II introduces the system architecture of the proposed synchronous ZVS gate driver, and presents detailed circuit designs and operation analysis of the new on-chip ZVS detector. The operation principle of a quasi-square-wave two-phase ZVS buck converter used for the gate driver verification is presented in Section III and the experimental results are provided in Section IV. Conclusions are finally given in Section V.

II. PROPOSED ON-CHIP SYNCHRONOUS GATE DRIVER AND CIRCUIT IMPLEMENTATIONS

A. Architecture and Operation Principles of the Proposed Gate Driver

Fig. 2 shows the structure and critical waveforms of the proposed on-chip gate driver. The high-side ZVS detection block (HZVSD) monitors and compares the drain voltage (V_{IN}) and the bootstrap voltage of high-side FET M_H to determine proper dead time of M_H. Similarly, the low-side ZVS detection block (LZVSD) monitors and compares the drain voltage of low-side FET M_L and low-side supply (V_{DD}) to determine proper dead time of M_L.

Assuming ZVS operation of M_H is realized by the negative current of inductor current I_L. At t_0, M_L is first turned off and the drain-source voltage (V_{dsH}) of M_H drops from V_{IN} towards 0 accordingly. With V_{SW} rising from 0 towards V_{IN}, V_{BT} rises from V_{DD} towards V_{IN}+V_{DD} and V_{BT} is always higher than V_{SW} by the value of V_{DD} (i.e. 5V). ZVS operation of M_H is achieved at t_1 when V_{dsH} drops to 0 and V_{BT} rises to V_{IN}+V_{DD} (higher than V_{IN}), which sets the output of the comparator and triggers a negative one-shot pulse (V_{CH}) to set the driver of M_H. The operation of LZVSD is similar to that of HZVSD. Both HZVSD and LZVSD are fully integrated in the gate driver. Also, the detection signals of HZVSD and LZVSD are generated in high-side and low-side, respectively, such that no additional delay caused by the level shifting of the detection signal is involved in the proposed dead time control.

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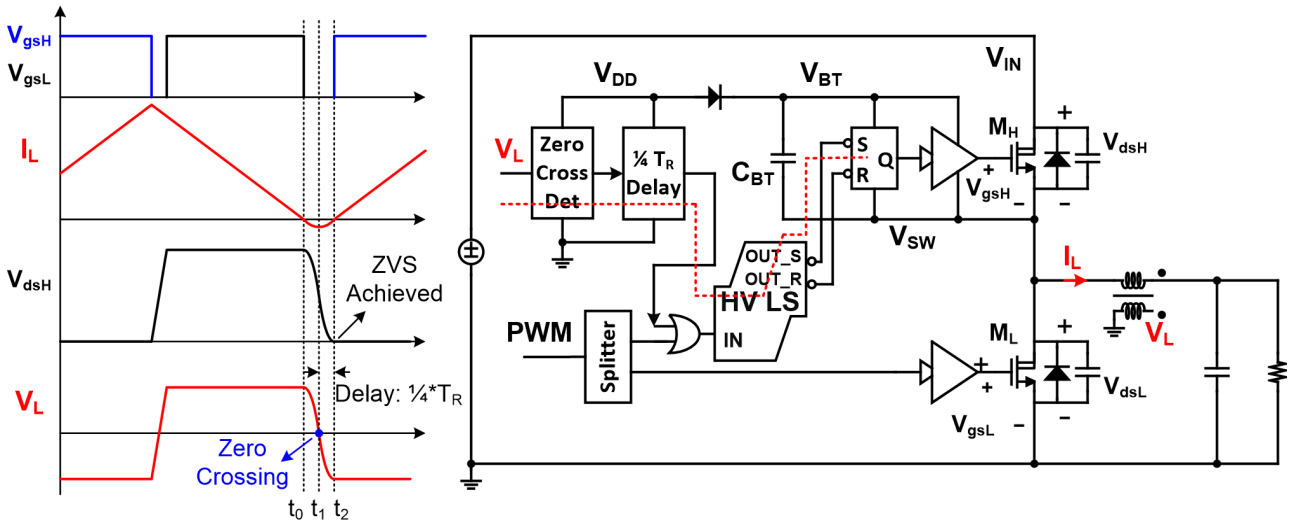


Fig.1: Schematic and waveforms of traditional off-chip ZVS detection.

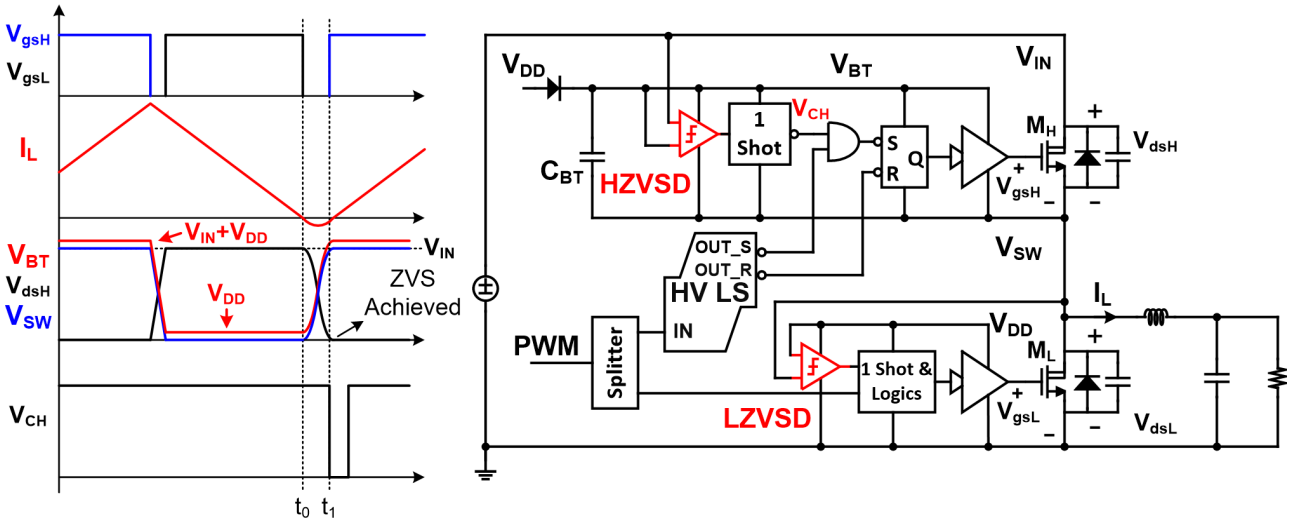


Fig.2: Schematic and waveforms of the proposed gate driver with on-chip ZVS detector.

B. Transistor Implementation of ZVS Detectors

Fig. 3 shows the schematic and operation waveforms of both ZVS detectors. In HZVSD, HV LDMOS M_{D1} is normally off before V_{BT} rises to V_{IN}, which pulls both V_1 and V_2 to V_{BT} such that M_{N1} is on, M_{P2} is off and V_3 equals V_{SW}. When V_{SW} = V_{IN} at t_0 (ZVS of M_H is achieved), the body diode of M_{D1} starts to conduct and pulls V_1 down to V_{SW}+0.7V (a diode voltage drop), which is barely lower than the threshold voltage of M_{N1}. The body diode current flows through M_{P1} and get mirrored to M_{P2} by a ratio of 1:1. By using a minimum size of M_{N1} and much larger size of M_{P2}, V_3 is pulled up to V_{BT} at t_0 to trigger the one-shot signal V_{CH}. After high-side FET M_H is turned off at t_2, both V_{SW} and V_{BT} start to drop and the body diode of M_{D1} cuts off. This pulls V_1 and V_2 up to V_{BT} and V_3 down to V_{SW} again. The detection circuit is reset at t_2 and ready to detect ZVS operation in the next switching cycle. The resistor R_1 is designed to be 100kΩ to limit the total current in both M_{P1} and M_{P2} lower than 30μA (V_{DD} = 5V) during $t_0 - t_2$ with less than 10ns delay of HZVSD. Schematic and operation of LZVSD is also illustrated in Fig. 3.

The operation of LZVSD is similar to that of HZVSD and is thus not described repetitively here. The proposed gate driver with on-chip ZVS detector and dead time controller is realized in a 0.7μm HV BCD technology.

III. A Quasi-Square-Wave Two-Phase ZVS Buck Converter

A two-phase quasi-square-wave (QSW) ZVS buck converter is used to test the function and performance of the proposed gate driver. As shown in Fig. 4, the auxiliary branch provides transient current ripple (I_A) to achieve ZVS operation of M_{HA} and M_{HB}. ZVS operation of M_{LA} and M_{LB} is achieved by the currents of main inductors L_{MA} & L_{MB}, respectively. The critical waveforms of the two-phase QSW ZVS buck converter are demonstrated in Fig. 4 and detailed descriptions of operation principles can be found in [8].

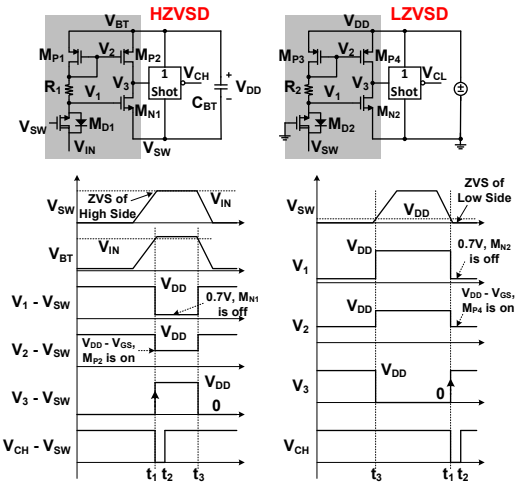


Fig.3: Transistor implementation of ZVS detectors.

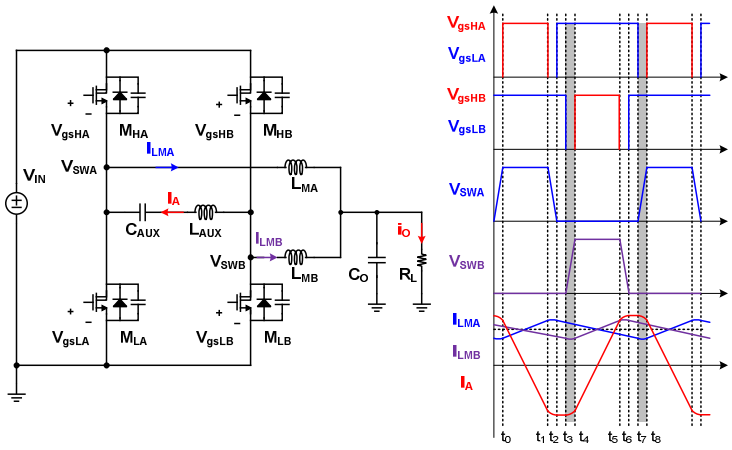
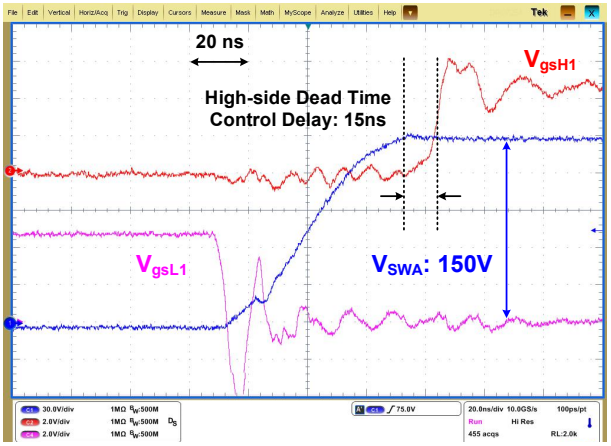


Fig. 4: Schematic and waveform of two-phase QSW ZVS converter.

(a)



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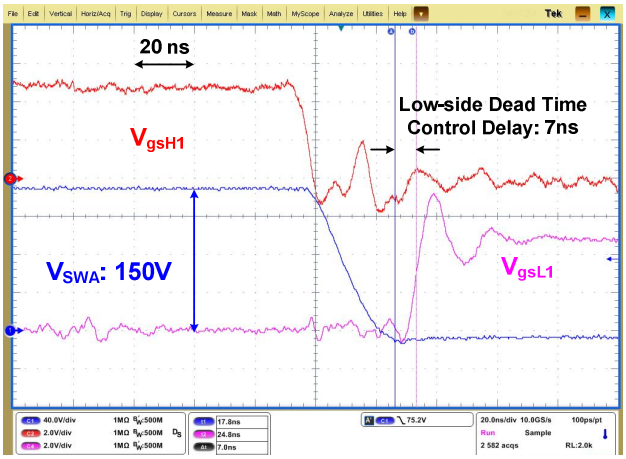

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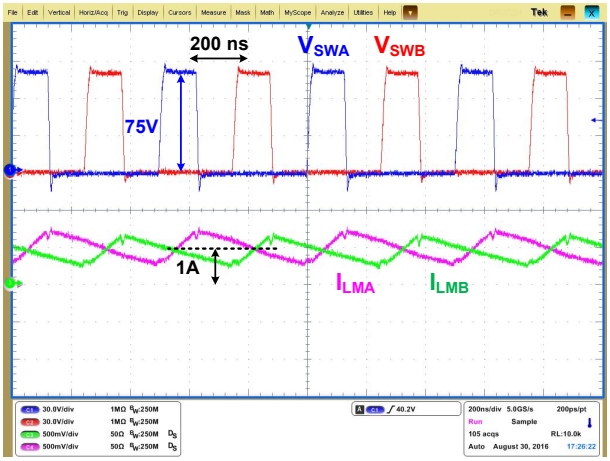

(d)

Fig. 5: (a) Photo of the testing board; (b) high-side dead time control delay; (c) low-side dead time control delay; and (d) steady-state waveforms of the converter.

TABLE I: Performance Comparisons Of Different HV Power Converters

	LTC7103 [9]	HFC0100 [10]	LMG5200 [11]	**This Work**
Max V_{IN} (V)	105	265 AC	75	**150**
Max P_{OUT} (W)	11.5	36	50	**60**
F_{SW} (kHz)	200 - 2000	140	600	**2000**
Power Switch	MOSFET	MOSFET	GaN FET	**GaN FET**
Switching Method	Hard switching	ZVS	Hard switching	**ZVS**
ZVS Detection	Not available	Traditional method using off-chip devices	Not available	**Fully integrated**
Dead Time Control Delay	Not available	100ns	Not available	**15ns (high-side); 7ns (low-side)**
Peak Power Efficiency	87% (72V, 300kHz)	90.5% (220VAC)	91% (48V); 89% (75V)	**92.8% (75V); 90.3% (150V)**

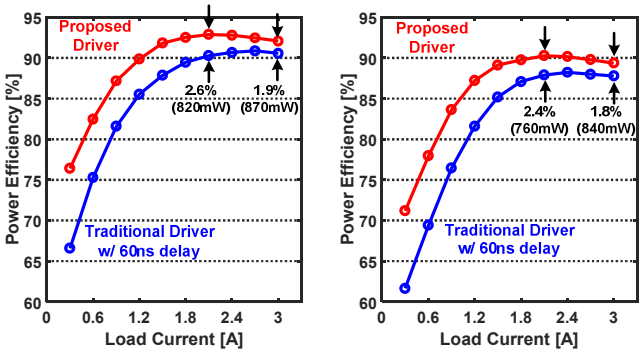

Fig.6: Efficiency comparison between the two-phase QSW ZVS buck converter using the proposed gate driver and the same converter using traditional gate driver with 60ns dead time control delay under (a) 75V and (b) 150V.

IV. Experimental Verification

The proposed gate driver was tested with the two-phase QSW ZVS buck converter as shown in Fig. 5(a). With the input voltage varying from 75V to 150V, the converter can deliver a maximum 60W (3A) to the output and run at 2MHz. Four 200V eGaN FETs (EPC 2010C) are used as power switches. Figs. 5(b) and 5(c) show the transient waveforms of gate drive signals and the switch-node voltage at 150V input. High-side dead time control delay, measured from switch-node voltage rising to V_{IN} to high-side switch being turned on, is 15ns. Low-side dead time control delay, measured from switch-node voltage falling to 0 to low-side switch being turned on, is around 7ns. Fig. 5(d) shows the steady-state waveforms of the converter running at 2MHz with 75V input and 2A load current.

Fig. 6 compares the power efficiency of the two-phase QSW ZVS buck converter using the proposed dead time control scheme and the same converter using gate driver with 60ns dead time control delay (typical value for the traditional off-chip solution). The power efficiency improvement is around 2.6% and 2.4% for 75V and 150V input voltages, saving 820mW and 760mW, respectively. Table 1 compares the performance of the two-phase QSW ZVS buck converter using the proposed gate driver with that of other state of the art from industry [9] – [11]. By comparison, the proposed fully on-chip gate driver achieves the shortest dead time control delay for ZVS operation. This helps the converter achieve high power efficiency with the highest switching frequency (in the MHz range) among candidates of similar voltage level.

V. Conclusions

A 150V synchronous ZVS gate driver is proposed and verified in this paper. By comparing the drain- and source-voltage of power FETs, the on-chip ZVS detector replaces the auxiliary inductor winding in the traditional discrete valley switching technique. This not only saves the BOM cost but also reduces the ZVS dead time control delay from 60-100ns in the conventional ZVS detector to around 15ns. With more accurate dead time control, the proposed ZVS gate driver enables 2MHz ZVS operations in a 60W two-phase half-bridge converter with eGaN power FETs and offers at least 840mW saving in the full-load conditions compared with the traditional off-chip ZVS detection.

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