Power Plateau and Anti-Power Phenomenon of Dual Active Bridge Converter with Phase-Shift Modulation

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***Abstract*—In this paper, an improved power flow model for dual active bridge (DAB) converters with phase-shift modulation is introduced. Based on the analysis and the accordingly derived equations, a power plateau phenomenon, in which the phase shift loses its power-regulating capability, is investigated. Moreover, it is found that this power plateau phenomenon leads to an inversed power flow characteristic in some specific regions compared to the models reported in previous literature. The characteristics of the power plateau and its occurring conditions are derived and analyzed in depth. The calculations, simulations and analyses have been verified by experiments.**

Keywords—dual active bridge; phase shift modulation; power flow model; power flow characteristics

I. INTRODUCTION

The utility grid, once passive and static with a limited number of distributed generators, is now more active and dynamic because of integration of distribution energy resources [1]-[2]. Therefore, solutions such as energy storage systems are required to improve grid reliability and stability [3]. Bidirectional dc-dc converters, which can interface energy storage systems to power conversion systems, have gained increasing attention [4]-[7]. Due to its small number of components, symmetrical structure, isolation capability and soft switching properties, the Dual Active Bridge (DAB) converter has become a popular topology for bidirectional dc-dc power conversion [7].

Several analyses have been implemented on the power flow of DAB converters with a Single Phase-Shift Modulation (SPSM) [8]-[12]. In [8], the power flow equation for a single-phase DAB was derived without considering any losses nor dead time between switches in the same leg. In [9], the short-time-scale transient processes in DAB converters with SPSM were discussed. However, no improvements in the power flow equation were made. In [10], an improved power flow equation was derived considering the dead-time effect and power semiconductor voltage drops, but the equation is not suitable for DAB converters using power MOSFETs; moreover the analyzed cases are limited. In [11], the power flow equation was derived considering MOSFET's ON resistance, and parasitic resistances of the inductor, transformer and PCB traces; however, the dead time effect was somehow neglected. In [12], the power flow equation was derived considering dead times. With those equations, some power flow characteristics were given, including the power plateau phenomenon which will be further investigated in this paper. However, the model in [12] does not consider any losses.

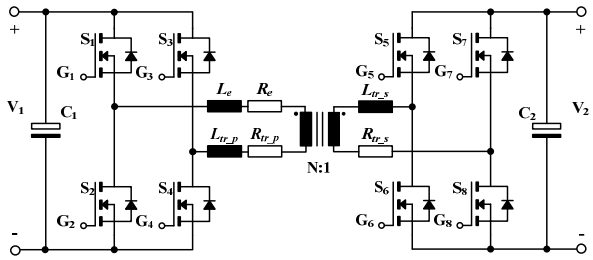

Fig. 1. Topology of a single-phase DAB converter.

In this paper, an improved power flow model was derived considering both parasitic resistances and dead time effects. Based on the obtained equations, a power plateau phenomenon is investigated in depth. It is found that Due to the power plateau, the power flow characteristic of the DAB is inversed compared to the previous studies at some specific operation points. Therefore, a comprehensive modeling, as well as its corresponding analysis, is essential for design and control of DAB converters. All calculations and analyses match the simulations well. Furthermore, experimental results from a laboratory prototype verify the analysis, characteristics and influences of the power plateau.

II. IMPROVED DAB MODELING AND ANALYSIS

Fig. 1 shows a single-phase DAB converter, where the magnetizing inductance is neglected. L_e and R_e represent the inductance and winding resistance of the external inductor; L_{tr_p}, R_{tr_p} and L_{tr_s}, R_{tr_s} represent the leakage inductance and the winding resistance of the transformer primary and secondary, respectively; MOSFETs are treated as a constant resistance when they are triggered ON by driving signals, and as a constant voltage drop when conducting reversely without driving signals; G_1~G_8 represent the driving signals; V_1 and V_2 are DC voltage sources; V_{dH} and R_{onH} are the forward voltage of body-diodes and the ON resistance of MOSFETs in the bridge connected to V_1; V_{dL} and R_{onL} are those of MOSFETs in the bridge connected to V_2; T_d is the dead time; f_s is the switching frequency. Input power P_{in} is defined as power sourcing from V_1, and output power P_o is power sinking into V_2.

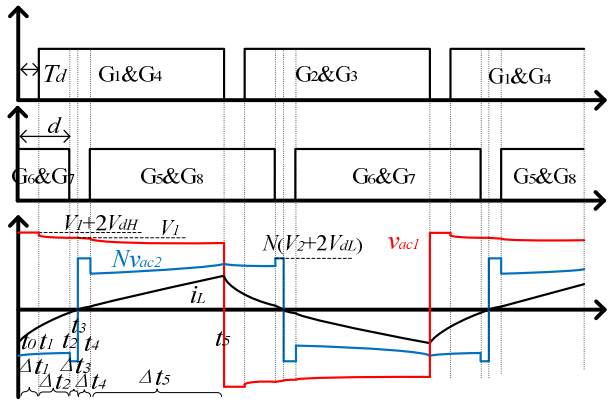

Fig. 2. Typical waveforms of the analyzed case.

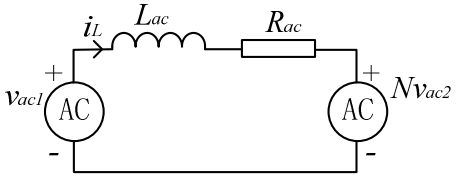

Fig. 3. Equivalent circuit of the DAB converter.

Here a special operation condition which leads to the power plateau phenomenon is analyzed. The typical waveforms of the DAB converter working in this case are given in Fig. 2, where assume $V_1>NV_2$ and commutation processes are neglected. The inductor current changes direction during the dead time of the active bridge connected to V_2. The unified phase shift d is defined as:

$$d=\frac{\beta}{\pi} \tag{1}$$

where β is the phase shift angle.

The equivalent circuit of the DAB converter illustrated in Fig. 1. can be derived as shown in Fig. 3.

L_{ac} and R_{ac} are expressed:

$$L_{ac}=L_{tr\_p}+N^2L_{tr\_s}+L_e \tag{2}$$

$$R_{ac}=R_{tr\_p}+N^2R_{tr\_s}+R_e \tag{3}$$

Based on Fig. 2, v_{ac1}, Nv_{ac2} and i_L can then be expressed as follows.

$$V_{ac1}(t)=\begin{cases}V_1+2V_{dH},t\in[t_0,t_1]\\V_1-2R_{onH}\cdot i_L(t),t\in(t_1,t_2]\\V_1-2R_{onH}\cdot i_L(t),t\in(t_2,t_3]\\V_1-2R_{onH}\cdot i_L(t),t\in(t_3,t_4]\\V_1-2R_{onH}\cdot i_L(t),t\in[t_4,t_5]\end{cases} \tag{4}$$

$$Nv_{ac2}=\begin{cases}-N\left(V_2-2R_{onL}N\cdot i_L(t)\right),t\in[t_0,t_1]\\-N\left(V_2-2R_{onL}N\cdot i_L(t)\right),t\in(t_1,t_2]\\-N\left(V_2+2V_{dL}\right),t\in(t_2,t_3]\\N\left(V_2+2V_{dL}\right),t\in(t_3,t_4]\\N\left(V_2+2R_{onL}N\cdot i_L(t)\right),t\in[t_4,t_5]\end{cases} \tag{5}$$

$$i_L(t)=\begin{cases}i_L(t_0)\cdot e^{-J_1(t-t_0)}+M_1\left[1-e^{-J_1(t-t_0)}\right],t\in[t_0,t_1]\\i_L(t_1)\cdot e^{-J_2(t-t_1)}+M_2\left[1-e^{-J_2(t-t_1)}\right],t\in(t_1,t_2]\\i_L(t_2)\cdot e^{-J_3(t-t_3)}+M_3\left[1-e^{-J_3(t-t_2)}\right],t\in(t_2,t_3]\\i_L(t_3)\cdot e^{-J_4(t-t_3)}+M_4\left[1-e^{-J_4(t-t_3)}\right],t\in(t_3,t_4]\\i_L(t_4)\cdot e^{-J_5(t-t_4)}+M_5\left[1-e^{-J_5(t-t_4)}\right],t\in[t_4,t_5]\end{cases} \tag{6}$$

where J_1~J_5 and M_1~M_5 are given in Table. 1.

Moreover, from Fig. 2, the following equations can be obtained.

$$\begin{cases}\Delta t_1=T_d\\\Delta t_2=\dfrac{d}{2f_s}-T_d\\t_4-t_2=T_d\\i_L(t_3)=0\\t_5-t_0=\dfrac{1}{2f_s}\end{cases} \tag{7}$$

At the end of half cycle:

$$i_L(t_5)=-i_L(t_0) \tag{8}$$

Based on (8), the following equation can be obtained:

$$\Delta t_4=\left(-\frac{1}{J_3}\right)\cdot\ln\left(\frac{\begin{pmatrix}M_1\left(1-e^{J_1\Delta t_1}\right)\\+M_5\left(1-e^{J_5\Delta t_5}\right)\\+e^{J_1\Delta t_1}\left(M_2+(M_3-M_2)e^{J_2\Delta t_2}\right)\end{pmatrix}}{M_4+M_3e^{J_2\Delta t_2+J_1\Delta t_1+J_5\Delta t_5+J_3T_d}}\right) \tag{9}$$

TABLE 1 EXPRESSIONS FOR J_1~J_5 AND M_1~M_5

J_1	$\dfrac{R_{ac}+2N^2R_{onL}}{L_{ac}}$	M_1	$\dfrac{V_1+2V_{dH}+NV_2}{R_{ac}+2N^2R_{onL}}$
J_2	$\dfrac{R_{ac}+2R_{onH}+2N^2R_{onL}}{L_{ac}}$	M_2	$\dfrac{V_1+NV_2}{R_{ac}+2R_{onH}+2N^2R_{onL}}$
J_3	$\dfrac{R_{ac}+2R_{onH}}{L_{ac}}$	M_3	$\dfrac{V_1+N(V_2+2V_{dL})}{R_{ac}+2R_{onH}}$
J_4	$\dfrac{R_{ac}+2R_{onH}}{L_{ac}}$	M_4	$\dfrac{V_1-N(V_2+2V_{dL})}{R_{ac}+2R_{onH}}$
J_5	$\dfrac{R_{ac}+2R_{onH}+2N^2R_{onL}}{L_{ac}}$	M_5	$\dfrac{V_1-NV_2}{R_{ac}+2R_{onH}+2N^2R_{onL}}$

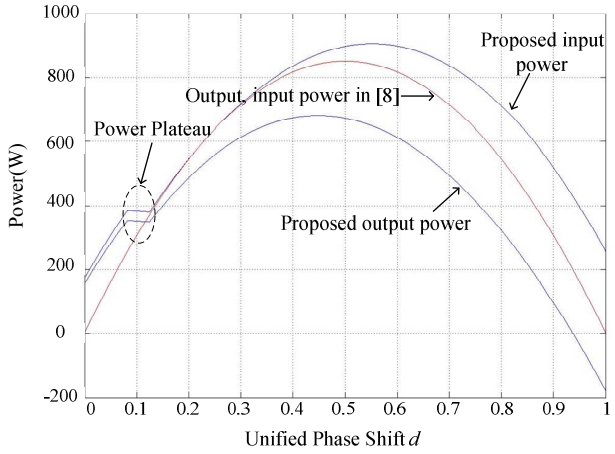

Fig.4. Calculated power flow characteristics.

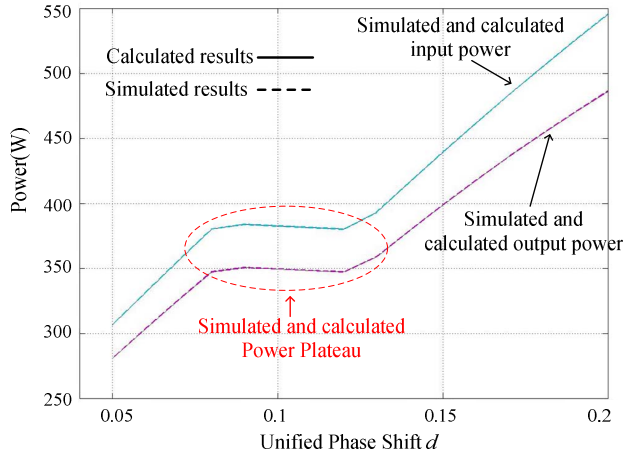

Fig. 5. Calculated and simulated power flow characteristics.

With (9), (7) and (4)~(6), P_{in} and P_o can be calculated as:

$$P_{in} = 2V_1 f_s \left(Int_1 + Int_2 + Int_3 + Int_4 + Int_5\right) \quad (10)$$

$$P_o = 2V_2 \cdot N f_s \left(-Int_1 - Int_2 - Int_3 + Int_4 + Int_5\right) \quad (11)$$

where Int_i ($1 \le i \le 5$) are the averaged i_L during interval Δt_i, whose expressions are given as follows:

$$\begin{cases} Int_1 = M_1\Delta t_1 + \left[i_L(t_0) - M_1\right]\left(-\dfrac{1}{J_1}\right)\left(e^{-J_1\Delta t_1} - 1\right) \\ Int_2 = M_2\Delta t_2 + \left[i_L(t_1) - M_2\right]\left(-\dfrac{1}{J_2}\right)\left(e^{-J_2\Delta t_2} - 1\right) \\ Int_3 = M_3\Delta t_3 + \left[i_L(t_2) - M_3\right]\left(-\dfrac{1}{J_3}\right)\left(e^{-J_3\Delta t_3} - 1\right) \\ Int_4 = M_4\Delta t_4 + \left[i_L(t_3) - M_4\right]\left(-\dfrac{1}{J_4}\right)\left(e^{-J_4\Delta t_4} - 1\right) \\ Int_5 = M_5\Delta t_5 + \left[i_L(t_4) - M_5\right]\left(-\dfrac{1}{J_5}\right)\left(e^{-J_5\Delta t_5} - 1\right) \end{cases} \quad (12)$$

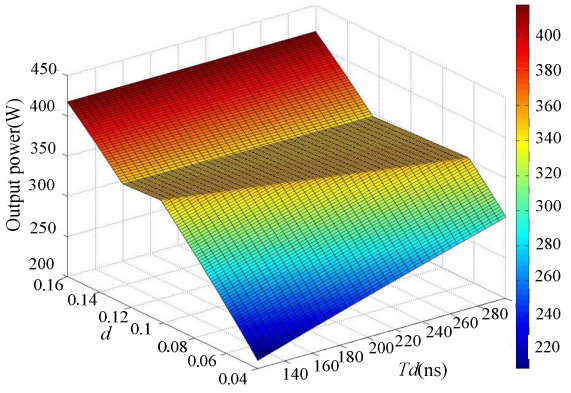

Fig. 6. Calculated output power as a function of d & T_d

Therefore, the calculated power flow here in (10) and (11) for $V_1 > NV_2$, and those proposed in [8] are plotted in Fig. 4 (the adopted parameters are given in Table 2). As shown, when d is 0.08~0.13, the input and output power do not keep increasing, and even decreases, which is against the results in [8]-[11]. The so-called power plateau phenomenon appears. The simulated and calculated input and output power are presented in Fig. 5 and they match very well, thus the proposed calculations are verified.

TABLE. 2 PARAMETERS OF THE PROTOTYPE

V_1	V_2	f_s	T_d	V_{dH}
200V	30V	100kHz	210ns	4.8V
V_{dL}	R_{onH}	R_{onL}	R_e	L_e
0.9V	65mΩ	1.9mΩ	52mΩ	41.2uH
N	R_{tr_p}	R_{tr_s}	L_{tr_p}	L_{tr_s}
14/3	1.8Ω	80mΩ	2.5uH	112nH

III. CHARACTERISTICS OF POWER PLATEAU

Given $V_1 > NV_2$, the calculations are done to investigate which parameters may have impact on the plateau's length i.e. phase shift range and where the plateau occurs. The conclusion is that T_d affects the power plateau's length and location, depending on certain N, L_e, V_{dH}, V_{dL}, R_{onH}, and R_{onL} since N, L_e are mainly determined by the required power, and V_{dH}, V_{dL}, R_{onH}, R_{onL} are constant once MOSFETs are selected. The influences of V_2 are given in section IV. As shown in Fig. 6, with the dead time increasing, the length of the power plateau increases, and its starting points shift to a smaller phase shift angle; however, the ending points keep unchanged.

IV. EFFECTS OF POWER PLATEAU ON DAB OPERATION

During the power plateau, the power flow is unable to be regulated over certain phase shift ranges. Especially in high power applications, where the phase shift angle is usually limited to small values (below $\pi/4$) to suppress reactive power loss, the power plateau takes a large portion of the allowable phase shift angle range and thereby has a negative impact on the converter control.

Moreover, during the plateau, the DAB's power no longer increases (or decreases) with increasing (or decreasing) lagging

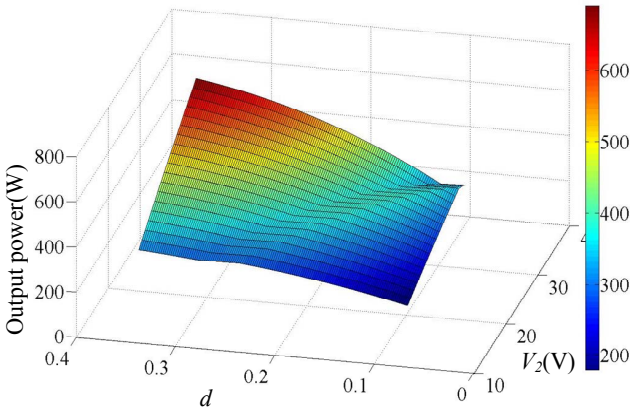

Fig. 7. Calculated output power as a function of d and V_2.

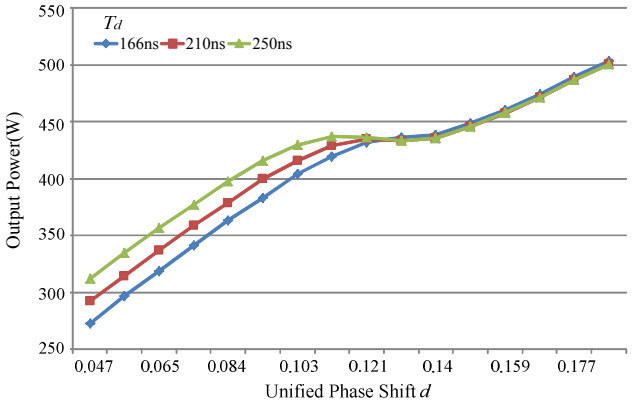

Fig. 9. Measured output power as a function of d & T_d

bridge DC voltage V_2, and it is named as anti-power phenomenon. Using the parameters listed in Table 2, the calculated output power as a function of d and V_2 is plotted in Fig. 7. As shown, at a specific phase shift angle, the output power will increase (or decrease) with decreasing (or increasing) V_2 over the specific V_2 range.

V. Experimental Results

In order to verify the theoretical analysis, a laboratory prototype with the same parameters given in Table 2 is constructed and tested. Fig. 9 plots the output power as a function of d at different T_d. A power plateau can be seen clearly at different T_d, therefore, the existence of power plateau and its associated analysis in section III are verified. Fig. 10 and Fig. 11 show the measured waveforms of the transformer port voltages, inductor current and driving signals of the MOSFETs in the V_2 active bridge with d=0.14 and T_d=210 ns. As shown, the inductor current changes its direction during the dead time so that this can verify the analysis given in Fig. 2. Fig. 12 shows that the power flow characteristic is inversed at the specific V_2 values. Due to the anti-power phenomenon, additional concerns must be taken in DAB power regulation, especially when on-line calculations [13]-[15] are used.

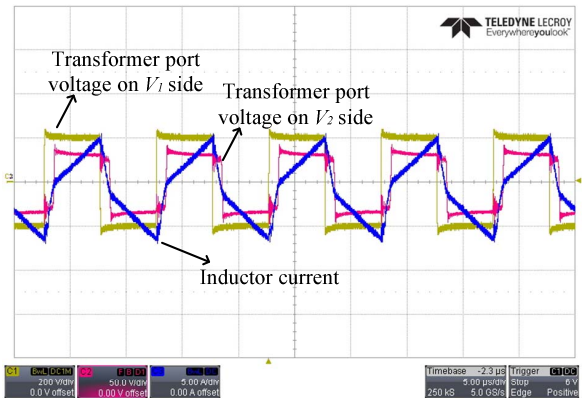

Fig. 10. Measured transformer voltages and inductor current at d=0.14 & T_d=210ns

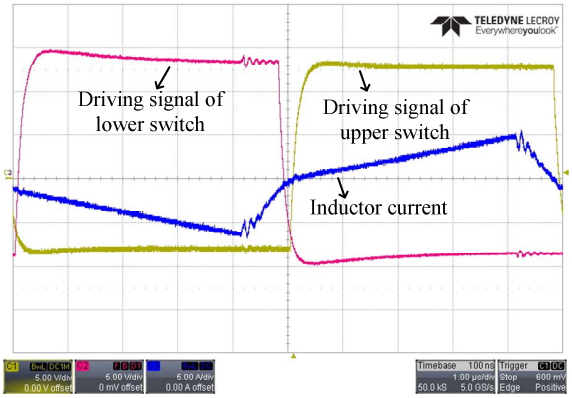

Fig. 11. Measured driving signals for MOSFETs in lagging bridge at d=0.14 and T_d=210 ns.

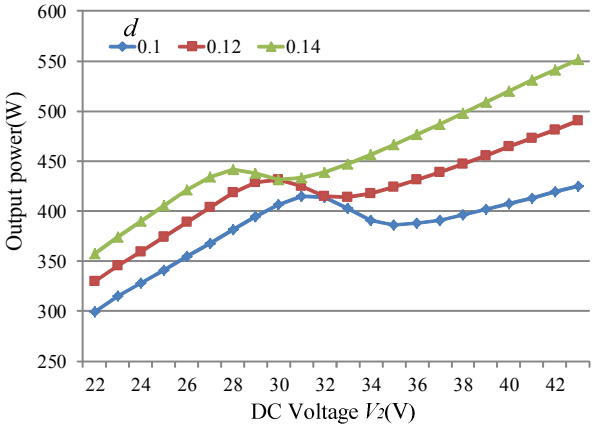

Fig. 12. Measured output power as a function of d & V_2

VI. Conclusions

In this paper, an improved power flow model for the single-phase DAB converter with phase shift control is derived, considering the conduction loss of MOSFETs and magnetic components and the dead time effects. A special operating condition in which inductor current changes direction during the dead time leads to the so-called power plateau in which the phase shift becomes unable to regulate the power flow. The

power plateau leads to different power flow characteristics compared to the results reported in previous investigations. Thereby, the characteristics of the power plateau are studied, and the impact due to dead time on the power plateau is addressed. All the theoretical analysis, calculations and simulations are verified by experiments. For the cases of $V_1<NV_2$ and for DAB converters with modulation schemes other than a single phase shift modulation, more investigations to study the DAB converter's power flow characteristics are needed in the future.

REFERENCES

[1] Q. C. Zhong, "Power electronics-enabled autonomous power systems: architecture and technical routes", IEEE Transactions on Industrial Electronics, vol. 64, no. 7, pp. 5907-5918, Jul. 2017.

[2] L. F. Costa, G. D. Carne, G. Butic chi, M. Liserre, "The smart transformer: a solid-state transformer tailored to provide ancillary services to the distribution grid", IEEE Power Electronics Magazine, vol. 4, no. 2, pp. 56-67, Jun. 2017.

[3] Y. Xu, C. Singh, "Power system reliability impact of energy storage integration with intelligent operation strategy", IEEE Transactions on Smart Grid, vol. 5, no. 2, pp. 1129-1137, Aug. 2013.

[4] K. Kruse, M. Elbo, Z. Zhang, "GaN-based high efficiency bidirectional DC-DC converter with 10MHz switching frequency", IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 273-278, Mar. 2017.

[5] B. Li, F. C. Lee, Q. Li, Z. Y. Liu, "Bi-directional on-board charger architecture and control for achieving ultra-high efficiency with wide battery voltage range", IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 3688-3694, Mar. 2017.

[6] R. M. Burkart, J. W. Kolar, "Comparative η-ρ-σ Pareto optimization of Si and SiC multilevel Dual-Active-Bridge topologies with wide input voltage range", IEEE Transactions on Power Electronics, vol. 32, no. 7, pp. 5258-5270, Jul. 2017.

[7] F. Xue, R. Y. Yu, A. Q. Huang, "A 98.3% efficient GaN isolated bidirectional DC-DC converter for DC Microgrid energy storage system applications", IEEE Transactions on Industrial Electronics, no. 99, Mar. 2017.

[8] R. W. A. A. De. Doncker, D. M. Divan, M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications", IEEE Transactions on Industrial Applications, vol. 27,no. 1, pp. 63-73, Jan/Feb. 1991.

[9] H. Bai, C. C. Mi, S. Gargies, "The short-time-scale transient processes in high-voltage and high-power isolated bidirectional DC-DC converters", IEEE Transactions on Power Electronics, vol. 23, no. 6, pp. 2648-2656, Nov. 2008.

[10] Y. H. Xie, J. Sun, J. S. Freudenberg, "Power flow characterization of a bidirectional galvanically isolated high-power DC/DC converter over a wide operating range", IEEE Transactions on Power Electronics, vol. 25, no. 1, pp. 54-66, Jan. 2010.

[11] F. Krismer, "Modeling and optimization of bidirectional dual active bridge DC-DC converter", Dissertation submitted to ETH Zurich for the Degree of Doctor of Sciences, 2010.

[12] B. Zhao, Q. Song, W. H. Liu, Y. D. Sun, "Dead time effect of the high frequency isolated bidirectional full bridge dc-dc converter: comprehensive theoretical analysis and experimental verification", IEEE Transactions on Power Electronics, vol. 29, No. 4, 2014: 1667-1680.

[13] H. Bai, Z. L. Nie, C. C. Mi, "A model-based dead-band compensation for the Dual-Active-Bridge isolated bidirectional DC-DC converter", IEEJ Transactions on Electrical and Electronic Engineering, pp. 517-524, Sep. 2011.

[14] D. Costinett, D. Maksimovic, R. Zane, "Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency", IEEE Transactions on Power Electronics, vol. 28, no. 8, pp. 3931-3940, Aug. 2013.

[15] R. Zgheib, K. Al-Haddad, "Neural network controller to manage the power flow of a hybrid source for electric vehicles", IEEE Vehicle Power and Propulsion Conference(VPPC), Oct. 2015.