

# A Series-AC-Link ISOP AC-AC Converter with Two Power Cells

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**Abstract**— Power converters used in shipboard power systems and industrial motor drives typically need to handle voltages and/or currents beyond the voltage/current ratings of the commercially available switches. A common solution is to employ multilevel converters. Most of the existing multilevel topologies are based on dc-link converters, and require a large number of switches and capacitors with high capacitances. This paper proposes a new three-phase ac-ac converter, the power cells of which are derived from a new class of highly reliable three-phase series-ac-link ac-ac converters. Using three-phase series-ac-link ac-ac converters as power cells minimizes the number of required components. A diode is placed between the two power cells to realize the series connection of power cells to accomplish the voltage sharing at the input side. Moreover, each power cell in the proposed configuration requires only a small film capacitor for transferring the power. This eliminates the need for electrolytic capacitors, which have high failure rates. The proposed ac-ac converter is evaluated in this paper, and the simulation results verify its promising features.

**Keywords**—ac-ac converter, high frequency link, high frequency transformer, high reliability, modular converter.

## I. INTRODUCTION

High power converters are typically needed in medium- or high-voltage systems. Having a high voltage source at the input side or a high current load at the output side of power converters, demands semiconductor switches with the capability of blocking high voltages and carrying high currents [1]. Since the technology of the semiconductor switches is still limited, multilevel converters [2], where a number of power cells (PC) are employed to share the voltage and current such that the commercialized switches can be used, are preferred for these applications. Several dc-link-based multilevel converters have been proposed in the literature, such as neutral point clamped (NPC) [3], modular multilevel converters (MMC), flying capacitor (FC) [4], and cascaded H-bridge (CHB) [5]. The power conversion in most ac-ac multilevel converters is performed through two stages, which are interconnected through a large dc electrolytic capacitor. These two power conversion stages are decoupled in terms of control [6, 7]. Since the dc-link capacitor maintains a high dc voltage with small ripples across the link, it has a high capacitance; hence, a large number of them are placed in series or parallel to realize the high capacitance and maintain the high dc voltage with small ripples. Use of these large and unreliable electrolytic capacitors is inevitable in high power multilevel converters, though the

power processed by each PC is a fraction of the total power. The main shortcoming of the multilevel converters is the short life-time and low reliability of the large electrolytic capacitors. Moreover, electrolytic capacitors are very sensitive to temperature, and can deteriorate the reliability of the system at higher temperatures [8, 9].

This paper introduces a new three-phase ac-ac converter topology with two PCs, which is derived from the series-ac-link ac-ac converter proposed in [10] and is depicted in Fig. 1. This converter uses small film capacitors instead of large electrolytic capacitors, even in high power applications. Moreover, a compact high frequency transformer added to the link can provide galvanic isolation. In case the converter proposed in [10] is intended to be used in an application with high input voltages, the voltage rating of the converter will surpass the voltage rating of the commercialized semiconductors. Use of multiple converters as PCs and input-series output-parallel (ISOP) connection of the terminals can address this issue in such applications, where the converter deals with high voltages at the input side and high currents at the output side. However, the input and output terminals of the converter proposed in [10] cannot be connected in series; therefore, this topology cannot be used as a PC for a high voltage system. In [11], an ISOP modular three-phase ac-ac converter topology is proposed, as shown in Fig. 2. The operation of each PC in this converter is inspired by the operation of the converter proposed in [10]. In this modular topology, having access to the neutral wire allows series connection of the PCs for voltage sharing at the input or output side. However, the number of switches is high in case the series-connection is desired. In this paper, a two-PC series-ac-link ac-ac converter with a smaller number of switches is proposed, which allows PCs to share the high voltages and high currents. Each PC is a single-stage power converter. Being single-stage, this converter does not require a decoupling capacitor, and a small capacitor can transfer the power from the input to the output. Owing to its high frequency capacitive link, there is no need for an electrolytic capacitor. This is a major advantage over the dc-link power converters in terms of the life-cycle, reliability, and power density. Another advantage of the proposed two-PC converter is that each PC offers galvanic isolation through a compact single-phase high frequency transformer, owing to the high frequency voltage variations of the capacitive link. This eliminates the need for a high voltage low frequency transformer, which is very bulky. The behavior of the proposed topology is similar to that of the capacitive



switches or diodes at the output-side switch-bridge (only one switch or diode on each leg) conduct to discharge the link capacitor through one of the output phase currents, and the input side switches/diodes provide paths for input currents and the link current. The input line-line voltages are built up by the link voltage during charging modes and the output line-line voltages are built up by the link voltage during the discharging modes. Two charging modes and two discharging modes allow all three input phases and all three output phases to be involved in charging or discharging the link capacitor.

Similarly, for the proposed ISOP ac-ac converter with two PCs, shown in Fig. 3, there are 5 modes in each switching cycle, including two charging modes, two discharging modes, and a zero operation mode. The voltage across the link capacitors and the unfiltered input and output line-line voltages of PCs are shown in Fig. 4. It should be noted that the link voltage shown in Fig. 4 is the summation of the voltages across the primary and secondary capacitors in each PC ( $V_{link1P}$  and  $V_{link1S}$  in PC1 and  $V_{link2P}$  and  $V_{link2S}$  in PC2); these capacitors on each side of transformers are equally charged and discharged at the same time. The unfiltered input line-line voltages across the phase terminals  $A_iB_i$ ,  $B_iC_i$ ,  $C_iA_i$ , where two PCs are connected through blue switches, is equal to the sum of unfiltered line-line voltages across the phase terminals  $A_{i1}B_{i1}$ ,  $B_{i1}C_{i1}$ ,  $C_{i1}A_{i1}$  and  $A_{i2}B_{i2}$ ,  $B_{i2}C_{i2}$ ,  $C_{i2}A_{i2}$ . Therefore, the voltage sharing at the input side is realized. Also, it is shown in Fig. 4 that the link current during discharging modes is equal to half of the output peak current, since the output terminals are connected in parallel. Parts (A) and (B) discuss the charging modes and the discharging modes of the proposed ISOP ac-ac converter, respectively.

#### A. Charging modes

As mentioned earlier, since the input side is intended to serve as series-connection for sharing the high input voltage between the two PCs, three switches are placed between the input source and each PC. Two charging modes are defined for the converter in each switching cycle. The link capacitors in both PCs are charged during modes 1 and 2 with the same current. For the case shown in Figs. 4, 5, and 6 it is assumed that the reference of line-line voltage across the input phase pair  $A_iB_i$  is positive and has the maximum value of input line-line voltages, and the reference of line-line voltage across output phase pair  $A_oB_o$  is negative and has the maximum value of output line-line voltages. It is clear that the phase pairs that have maximum input and output line-line voltages vary over time. In order to establish a path for the link current of PC1 to flow through the link capacitors of PC2, the middle diode ( $D_M$ ), is added to connect the two PCs.

During mode 1, since the input phase pair  $A_iB_i$  has the maximum positive value and phase  $A_i$  is carrying the highest current, switch  $S_{A1}$  is turned on and anti-parallel diode of  $S_1$  starts conducting to charge the link capacitors of PC1 ( $C_{1P}$  and  $C_{1S}$ ). Proper switch in the bidirectional switch should be turned on according to the direction of the phase current. The switches  $S_{B1}$  and  $S_{C1}$  are turned off so that the link current cannot flow back through the  $B_{i1}$  and  $C_{i1}$  phase terminals of PC1 and finds the path through  $D_M$  to the second PC and charges the link capacitors of PC2 ( $C_{2P}$  and  $C_{2S}$ ). To do so, the switches  $S_{B2}$  and  $S_{C2}$  are turned

on so that the phase  $B_i$  and  $C_i$  currents can flow back through the anti-parallel diodes of switches  $S_{52}$  and  $S_{62}$  in PC2. If the current of phase  $A_i$  is maximum and negative, switches  $S_{A2}$ ,  $S_{B1}$ , and  $S_{C1}$  will be turned on instead of  $S_{A1}$ ,  $S_{B2}$ , and  $S_{C2}$ . It should be noted that since the transformer is placed in the link of each PC, the same current flows through the secondary side capacitors. Also, during the first charging modes, depending on the output references, proper switches at the output side are turned on to let the output phase currents flow through the switches.

During mode 2 (Fig. 5 (b)), current of phase  $B_i$  charges the link capacitors in both PCs. Therefore, the switches  $S_{C1}$  and  $S_3$  are turned on so that the link current is equal to the current of phase  $B_i$ . Also, the switch  $S_{B1}$  is remained off so that the link current finds the path through the  $D_M$  to flow through the link capacitors of PC2. Switch  $S_{B2}$  in the second PC is turned on; thus, phase  $B_i$  current can flow back to the source through the anti-parallel diode of switch  $S_{52}$  in PC2. During modes 1 and 2, the unfiltered input line-line voltages of PC1 and PC2 are built up and their summation produces the unfiltered line-line voltages at terminals  $A_iB_iC_i$ . It should be noted that during mode 2, the switch commands of the output side bridge are the same as mode 1 such that the output phase current can flow through the output switches and a path is established for the link currents to flow.

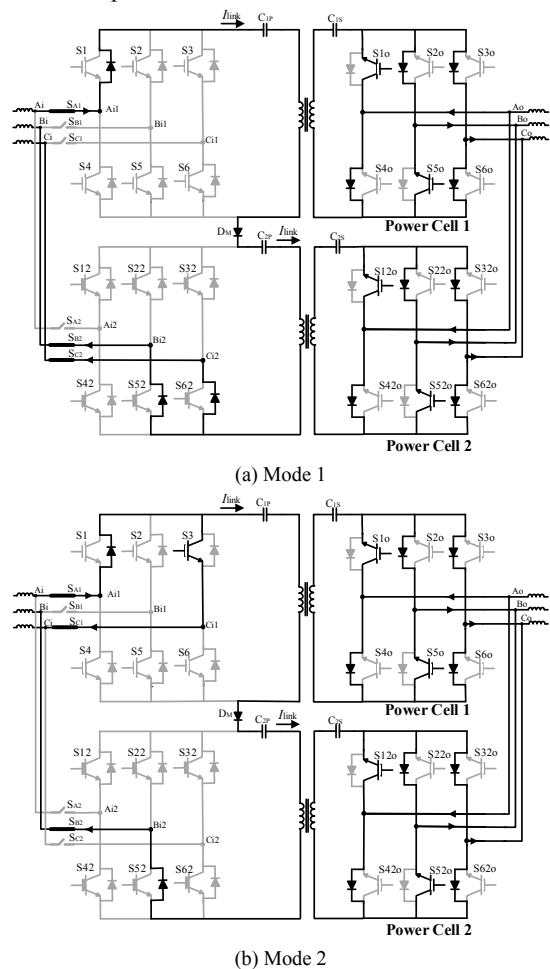


Fig. 5. The behavior of the proposed converter during modes 1 and 2.

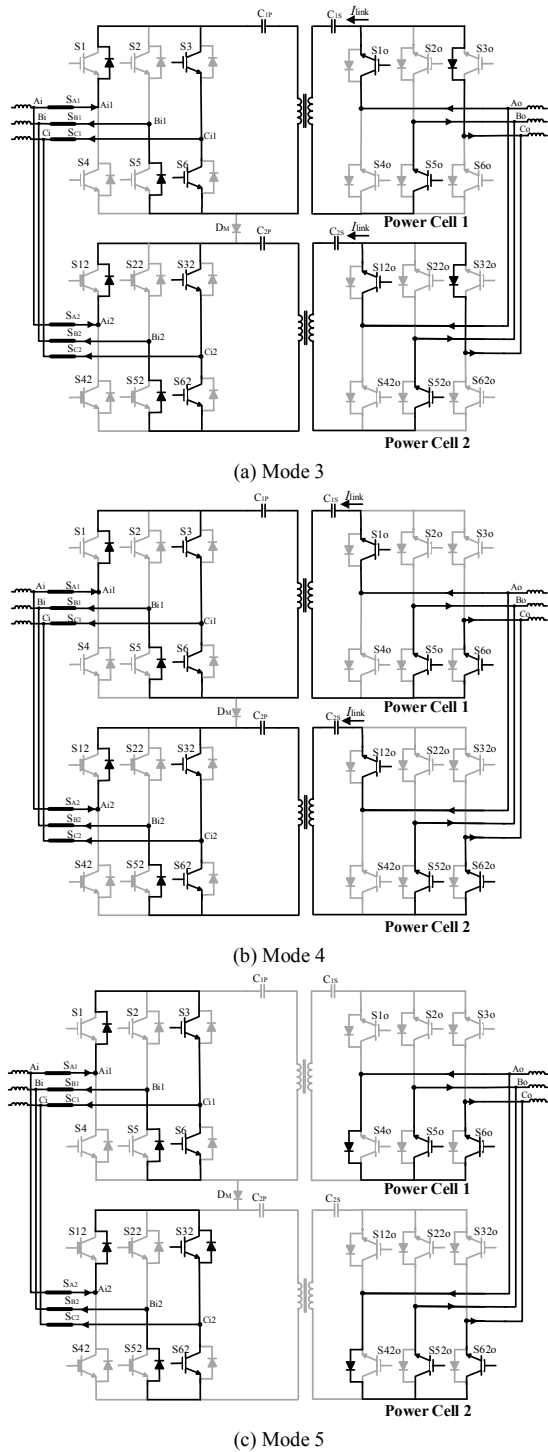


Fig. 6. The behavior of the proposed converter during modes 3, 4, and 5.

### B. Discharging and zero operation modes

There are two modes for discharging the link capacitors into the output. Since the output terminals of the PCs are connected in parallel, both PCs are discharged at the same time with half of the output current. In the first discharging mode, the second highest output phase current discharges the link capacitors ( $I_3 = -$

$|I_{B0}|/2$ ). To do so, the switches  $S_{10}$  and  $S_{50}$  of PC1 and  $S_{120}$  and  $S_{520}$  of PC2 are turned on. Since the link current in both PCs is negative, two switches at the input side need to be turned on to establish a path for the link current. These two switches are determined based on the input line-line voltage references. Therefore, the switch commands for both PCs are the same during discharging modes. However, the switches on the terminals of PC1 and PC2 are turned on to let the input currents flow through the input side switches of both PCs. Since both PCs are providing the path for the input currents to flow through the input switch bridges, the input current is divided between the two PCs. In order to move from mode 3 to mode 4, switch  $S_{60}$  and  $S_{620}$  in both PCs are turned on, so that the highest output phase current ( $I_4 = -|I_{A0}|/2$ ) starts discharging the link capacitors of both PCs.

Once the link capacitors of PC1 and PC2 are fully discharged, mode 5 starts. As discussed, mode 5 is added to the operation of the converter to realize a fixed switching frequency control. During this mode, the link capacitors of both PCs are open circuit, by turning off switches  $S_{10}$  and  $S_{120}$ . During this mode, the link voltage and current remain zero in both PCs until the end of the link cycle. During this mode, the input and output phase currents have the path for free-wheeling.

### III. DESIGN AND CONTROL OF THE PROPOSED CONVERTER

This section presents the method to calculate  $t_1-t_5$ , which are the durations of modes 1 to 5, respectively. It is assumed that the transferred power during modes 1 to 4, are denoted by  $P_1-P_4$ .  $V_1-V_4$  and  $I_1-I_4$ , are equal to the average values of the link voltage and current of a PC during modes 1 to 4, respectively. As shown in Fig. 2, in the ISOP configuration with two PCs, the input terminals of the PCs are connected in series and their output terminals are connected in parallel. Therefore, the input voltage references of each PC are half the input voltage references, while at the output side phase currents are divided by two. To find proper values of  $t_1-t_5$ , the reference values of  $V_1-V_4$  and  $I_1-I_4$  are used in the control algorithm. Assuming  $V_{p1}-V_{p3}$  are the voltages of the link capacitors in both PCs at the end of modes 1, 2, and 3, respectively,  $V_1-V_4$  can be as determined as follows:

$$V_1 = \frac{1}{2}(V_{p1})t_1f \quad (1)$$

$$V_2 = \frac{1}{2}(V_{p1} + V_{p2})t_2f \quad (2)$$

$$V_3 = \frac{1}{2}(V_{p2} + V_{p3})t_3f \quad (3)$$

$$V_4 = \frac{1}{2}(V_{p3})t_4f \quad (4)$$

The current passing the link capacitor during each mode determines the amount of increase or decrease of the link voltage:

$$I_1 = C \frac{V_{p1}}{t_1} \quad (5)$$

$$I_2 = C \frac{V_{p2} - V_{p1}}{t_2} \quad (6)$$

$$|I_3| = C \frac{V_{p2} - V_{p3}}{t_3} \quad (7)$$

$$|I_4| = C \frac{V_{p3}}{t_4} \quad (8)$$

where  $C$  is the equivalent link capacitance in each PC, i.e.,  $C = \frac{C_{1P}}{2} = \frac{C_{1S}}{2}$ , and  $C_{1P}$  and  $C_{1S}$  are the capacitances of the capacitors placed on primary and secondary sides of the transformer in each PC, respectively. Using (1)-(8), the transferred power during each mode can be calculated based on  $C, f, V_{p1}-V_{p3}$ . Then, the values of  $V_{p1}-V_{p3}$  can be obtained, resulting in the values of  $t_1-t_5$ .

$$t_1 = \frac{2V_1}{\sqrt{\frac{2fP_1}{C}}} \quad (9)$$

$$t_2 = \frac{2V_2}{\sqrt{\frac{2fP_1}{C} + \frac{2f(P_1 + P_2)}{C}}} \quad (10)$$

$$t_3 = \frac{2V_3}{\sqrt{\frac{2f(P_3 + P_4)}{C} + \frac{2fP_4}{C}}} \quad (11)$$

$$t_4 = \frac{2V_4}{\sqrt{\frac{2fP_4}{C}}} \quad (12)$$

$$t_5 = \frac{1}{f} - t_1 - t_2 - t_3 - t_4 \quad (13)$$

It can be shown that the equivalent link capacitance for each PC can be obtained as follows:

$$C \leq \frac{P_T/2}{2f \left( \frac{1}{2} V_{in-peak} + V_{o-peak} \right)^2} \quad (14)$$

$$C_{1P} = C_{2P} = C_{1S} = C_{2S} = 2C \quad (15)$$

where  $V_{in-peak}$ ,  $V_{o-peak}$ , and  $P_T$  are the peak values of the line-line input and output voltages and the rated power, respectively.  $C_{1P}$ ,  $C_{1S}$ ,  $C_{2P}$ , and  $C_{2S}$  are the link capacitances of the primary and secondary side of the transformer in PC1 and PC2, respectively. To operate in DCM, the required link capacitance for each PC should be smaller than the value obtained in (14). Once the required capacitance is chosen, the maximum link voltage of each power cell ( $V_{link-max}$ ) can be calculated using (16).

$$V_{link-max} = \sqrt{\frac{P_T}{Cf}} \quad (16)$$

According to (16), choosing a very small value for the link capacitance will increase the link peak voltage. To minimize the peak value of the link voltage, the value selected for the link capacitance need to be close to the maximum value determined by (14). In this case the link peak voltage can be approximated using (17). It can be observed because of using two PCs at the input side, the peak value of the line-line voltages at the input terminals of each PC is divided by two, leading to a lower value for the link voltage in each PC.

$$V_{link-max} \cong 2 \left( \frac{V_{in-peak}}{2} + V_{o-peak} \right) \quad (17)$$

## IV. SIMULATION RESULTS

In order to evaluate the performance of the proposed topology, a three-phase ac-ac converter with two PCs in ISOP structure is designed and simulated in PSim. Specifications of the investigated system are listed in Table I. According to (14), the selected equivalent link capacitance for each PC is 0.1  $\mu$ F, which is very small for a 10 kW power converter. Figs. 7 and 8 represent the line-line voltages and phase currents references of the input and output of each PC, respectively. Fig. 9 shows the input three-phase currents. The three-phase output currents of PC1 and PC2, and the total output three-phase currents are shown in Figs. 10 (a), (b), and (c), respectively. In the ISOP structure, the output phase currents are divided between the two PCs. The RMS of the total output current is equal to 57.7 A, while the RMS of output current in each PC is equal to 28.8 A.

TABLE I. SPECIFICATIONS OF THE INVESTIGATED SYSTEM.

Parameter	Value
Power Rating	10 kW
Input Voltage	500 V (L-L, RMS)
Output Voltage	100 V (L-L, RMS)
Load	L=200 $\mu$ H, R= 1 $\Omega$
Input L Filter	3 mH
Link Frequency ( $f$ )	50 kHz
Equivalent Link Capacitance of each PC ( $C$ )	0.1 $\mu$ F

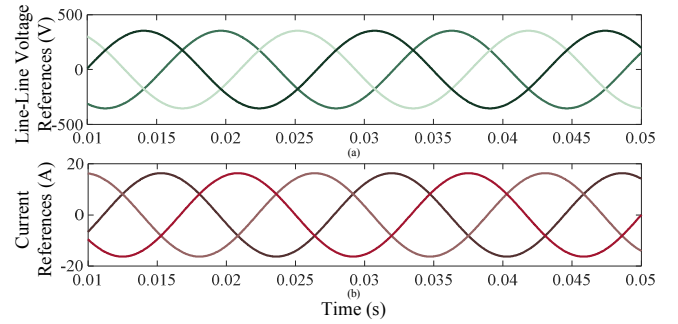


Fig. 7. The input side line-line voltages and phase currents references.

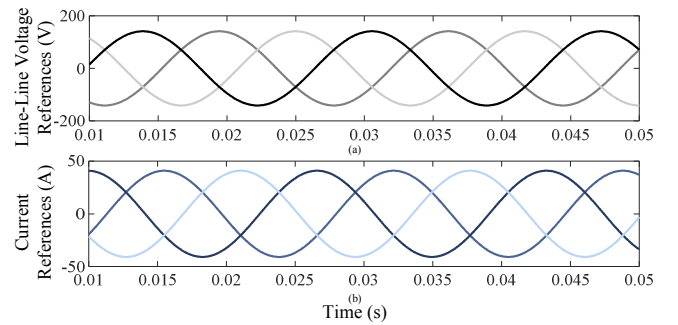


Fig. 8. The output side line-line voltages and phase currents references.

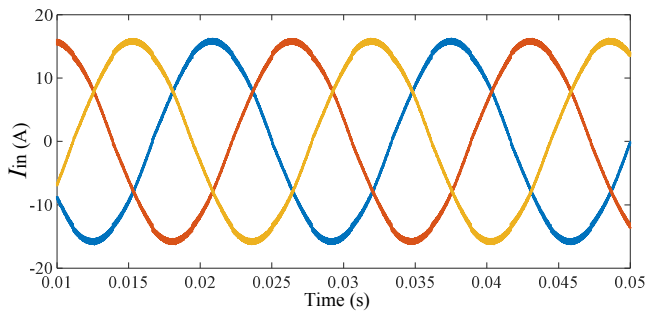


Fig. 9. The three-phase input currents.

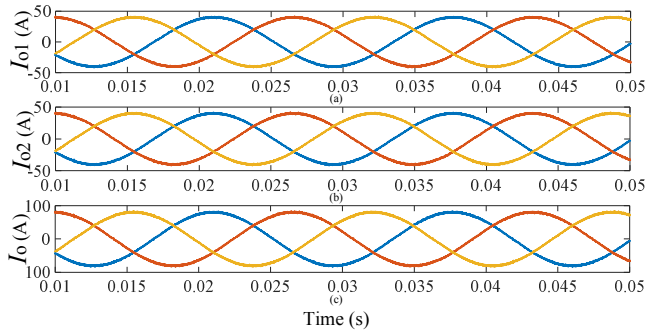


Fig. 10. The simulations results of the ISOP converter, (a) output currents of PC1, (b) output currents of PC2, (c) total output currents.

Figs. 11 (a) and (b) present the link voltage and current of primary side link capacitor in each PC. The peak value of the primary side link capacitor of each PC is low, due to series-connection of the input side. Also, the discharging link current is divided between the two PCs. The peak discharging link current is equal to 41 A in each PC, while the peak output current is equal to 82 A, which verifies the effectiveness of the proposed approach for sharing the current at the output side. Moreover, the operation of fifth mode is clear in Figs. 11 (a) and (b), during which the link current and voltage are equal to zero. Figs. 12 (a) and (b) depict the unfiltered input line-line voltages at the terminals of each PC. Also, Fig. 12 (c) represents the unfiltered input line-line voltages at the terminals that the two PCs are connected, which are equal to the summation of voltages shown in Figs. 12 (a) and (b). Fig. 13 depicts the unfiltered output line-line voltages of both PCs. Since the output terminals are connected in parallel, the unfiltered output line-line voltages of both PCs are the same.

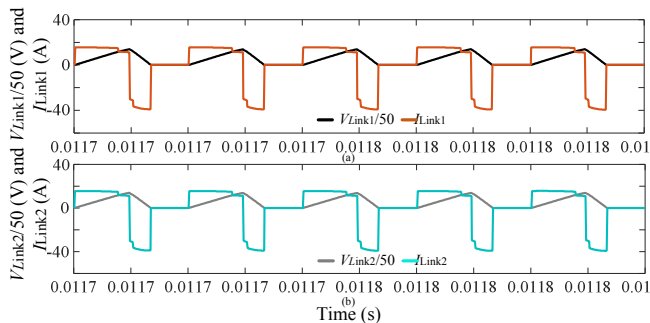


Fig. 11. The link current and voltage of primary side link capacitor in each PC.

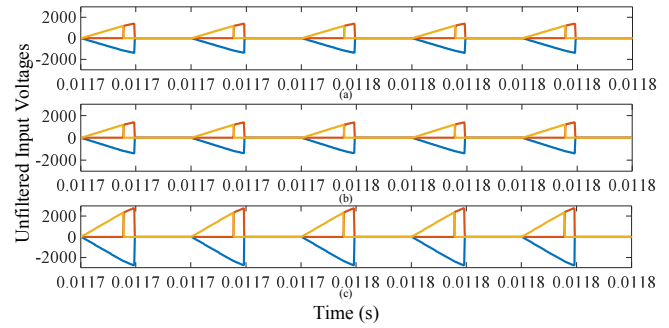


Fig. 12. Simulation results of the ISOP converter, (a) Unfiltered input line-line voltages of PC1, (b) Unfiltered input line-line voltages of PC2, (c) Unfiltered input line-line voltages at the point of connection of both PCs.

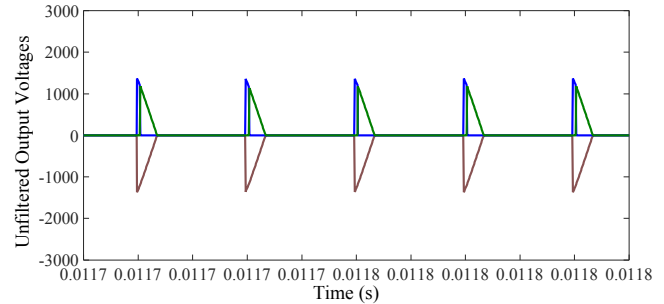


Fig. 13. The unfiltered output line-line voltages of both PCs at the point of their connection.

Fig. 14 (a) presents the voltage stress across the switches S1 and S1o (in PC1), which are the same and equal to the total link voltage of the PC1. Also, Fig. 14 (b) illustrates the voltage stress across the switches S12 and S12o (in PC2), which are the same and equal to the total link voltage of PC2. These voltages are smaller than those of a converter with a single PC, because of the series-connection of the input side converter. This allows using the commercialized semiconductor switches in applications with higher voltages. The duration of modes 1-5 are shown in Fig. 15, which clarifies that the duration of each mode changes over time according to the reference values of line-line voltages and line currents.

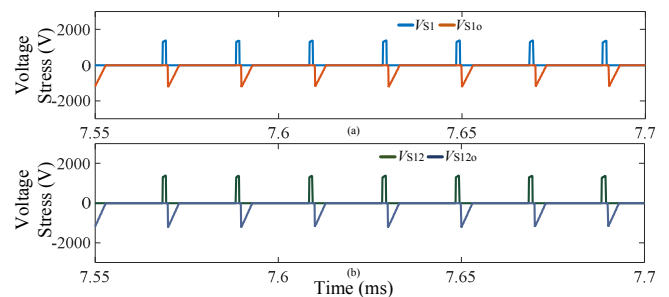


Fig. 14. The voltage stress across (a) S1 and S1o in PC1, (b) S12 and S12o in PC2.

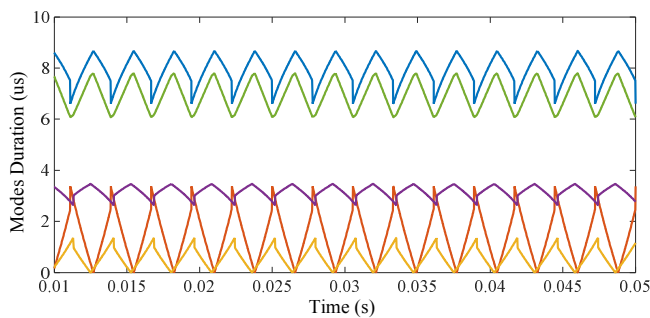


Fig. 15. The duration of modes 1-5.

## V. CONCLUSION

In high power systems with high currents or voltages, which are above the rated current or voltage of the commercialized switches, power conversion is typically accomplished through multilevel converters. Most of the existing multilevel converters require dc electrolytic capacitors, which are known as the bottleneck of these systems due to their low reliability, short life-time, and large size. This paper introduced a three-phase ac-ac converter with two power cells for high power applications, which is inspired by a three-phase series-ac-link ac-ac converter that uses small film capacitors for transferring the power. This feature increases the reliability and power density of the proposed ISOP converter. Furthermore, this converter benefits from high frequency voltage variations across the link capacitors that allows using high frequency transformers for isolation. The proposed ISOP converter is a promising solution for applications that deal with high voltages at the input side and high currents at the output side. The principles of the operation of the proposed converter were described in this paper. The simulation results for a 10 kW three-phase system verified that the proposed converter can effectively accomplish the voltage and current sharing at the input and output side.

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