SiC Solid State Circuit Breaker with an Adjustable Current-Time Tripping Profile

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***Abstract*—This paper reports a SiC-based solid-state circuit breaker (SSCB) with an adjustable current-time (*I-t*) tripping profile for both ultrafast short circuit protection and overload protection. The tripping time ranges from 0.5 microsecond to 10 seconds for a fault current ranging from 0.8X to 10X of the nominal current. The *I-t* tripping profile, adjustable by choosing different resistance values in the analog control circuit, can help avoid nuisance tripping of the SSCB due to inrush transient current. The maximum thermal capability of the 1200V SiC JFET static switch in the SSCB is investigated to set a practical thermal limit for the *I-t* tripping profile. Furthermore, a low fault current 'blind zone' limitation of the prior SSCB design is discussed and a new circuit solution is proposed to operate the SSCB even under a low fault current condition. Both simulation and experimental results are reported.**

Keywords—Solid State Circuit Breaker; Adjustable Current-Time Tripping Profile; Inrush Current; Upper and Lower Limitation; SiC JFET

I. INTRODUCTION

With the increasing interest in DC power distribution networks, fast-acting solid state circuit breakers (SSCB) become a critical enabling technology to provide protection against circuit faults [1]-[5]. SiC JFETs become an excellent static switch in the SSCBs because of their very low on-resistance and repetitive energy absorption capability [6]-[10]. A self-powered, ultrafast, autonomously operated SSCB concept was introduced in [11]-[14], which can interrupt a fault current up to 180A within 0.7 μs at a DC bus voltage of 400V. However, the previous work only reported the ultrafast reaction of the SSCB to a single fault current level, raising the question whether or not the SSCB is susceptible to false triggering (nuisance tripping) in the event of inrush currents during the startup of power supplies or motors. In comparison, a traditional electromechanical circuit breaker offers a current-time (*I-t*) tripping profile, which includes "instantaneous" tripping (typically tens of milliseconds) at a high short circuit fault current, and overload tripping for a much lower overload current but after a much longer time duration (seconds) [15]-[18]. The *I-t* tripping profile can help distinguish an inrush current from a short circuit fault current, and reduce nuisance tripping to a certain extent. In addition, selective coordination among multiple mechanical circuit breakers with different *I-t* tripping profiles can be realized in a hierarchical power system. The instantaneous tripping is based on a magnetic mechanism while the overload tripping is based on a thermal mechanism in a mechanical circuit breaker. To generate the *I-t* response profile, the thermal-magnetic circuit breaker must have an adjustable thermal-sensitive element and an adjustable current-sensitive electromechanical element[19]-[20].

In this paper, we present an expanded current-time response profile for the previously reported SSCB [11]-[14], which is similar to that of a traditional thermal-magnetic circuit breaker except for a much faster short circuit response time in the μs range. The *I-t* response profile can be further adjusted by choosing different resistors in the SSCB analog control circuit. A mechanical circuit breaker current time profile contains two distinct regimes: the short circuit regime (typically 10-100ms) and the overload regime (typically 1-1000s) [21]-[23]. Similarly, the new SSCB emulates these characteristics of the mechanical breaker. For the short circuit regime, the SSCB offers a current-time profile with a response time of 0.5-300 μs for a short circuit fault current ranging from 2 to 10 times of the nominal current. For the overload regime, the SSCB offers a current-time profile with a response time of 0.3-10 seconds for an overload current ranging from 0.8 to 2 times of the nominal current. The previously reported SSCB does not respond at all to an overload current below the preset threshold for short circuit faults, exhibiting a so-called "blind zone" between the short circuit threshold and the nominal current. A new analog control circuit is designed which eliminates this "blind zone", and extends the response time into the second range for the overload protection. The maximum fault or overload current capability of the SSCB is limited by the thermal capability of the semiconductor power switch. To this end, we theoretically analyze and experimentally characterize the current-time capability of the commercial 1200V normally-on SiC JFET (USCi UJN1205K [24]) to identify the upper limit of the *I-t* response profile for the SSCB.

II. CURRENT-TIME TRIPPING PROFILE OF MECHANICAL CIRCUIT BREAKERS

Fig. 1 shows the two distinct regimes of a mechanical circuit breaker current-time profile. To define the two regimes, several important parameters are used for a mechanical breaker in Table I and Fig. 1.

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TABLE I. CURRENT-TIME PARAMETERS OF MECHANICAL CIRCUIT BTEAKERS

Symbols	Definition
U_e	Rated operational voltage
I_n	Rated current
I_r	Overload trip current setting
I_m	Short circuit trip current setting
I_{cu}	Rated short circuit capability
I_{cs}	maximum perspective fault current which a circuit breaker can clear and remain serviceable

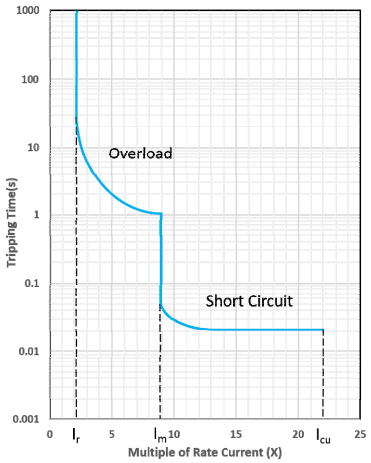


Fig. 1. Typical current time curve of mechanical circuit breaker

By adjusting the thermal-sensitive and current-sensitive elements, the typical current-time curve of a mechanical circuit breaker can be modified to distinguish between a short circuit fault current and a startup inrush current. The curve in Fig.1 shows that I_r, I_m, and I_{cu} are the main parameters for the two operating regimes. The current-time profile is defined by these parameters. Overload trip current setting I_r is typically 0.7 to 2 times of the rated current. This parameter is determined by the thermal-sensitive element. It also represents the maximum nominal current that the circuit breaker can carry without tripping. Short circuit trip current setting I_m is determined by the current-sensitive element. This parameter defines the threshold current to quickly trip the circuit breaker in the event of a short circuit fault. The rated short circuit capability I_{cs} defines the maximum fault current that the circuit breaker can safely interrupt. I_{cu} is the maximum perspective fault current which the circuit breaker can still clear while the breaker may be damaged after the fault.

III. SHORT CIRCUIT TRIPPING REGIME OF SSCB

A. Basic Operation of SSCB

The basic operation principle of the SSCB is described here. Fig. 2 illustrates the circuit schematic of the self-powered, ultrafast, autonomously operated bidirectional SSCB [11]. It basically comprises two common source normally-on SiC JFETs as the main static switch; a fast-starting isolated DC/DC converter as the protection driver; a power supply circuit for the driver; and a diode bridge to convert bidirectional power into one direction for the power supply. When the load is shorted under a short circuit fault, the SSCB detects the fault by sensing the voltage rise across the JFETs. The sudden increase of the JFETs drain-source voltage will charge capacitor C2 through the diode bridge. When the capacitor voltage exceeds a certain threshold value, the protection driver circuit will be activated to turn off the JFETs. From the circuit schematic, it is apparent that the turnoff time of the JFET is mainly determined by the charging time of capacitors C2 and C3. C2 needs to be charged up to the threshold voltage of the protection driver circuit, and C3 needs to be charged to a negative voltage below the threshold voltage of JFETs to turn them off. Furthermore, the charging time of the two capacitors is dependent on the value of R2, R3, C1, C2, and C3 as well as the fault current level. The values of these five components can be adjusted to provide an adjustable current-time profile for the SSCB.

B. Short Circuit Tripping Profile of SSCB

A simple approach for generating an adjustable current-time profile is to vary R2 in the power supply circuit in Fig. 2 while keeping all other components unchanged. By tuning R2 (e.g. using a potentiometer for R2), the charging time of the self-power circuit, and subsequently the response time of the SSCB can be adjusted.

Fig. 3 shows the measured SSCB response waveforms. Waveforms in BLUE are the JFET drain current I_{DS}, RED the JFET gate voltage V_{GS}, GREEN the JFET drain-source voltage V_{DS}, and YELLOW the C2 voltage V_{C2}, respectively. Figs. 3 (a) and (b) compare the waveforms of the SSCB with the same RC values but at different fault current levels. It is observed that a higher fault current leads to a shorter response time, as a result of a higher voltage across the SSCB. Figs. 3 (c) and (d) compare the waveforms of the SSCB at the same fault current but with different R2 values. It is observed that a smaller R2 leads to a shorter response time. An adjustable current-time tripping profile can therefore be generated for an R2 of 10, 50, 100, 150 and 200Ω, as shown in Fig. 4. Each curve in Fig. 4 represents the tripping current-time characteristic for a certain R2 value. If we choose a variable R2 in the SSCB design, the SSCB can offer a programmable *I-t* tripping profile. The blue shaded area in Fig. 4 is equivalent to the short circuit regime of a traditional mechanical circuit breaker except for the SSCB offers a response time of 0.5-300 μs instead of 10-100ms. With this set of resistance selection, the I_m value ranges from 2.6X to 10X of the rated current of the JFETs (38A) in the SSCB.

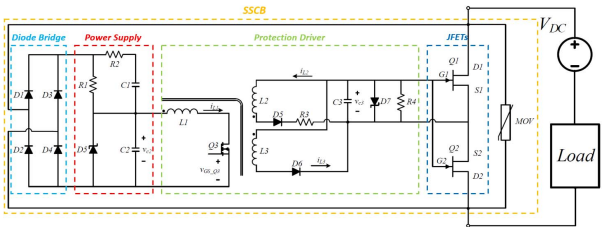
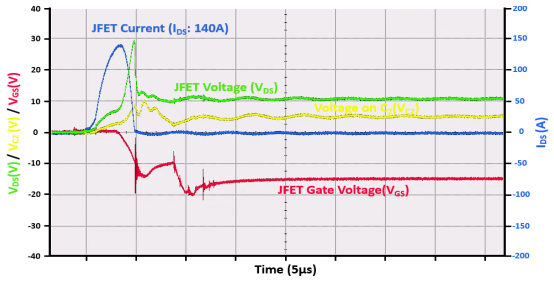
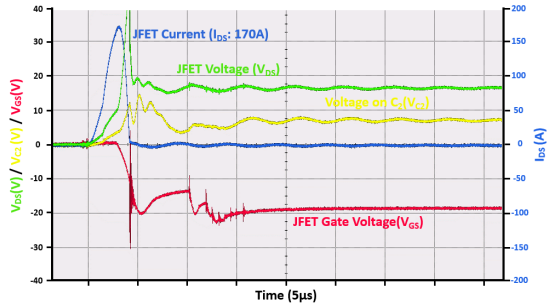


Fig. 2. Circuit schematic of the proposed bidirectional self-powered SSCB.



(a)



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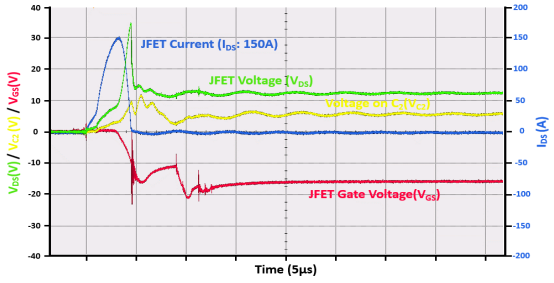
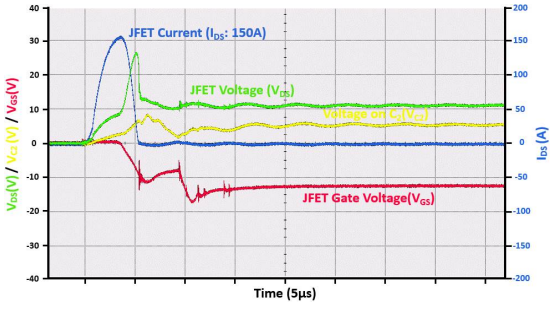


(c)



(d)

Fig. 3. Measured SSCB switching waveforms showing the influence of fault current and R2 on tripping time: (a) fault current of 140A and tripping time of 5 µs; (b) fault current of 170A and tripping time of 4 µs; (c) R2 of 5.6 Ω and tripping time of 4.5 µs at 150 A; and (d) R2 of 10 Ω and tripping time of 5.5 µs at 150 A.

The I_m range for the SSCB is narrower than that of a mechanical circuit breaker because of the thermal capacity limitation on the SiC JFET chip. More detailed discussion will be provided in Section V.

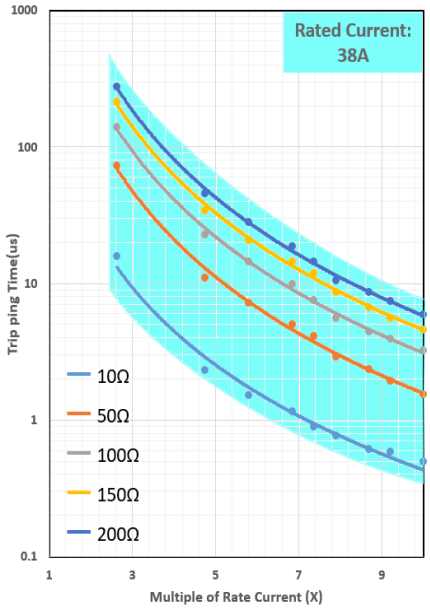


Fig. 4. Measured SSCB short circuit current-time tripping profile for R2 of 10 Ω, 50 Ω, 100 Ω, 150 Ω, and 200Ω, respectively.

IV. Overload Tripping Regime of SSCB

With the short circuit current time profile, the SSCB can interrupt a fault current from 2.6X to 10X of the nominal current within 0.5-300 µs, sufficiently fast to protect the power electronic equipment in the network. However, the SSCB also needs to wait for a much longer time before reacting to a considerably lower overload current, similar to a thermal-magnetic mechanical circuit breaker. This particular characteristics may allow the SSCB to endure an inrush current scenario during the startup of the equipment without false tripping. We select 0.8X to 2X of the SiC JFET rating (38A) as the overload current range for the SSCB in this study to protect the circuit from overload conditions and to prevent false tripping due to startup inrush currents. The overload tripping regime offers a long delay time of 0.35 to 10 seconds. The delay time should be selected based on both the system requirement and the maximum thermal capability of the SiC JFET. This later subject will be discussed in Section V. Using the convention of the mechanical circuit breaker, the overload trip current setting of SSCB I_r is 0.8X of the nominal current rating for the 1200V SiC JFET.

To allow such a long delay time for the SSCB, both the fault detection circuit and the self-power circuit need to be modified. The SSCB detects a circuit fault by measuring the voltage drop across the SiC JFETs. It will trip when the voltage across C2 is charged higher than the threshold of the protection converter circuit. When there is an overload current in the range of 0.8X to 2X of the nominal current, the voltage drop across the SiC JFETs is between 2.7V and 7.0V, which is lower than the threshold of the original SSCB design. The SSCB will therefore not trip under this overload condition, exhibiting a so-called "blind zone" of its operation. A new fault detection circuit and a modified self-power circuit are proposed

to eliminate the “blind zone” and extend the response time, as shown in Fig. 5.

It is not practical to boost the output voltage of the self-power circuit under the “blind zone” condition since it will increase circuit complexity. Instead we choose to lower the input threshold voltage for the JFET gate driver circuit by using a different control IC (TPS43000) which has a supply voltage range of 1.65V to 9V (a significant reduction from the supply voltage of 7-40V of TL494 in the previous SSCB circuit). In the new power supply circuit, we adjust C1 and C2 values to reduce its initial transient voltage output so the SSCB will not be activated instantaneously in the 0.8X-2X overload current range. C2 will be eventually charged to a higher voltage through R4, and then activate the JFET gate driver circuit. The RC charging time of R4 and C2 will determine the overload response time of the SSCB. These changes in R4, C1, and C2 allow the SSCB to trip only after a preset long delay time (0.35-10 seconds). With the changes in C1 and C2, the output voltage across C2 will become excessive under a short circuit fault condition. To solve this problem, we add a new voltage reduction circuit made of R5, C3, C4, C5, and a small power MOSFET M1. The voltage reduction circuit is not activated under the overload condition. However, under a short circuit fault (higher SSCB voltage), the voltage across C4 will become high enough to turn on the MOSFET M1. Then C5 and C2 are now in parallel and the transient voltage across them is reduced, and the stress on the parallel Zener diode D1 is relieved. It will help to limit the start inrush current go through the Zener diode when the voltage is higher than a certain level. The new power supply circuit will nonlinearly convert an input voltage range of 2.7V to 128V to an output range of 1.65V to 9V, a perfect voltage supply range for the control IC operation.

The purpose of the new fault detection circuit is to cut off the input voltage to the power supply circuit, which is made of two resistors R1 and R2, and a small thyristor X1. By turning off the thyristor X1 when the current through the SSCB is in a normal range (<0.8X of the rated current of the SiC JFET), there is no power supplied to the gate driver circuit and the JFET will remain in the ON state. The fault detection circuit does not impact the operation of the SSCB circuit at all when the current is over 0.8X of the rated current. Fig. 6 shows the measured output voltage of the new power circuit as a function of the input voltage, which is essentially the voltage across the SSCB. The red dot on the curve indicates the threshold voltage of the power circuit, below which there is no power supplied to the SiC JFET gate driver.

The delay time of the power supply circuit is measured as a function of the overload current for various R4 values, as shown in Fig. 7. For an overload current of 0.8-2X of the nominal current, a response time of 0.35-10 seconds is observed. The response time can also be adjusted by choosing a large R4 value. The blue shaded area shows the available operating area of the SSCB, similar to that of a mechanical circuit breaker. This large adjustable tripping time range can provide a flexible protection for the system overload fault situation without nuisance tripping due to inrush current.

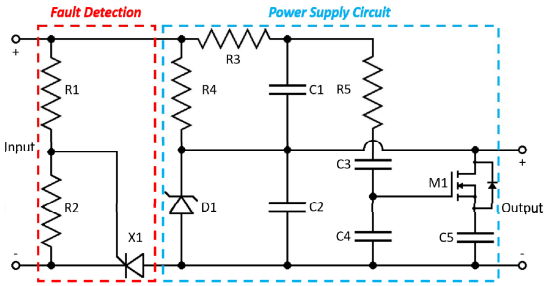


Fig. 5. Circuit schematic of the new SSCB fault detection circuit and self-power circuit design.

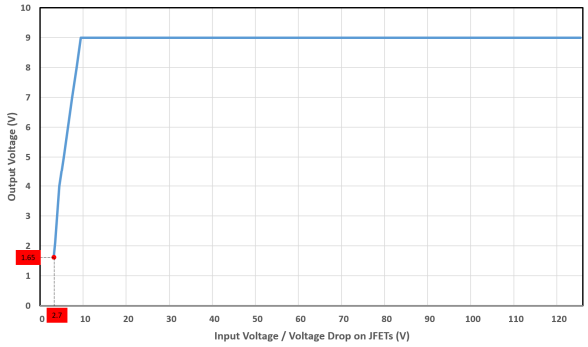


Fig. 6. Measured output voltage of the new power circuit as a function of input voltage (the voltage across the SSCB).

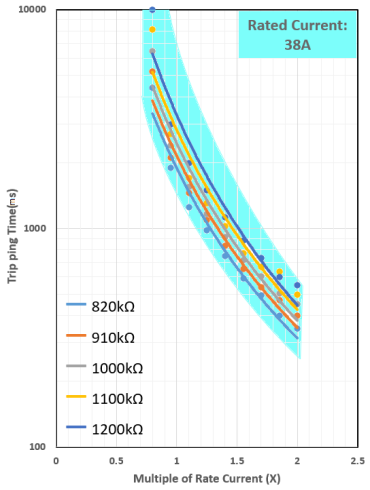


Fig. 7. Measured SSCB overload current-time tripping profile for R4 of 810kΩ, 920kΩ, 1000kΩ, 1100kΩ, and 1200kΩ, respectively.

V. Maximum Fault Current Capability of SiC JFET

The thermal stress of the SiC JFET chip during a prolonged delay becomes a concern for the overload operation of the SSCB. Even for the short circuit tripping regime, there is a thermal concern for the range of lower fault currents but longer response times. To find out the maximum fault current

capability of the SSCB, overcurrent capability of the SiC JFET is studied, which is mainly limited by its thermal capability.

Using the datasheet transient thermal impedance parameters, we calculate the current-time limit of the SiC JFET while not exceeding a maximum junction temperature of 175℃, as shown in Fig. 8. The x-axis is the multiple of the rated current. The y-axis is the maximum pulse width that the SiC JFET can conduct without exceeding 175℃. For a fault current of 3X to 10X of the rated current (38A), the maximum pulse width ranges from 15 µs to 1 ms. This calculation is based on the assumption of 25℃ ambient temperature. In practice, the limit may be lower than this result if the ambient temperature is higher than the assumption. For current lower than two times of the rated current, the conduction time limit is longer than 10 seconds. These thermal capability calculations can be used to correlate with the overload and short circuit current-time profiles of our SSCB design.

In addition, we measure the pulse current capability of the SiC JFET using a capacitor discharge circuit with a pulse width of 10 µs. Fig. 9 shows the pulsed JFET current I_D as a function of the measured V_{DS}. Both the measured data (in blue) and the datasheet values (in orange) are included. The difference between two lines is results of testing circuit impedance and testing environment condition. It is observed that the 1200V SiC JFET can safely conduct 380A (10X nominal current) for more than 10 µs.

The threshold voltage of 1.65V for the control IC sets a lower limit for the overload trip current I_r to 0.6X of the nominal current. The JFET theoretically conduct 1X of nominal current continuously. We select an I_r of 0.8X of the nominal current for the SSCB. Maximum pulse width drops quickly when the current level exceeds 3X of the nominal current. Based on the above thermal analysis and characterization results, we select an I_m of 2X of the nominal current without exceeding the maximum junction temperature of 175℃, which also meets the requirement of most power systems. The SSCB tripping profile can therefore be adjusted based on system requirements and these design considerations.

A final current-time profile of the new SSCB is shown in Fig. 10, which includes both the short circuit and overload regimes. The main circuit breaker tripping parameters of the SSCB are summarized in Table II.

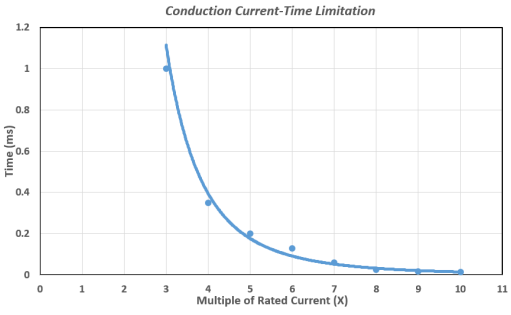


Fig. 8. Calculated 1200V SiC JFET current-pulsewidth limit to keep Tjmax below 175℃.

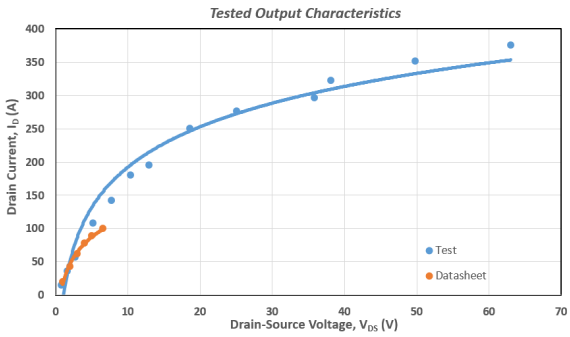


Fig. 9. Measured V_{CE} as a function of I_{CE} of JFET compared with datasheet value.

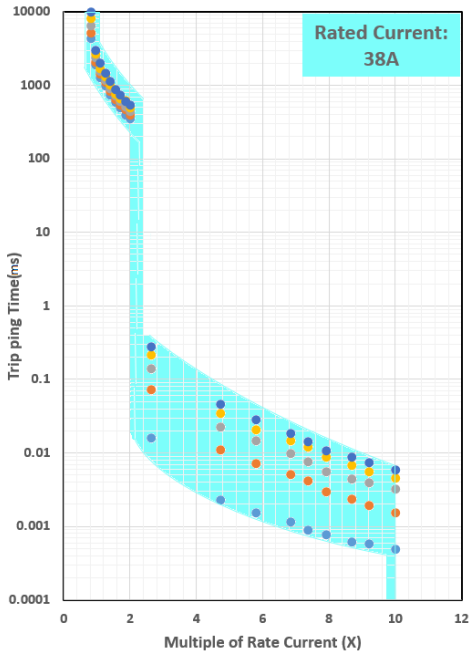


Fig. 10. Final current-time tripping profile of the proposed SSCB with various resistor selections.

TABLE II. CURRENT-TIME PARAMETERS OF SSCB

Symbols	Definition	Value
U_e	Rated operational voltage	380V
I_n	Rated current	38A
I_r	Overload trip current setting	0.8X
I_m	Short circuit trip current setting	2X
I_{cu}	Rated short circuit capability	10X
I_{cs}	maximum perspective fault current which a circuit breaker can clear and remain serviceable	10X

VI. CONCLUSION

In this paper, a SiC JFET based SSCB with an adjustable current-time (*I-t*) tripping profile for both ultrafast short circuit protection and overload protection is reported. The measured current-time profile of the SSCB is similar to that of commercial mechanical circuit breakers except for a much faster short circuit response time in the µs range. For the short circuit regime, the SSCB offers a current-time profile with a response time of 0.5-300 µs for a short circuit fault current ranging from 2 to 10 times of the nominal current. For the overload regime, the SSCB offers a current-time profile with a response time of 0.3-10 seconds for an overload current ranging from 0.8 to 2 times of the nominal current. The *I-t* response profile of the SSCB can be further adjusted by choosing different resistors in the SSCB analog control circuit. The *I-t* tripping profile helps to avoid nuisance tripping of SSCB due to inrush transient current, and to accommodate selective coordination among multiple SSCBs with different *I-t* tripping profiles in a hierarchical power system. A new control circuit design is proposed to allow the SSCB to react to low overload currents after a long response time in a range up to 10 seconds. The maximum thermal capability of the 1200V normally-on SiC JFET used as the static switch in the SSCB is also investigated both theoretically and experimentally to identify the upper fault current limit of the SSCB.

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