Optimum Harmonics Injection to Minimize Bus Capacitance of CRM Boost PFC Conveters Meeting EN61000-3-2 Class D Limits

Zhehui Guo, Xiaoyong Ren, Yu Wu, Lei Bai, Zhiliang Zhang, Qianhong Chen
Jiangsu Key Laboratory of New Energy Generation and Power Conversion
Nanjing University of Aeronautics and Astronautics (NUAA)
Nanjing, Jiangsu, P. R. China
E-mail: guozhehui@nuaa.edu.cn

***Abstract*—Based on the energy-ripple perspective, this paper discusses the optimum 3rd and 5th order harmonic injection to minimize bus capacitance of CRM boost PFC converters. Within EN61000-3-2 Class D limits, 34% 3rd and 19% 5th order harmonics injection can theoretically achieve the maximum bus capacitance reduction of 36.1% for wide input application (100~240Vac). However, the conventional on-time control ignores the deviation effect of CRM operation, which introduces the exceeding 3rd and 5th order injected harmonics than EN61000-3-2 Class D limits. In order to eliminate the deviation effect, a novel on-time compensation method is proposed to realize accurate harmonics injection. The experimental results from an 120W prototype show that the maximum bus capacitance reduction of 33% is achieved in practice meeting EN61000-3-2 Class D limits within 100~240Vac input range.**

Keywords—harmonics injection; bus capacitance; CRM boost PFC; on-time compensation; EN61000-3-2 Class D

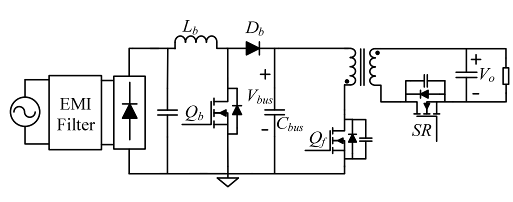
I. INTRODUCTION

Ac-dc adaptors above 75W usually employ the two-stage topology composed of a power factor correction (PFC) stage and an isolated dc-dc converter (see Fig.1) [1, 2]. The PFC stage achieves high power factor (PF) and low input current total harmonic distortion (THD). Fly-back or LLC dc-dc converters are employed to provide the isolated voltage step-down. LLC dc-dc converters can operate as the dc transformer (DCX) to improve efficiency and in this case, the output voltage of the adaptor will be regulated by PFC stage indirectly [3]. Increasing the switching frequency can effectively reduce the size of the boost inductor size and EMI filter [4, 5]. However, it has no effect on reducing the bulky bus capacitance, which limits the power density of ac-dc adaptors. For the ac-dc adaptor with DCX structure, the bus capacitance is considerable due to the strict voltage ripple requirement of the post stage.

Many methods are proposed to shrink the bus capacitance of PFC stage [6]-[10]. A bidirectional converter is adopted to decouple the ripple power but it complicates the control circuit and impairs the reliability [6]. The bus capacitance is reduced by a larger voltage ripple design [7], which deteriorates efficiency and is not suitable for the DCX structure. The peak-to-average ratio is minimized by the certain 3rd and 5th order harmonics injection in LED drivers [8]. However, the bus capacitance is not minimized meanwhile. The 3rd, 5th and 7th order harmonics are injected into a 65W ac-dc adaptor (without harmonic limits) to reduce the bus capacitance above 50% [9]. The partial constant power control obtains the constant output current during the partial line cycle [10]. However, the relation between the controlled variable and the harmonics content is not clear, resulting in an inevitable trail-and-error design. Aiming at ac-dc adaptors above 75W, this paper discusses clearly the relation of the injected harmonics ratio and the bus capacitance in CRM boost PFC converters meeting EN61000-3-2 Class D limits within 100~240Vac range.

Moreover, the practical CRM operation introduces negative inductor current and delayed switching period [11]-[13], making actual input current deviate from ideal waveforms. With the conventional control method, deviation effect of CRM introduces the excessive 3rd and 5th order injected harmonics beyond EN61000-3-2 Class D limits. Therefore, this paper also investigates the on-time compensation to eliminate deviation effect and obtain accurate harmonics injection.

From the energy-ripple perspective, this paper discusses the optimum 3rd and 5th order harmonics injection to minimize the bus capacitance of CRM boost PFC converters. Within EN61000-3-2 Class D limits, 34% 3rd and 19% 5th order harmonics injection can theoretically achieve the maximum bus capacitance reduction of 36.1% for 100-240Vac input range. In order to eliminate deviation effect of CRM, this paper adopts a novel on-time compensation method to achieve accurate harmonic injection. The experimental results from an 120W prototype show that maximum bus capacitance reduction of 33% is achieved in practice within EN61000-3-2 Class D limits.



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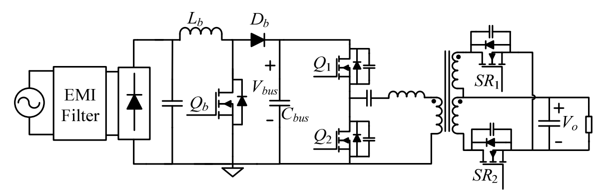


(b)

Fig. 1. Typical two-stage topology of the ac-dc adaptor above 75W. (a) Boost PFC + Fly-back dc-dc converter. (b) Boost PFC + LLC dc-dc converter.

II. Optimum Injection Ratios of the 3rd and 5th Order Harmonics

A. Relation of capacitance energy-ripple and bus capacitance

The bus capacitance C is an energy storage element and its energy E_C is a function of its voltage V_C as

$$E_C=\frac{1}{2}CV_C^2 \tag{1}$$

From (1), the maximum bus voltage V_{Cmax} corresponds to the maximum energy E_{Cmax} and the minimum bus voltage V_{Cmin} corresponds to the minimum energy E_{Cmin}, so the capacitance energy-ripple $E_{Cp\text{-}p}$ can be expressed as follows

$$E_{Cp\text{-}p}=E_{C\max}\text{-}E_{C\min}=\frac{C}{2}\left(V_{C\max}^2\text{-}V_{C\min}^2\right)=\frac{C}{2}\left(V_{C\max}+V_{C\min}\right)V_{Cp\text{-}p} \tag{2}$$

where $V_{Cp\text{-}p}$ is the bus voltage ripple, the difference of V_{Cmax} and V_{Cmin}. Define the average value of V_C during the half line cycle as V_{Cavg}. When only the odd order harmonic currents are injected, V_{Cmax}-V_{Cavg}=V_{Cavg}-V_{Cmin}, thus (2) can be rewritten as

$$E_{Cp\text{-}p}=CV_{Cavg}V_{Cp\text{-}p} \tag{3}$$

From (3), C is proportional to $E_{Cp\text{-}p}$ with the given $V_{Cp\text{-}p}$ requirement. Thus, the lower $E_{Cp\text{-}p}$ leads to the lower C.

B. Calculation of the capacitance energy-ripple

The input voltage v_{in} is defined as

$$v_{in}(\omega t)=\sqrt{2}U_{rms}\sin\omega t \tag{4}$$

where ω is the line angular frequency and U_{rms} is the input RMS voltage. Ignoring the phase displacement between v_{in} and the fundamental component of the input current i_{in}, and i_{in} with the 3rd and 5th order harmonics injection can be defined as

$$i_{in}(\omega t)=\sqrt{2}I_{rms}\left(\sin\omega t+I_3^*\sin 3\omega t+I_5^*\sin 5\omega t\right) \tag{5}$$

where I_{rms} is the fundamental component RMS of i_{in}, I_3^* and I_5^* are the normalized amplitude of 3rd and 5th harmonics current with the base of I_{rms}, respectively. From (4) and (5), the instantaneous input power p_{in} can be derived as

$$\begin{aligned}p_{in}(\omega t)&=v_{in}(\omega t)i_{in}(\omega t)\\&=2U_{rms}I_{rms}\sin\omega t\left(\sin\omega t+I_3^*\sin 3\omega t+I_5^*\sin 5\omega t\right)\end{aligned} \tag{6}$$

Suppose the unity system efficiency, thus the output power equals to the average input power, that is

$$P_o=P_{in}=\frac{1}{\pi}\int_0^{\pi}p_{in}d\omega t=\frac{1}{\pi}\int_0^{\pi}v_{in}i_{in}d\omega t=U_{rms}I_{rms} \tag{7}$$

when $p_{in}>P_o$, C is charged and V_C increases, thus E_C increases; when $p_{in}<P_o$, C is discharged and V_C decreases, thus, E_C decreases. Integrate (p_{in}-P_o) on time to obtain the increment of E_C as follows

$$\Delta E_C(\omega t)=\int_0^{\omega t}\left(p_{in}\text{-}P_o\right)d\omega t \quad \omega t\in(0,\pi) \tag{8}$$

From (8), $\Delta E_C(\omega t)$ is a function of time. Define the initial value of E_C at instant as E_{C0}, the variation of E_C during the half line cycle can be expressed as

$$E_C(\omega t)=E_{C0}+\Delta E_C=\int_0^{\omega t}\left(p_{in}\text{-}P_o\right)d\omega t \quad \omega t\in(0,\pi) \tag{9}$$

From (9), E_{Cmax} and E_{Cmin} are

$$E_{\max}=E_{C0}+\Delta E_{C\max}=E_{C0}+\max\left(\int_0^{\omega t}\left(p_{in}\text{-}P_o\right)d\omega t\right) \quad \omega t\in(0,\pi) \tag{10}$$

$$E_{\min}=E_{C0}+\Delta E_{C\min}=E_{C0}+\min\left(\int_0^{\omega t}\left(p_{in}\text{-}P_o\right)d\omega t\right) \quad \omega t\in(0,\pi) \tag{11}$$

From (10) and (11), $E_{Cp\text{-}p}$ can be calculated as follows

$$E_{Cp\text{-}p}=\max\left\{\int_0^{\omega t}\left(p_{in}\text{-}P_o\right)d\omega t\right\}\text{-}\min\left\{\int_0^{\omega t}\left(p_{in}\text{-}P_o\right)d\omega t\right\} \quad \omega t\in(0,\pi) \tag{12}$$

C. Relation of capacitance energy-ripple and the 3rd and 5th order harmonics injection

From (6) and (12), we know that the essence of harmonics injection is to reduce $E_{Cp\text{-}p}$ by reshaping i_{in} or p_{in} during the half line cycle. $E_{Cp\text{-}p}$ with different 3rd and 5th order harmonics injection can be calculated according to (12). Fig.2 shows the three dimensional map of $E_{Cp\text{-}p}^*$, I_3^* and I_5^*. $E_{Cp\text{-}p}^*$ is the normalized amplitude of capacitance energy-ripple with the base of $E_{Cp\text{-}p}$ when $I_3^*=I_5^*=0$.

From Fig.2, the minimum $E_{Cp\text{-}p}^*$ occurs at 100% I_3^* and 100% I_5^* and its value is only 33.3%, which means that 100% 3rd and 100% 5th order harmonics injection achieves the bus capacitance reduction of 66.7% (the same analysis result is seen in [8]). When ignoring the phase displacement of v_{in} and fundamental component of i_{in}, PF with the 3rd and 5th order harmonics injection can be defined as

$$\text{PF}=\frac{I_{rms}^2}{\sqrt{I_{rms}^2+I_{rms}^2I_3^{*2}+I_{rms}^2I_5^{*2}}}=\frac{1}{\sqrt{1+I_3^{*2}+I_5^{*2}}} \tag{13}$$

In order to ensure PF above the certain requirement such as λ, I_3^* and I_5^* should satisfy

$$I_3^{*2}+I_5^{*2}\le\left(1/\lambda^2-1\right) \tag{14}$$

In Fig.2, the red solid line represents the boundary for PF⩾0.9. In the region for PF⩾0.9, the minimum $E_{Cp\text{-}p}^*$ occurs at 34% I_3^* and 34% I_5^* and its value is down to 57.2%, which means that 34% 3rd and 34% 5th order harmonics injection achieves the maximum bus capacitance reduction of 42.8% considering PF⩾0.9 limit (same analysis result is seen in [7]).

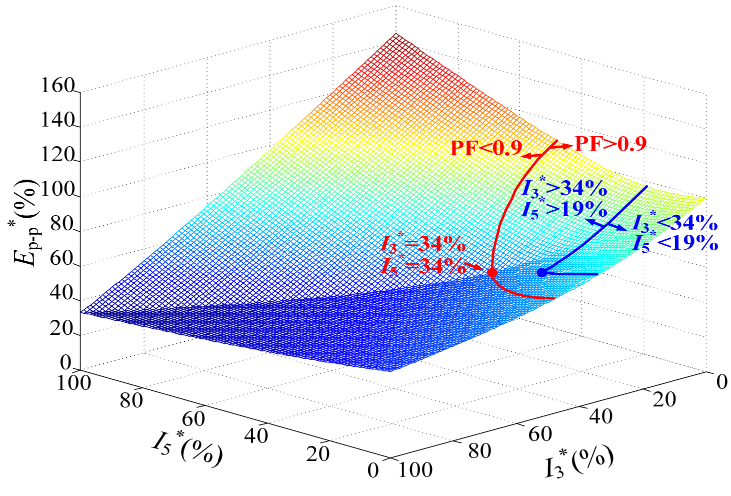


Fig. 2. Three dimensional map of $E_{Cp\text{-}p}^*$, I_3^* and I_5^*

EN61000-3-2 Class D dictates the certain values for the maximum allowable amplitude of each odd harmonics. With the same load, the fundamental component amplitude of i_{in} decreases following the increasing U_{rms}, which means that the allowable ratios are enlarged and the less $E_{Cp\text{-}p}^*$ is obtained with the increasing U_{rms}. Therefore, the value of C is determined by the maximum $E_{Cp\text{-}p}^*$ occurring at the minimum U_{rms} for the wide input range (100~240Vac in this paper). Generally, the more harmonics injection usually introduces the more reactive power, resulting in the higher conduction loss and lower efficiency.

In order to improve the efficiency at high line input, this paper selects the optimum fixed injected ratios at 100Vac input as the *unified* ratio for the wide input range. Table I calculates the allowable ratio of 3rd and 5th order harmonics at 100Vac input, which are respectively 34% and 19%. The blue solid line in Fig.2 represents the boundary condition of I_3^* =34%, I_5^*=19%. The minimum $E_{Cp\text{-}p}^*$ is 63.9%, occurring at 34% I_3^* and 19% I_5^*, meaning 34% 3rd and 19% 5th order injected harmonic can achieve the bus capacitance reduction of 36.1% meeting EN61000-3-2 Class D limits.

TABLE I. EN61000-3-2 CLASS D LIMITS FOR 3RD AND 5TH ORDER HARMONICS AND ALLOWABLE RELATIVE RATIOS AT 100VAC INPUT

Harmonics Order	Allowable Max. Amplitude	Allowable Max. Ratio at 100Vac[a]
3	3.4mA/W, 408mA@120W	34%
5	1.9mA/W, 228mA@120W	19%

[a] The allowable relative ratio is the quotient of the allowable maximum harmonic amplitude and the fundamental amplitude, of input current, which is 10mA/W at 100Vac input.

III. ON-TIME COMPENSATION FOR THE ACCURATE HARMONIC INJECTION

A. *Conventional On-time Control and its Inaccuracy*

In ideal CRM analysis, the inductor current i_L is regarded as in a standard triangle in the switching cycle. Thus i_{in} equals to one half of peak inductor current i_{Lpeak} because the minimum inductor current i_{Lmin} is simplified as 0. i_L in the ideal analysis can be expressed as

$$i_{in}(\omega t) = \frac{1}{2} i_{Lpeak}(\omega t) = \frac{v_{in}(\omega t)}{2L_b} T_{onh}(\omega t) \tag{15}$$

where L_b is the boost inductor and T_{onh} is the on-time for the harmonics injection based on the ideal CRM analysis without considering deviation effect.

Substitution of (4) and (5) into (15) yields

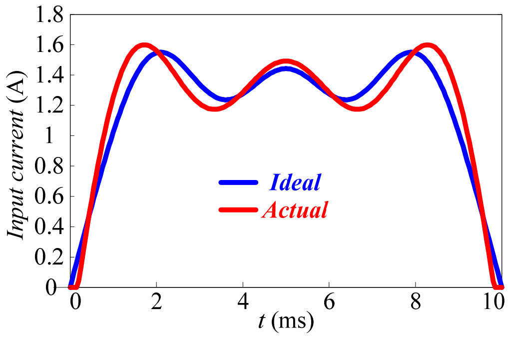
$$T_{onh}(\omega t) = 2L_b \frac{I_{rms}}{U_{rms}} \left(1 + I_3^* \frac{\sin 3\omega t}{\sin \omega t} + I_5^* \frac{\sin 5\omega t}{\sin \omega t}\right) \tag{16}$$

where ($I_3^*\sin 3\omega t/\sin\omega t + I_5^*\sin 5\omega t/\sin\omega t$) controls the injected harmonics current, $2L_bI_{rms}/U_{rms}$ is a constant during the half line cycle because of the narrow bandwidth of PFC stage and can be provided by the voltage regulator adaptively [13].

However, (15) and (16) ignore the practical resonance between the boost inductor and the parasitic capacitances of power devices in CRM operation. The practical resonance is used to achieve zero-voltage or valley turn-on, but meanwhile introduces the negative input current and the delayed switching period, resulting in the practical inductor current deviating from the ideal triangle waveform and the input current deviating from the expectation. The deviation effect results in the undesired injected content of the 3rd and 5th harmonics.

With the conventional on-time control in (16), Fig.3 compares the actual input current waveforms with the ideal ones at 100/ 240Vac inputs assuming I_3^*=34%, I_5^*=19%, output power P_{out}=120W, line frequency f_{line}=50Hz, L_b=175μH, equivalent capacitance C_{eq}=C_{dp}+C_{oss}=130pF, (C_{dp} is the equivalent parallel capacitance of the boost diode and C_{oss} is the output capacitance of the power switch). It is observed that the deviation effect makes the actual input current deviate from the ideal ones.

Furthermore, Fig.4 compares the harmonics content of i_{in} in Fig.3. From Fig.4, it is observed that the deviation effect causes much more 3rd and 5th order harmonics content than EN61000-3-2 Class D limits at 100Vac input. Thus, the conventional control in (16) cannot achieve the accurate harmonics injection.



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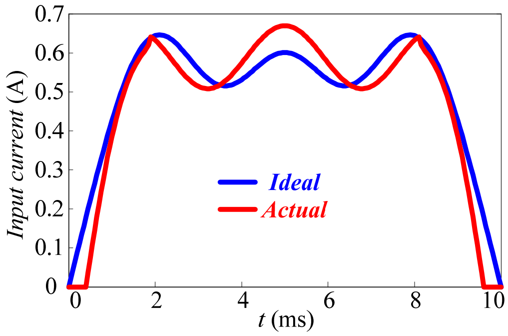

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Fig. 3. Input current waveforms comparison with the conventional on-time control. (a) 100Vac input. (b). 240Vac input.

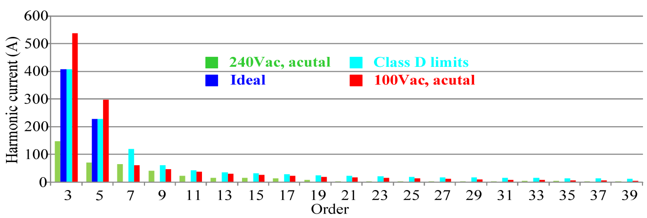


Fig. 4. Comparison of input current harmonics content

B. On-time compensation for accurate harmonic injection

In order to obtain the accurate harmonics injection, this paper adopts a novel on-time compensation considering the influence of the resonance in practical CRM. The same approximation process in [11] is used to calculate i_{Lavg}, that is, considering i_L changes linearly during the most time of the switching period, i_L waveform during one switching cycle is simplified as a triangular shape with negative offset. Then i_{Lavg} approximately equals to the average value of i_{Lpeak} and i_{Lmin} ($i_{Lmin}\neq 0$, which is different with the ideal analysis), that is

$$i_{in}(\omega t)=i_{Lavg}(\omega t)=\frac{1}{2}\left(i_{Lpeak}(\omega t)+i_{L\min}(\omega t)\right) \tag{17}$$

According to the detailed resonance analysis in [12], and ignoring the variation of i_L during the forward resonance interval, i_{Lpeak} and i_{Lmin} are expressed as follows

$$i_{Lpeak}(\omega t)=\begin{cases}\dfrac{v_{in}(\omega t)}{L_b}T_{onhc}(\omega t), v_{in}(\omega t)\geq\dfrac{1}{2}V_o\\ \dfrac{v_{in}(\omega t)}{L_b}T_{onhc}(\omega t)-\sqrt{\dfrac{C_{eq}}{L_b}}\sqrt{V_o(V_o\text{-}2v_{in}(\omega t))}, v_{in}(\omega t)<\dfrac{1}{2}V_o\end{cases} \tag{18}$$

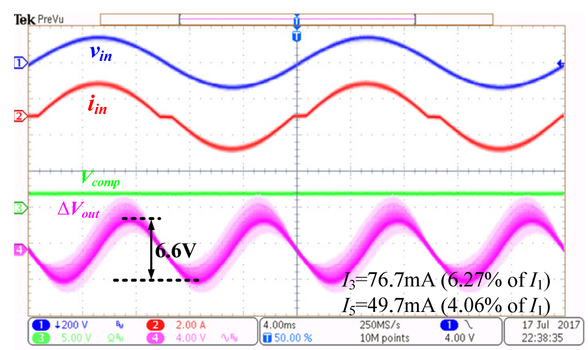
$$i_{L\min}(\omega t)=-\frac{V_o-v_{in}(\omega t)}{\sqrt{L_b/C_{eq}}} \tag{19}$$

where V_o is the output voltage of the PFC converter, T_{onhc} is the on-time for the harmonics injection after compensation.

Substitution of (5), (18), (19) into (17) yields to (20), where ($I_3^*\sin3\omega t/\sin\omega t+I_5^*\sin5\omega t/\sin\omega t$) controls the injected harmonics current, $2L_bI_{rms}/U_{rms}$ is a constant during the half line cycle and is provided by the voltage regulator adaptively [13], and the other items are used to compensate the deviation effect.

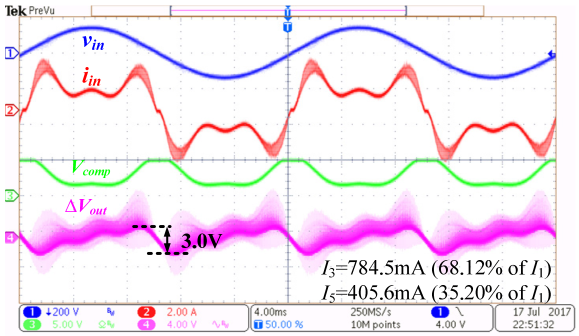
IV. Experimental Verification

In order to verify the optimum harmonic injection to minimize bus capacitance of CRM boost PFC converters within EN61000-3-2 Class D limits, an 120W 100~240Vac/380V CRM boost PFC prototype has been built. TPH3206PS and C3D02060A are selected as the power switch and boost diode, respectively ($C_{eq}=C_{oss}+C_{dp}$=130pF). L_b is selected as 175μH and the output capacitance is selected as 150μF. TMS320F28335 is used as the digital controller and it can calculate the on-time in real-time according to sensed v_{in} and V_o. It is noted that $2L_bI_{rms}/U_{rms}$ in (20) could be provided by the voltage regulator adaptively without additional sensing. Using the same prototype, different control methods are tested and compared, including the constant on-time (COT) control without harmonics injection, the conventional on-time control for harmonic injection (CHOT) and the proposed novel on-time control for harmonic injection (NHOT).



(a)

$$T_{onhc}(\omega t)=\begin{cases}2L_b\dfrac{I_{rms}}{U_{rms}}\left(1+I_3^*\dfrac{\sin3\omega t}{\sin\omega t}+I_5^*\dfrac{\sin5\omega t}{\sin\omega t}\right)+\dfrac{\sqrt{L_bC_{eq}}}{v_{in}(\omega t)}\left(V_o-v_{in}(\omega t)\right), \quad v_{in}(\omega t)\geq\dfrac{1}{2}V_o\\ 2L_b\dfrac{I_{rms}}{U_{rms}}\left(1+I_3^*\dfrac{\sin3\omega t}{\sin\omega t}+I_5^*\dfrac{\sin5\omega t}{\sin\omega t}\right)+\dfrac{\sqrt{L_bC_{eq}}}{v_{in}(\omega t)}\left(V_o-v_{in}(\omega t)+\sqrt{V_o(V_o-2v_{in}(\omega t))}\right) \quad ,v_{in}(\omega t)<\dfrac{1}{2}V_o\end{cases} \tag{20}$$



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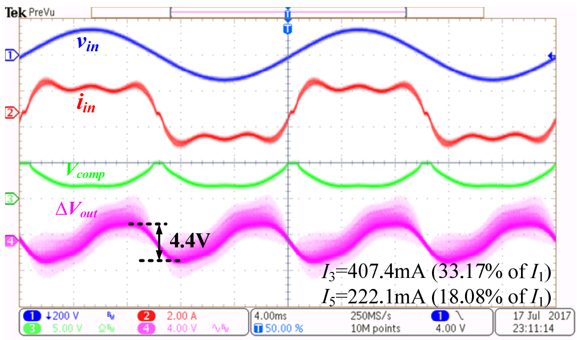

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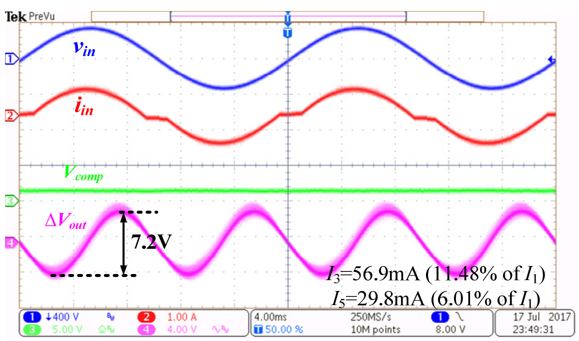
Fig. 5. Measured waveforms comparison with full load at 100Vac input. (a) with COT control. (b) with CHOT control. (c) with NHOT control.



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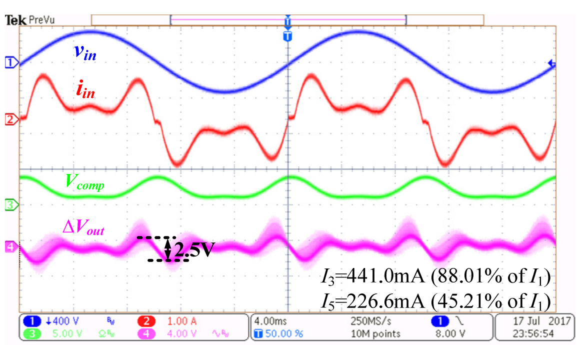

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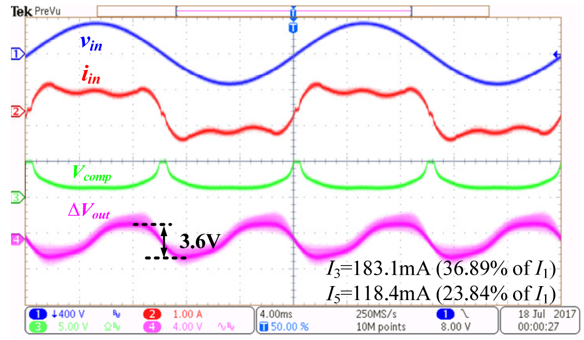

(c)

Fig. 6. Measured waveforms comparison with full load at 240Vac input. (a) with COT control. (b) with CHOT control. (c) with NHOT control.

For CHOT/ NHOT control, the injected ratios of 3rd and 5th order harmonic are 34% and 19%, respectively. For CHOT control, on-time is calculated according to (16). For NHOT control, on-time is calculated according to (20). The measured v_{in}, i_{in}, feedback loop error signal V_{comp} and output voltage ripple ΔV_{out} waveforms at 100Vac and 240Vac inputs are shown in Fig.5 and Fig.6, respectively. V_{comp} proportionately controls the actual on-time during the half line cycle.

Comparing with COT control, CHOT/NHOT control can both reduce output voltage ripple due to 3rd and 5th order injected harmonics. However, CHOT control cannot achieve the accurate harmonics injection and introduces much more content of harmonics content, which exceeds EN61000-3-2 Class D limits. Comparing with CHOT control, NHOT control achieves accurate injected harmonic to meet Class D limits within the wide input range and whole load range.

Table II gives the measured harmonic current with NHOT control at 100Vac input and full load, where the measured harmonics current are the maximum. With NHOT control, the output voltage ripple is reduced from 6.6V to 4.4V (ignoring the switching frequency ripple) at 100Vac input (an output voltage ripple reduction of about 33%), accordingly meaning that a bus capacitance reduction of 33% can be obtained with proposed NHOT control.

TABLE II. MEASURED HARMONIC CONTENT AT 100VAC AND FULL LOAD, WITH NHOT CONTROL

Order	Measured (mA)	Class D Limits (mA)	Order	Measured (mA)	Class D Limits (mA)
3	407	408	23	8.7	20
5	222	228	25	8.2	18.5
7	11.4	120	27	8	17.1
9	7.5	60	29	7.4	15.9
11	8.5	42	31	6.5	14.9
13	7.4	35.5	33	6.2	14
15	8.5	30.8	35	5.5	13.2
17	8.5	27.2	37	4.3	12.5
19	9.4	24.3	39	1.4	11.8
21	8.4	22			

V. CONCLUSIONS

From energy-ripple perspective, this paper discusses the optimum 3rd and 5th order harmonic injection to minimize bus capacitance of CRM boost PFC converters. Within EN61000-3-2 Class D limits, 34% 3rd and 19% 5th order harmonic injection can theoretically achieve the maximum bus capacitance reduction of 36.1% for the wide input range (100~240Vac). However, the conventional control based on the ideal analysis cannot compensate the deviation effect of CRM operation, which introduces exceeding 3rd and 5th order injected harmonics current beyond Class D limits. In order to eliminate deviation effect, a novel on-time compensation method is proposed to realize accurate harmonics injection. The experimental results from an 120W prototype show that the maximum bus capacitance reduction of 33% (or maximum output voltage ripple reduction of 33%) is achieved in practice.

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