A Simple ZVT Auxiliary Circuit for Full-Bridge based Bridgeless Single-Phase PFC with Hybrid PWM Modulation Scheme

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***Abstract*—This paper proposes a zero-voltage-transition (ZVT) technique for the full-bridge based bridgeless single-phase PFC. An auxiliary circuit consists of a small auxiliary inductor and two active switches is placed in parallel with the main filter inductor. The proposed ZVT technique has several advantages over the existing ZVT schemes including low ripple of the filter inductor current, natural zero-current-switching (ZCS) for the auxiliary switches, relatively less additional components and allowing unipolar or hybrid PWM modulation of the full-bridge converter. The effectiveness of the proposed scheme has been validated through hardware experiment. It shows that the proposed ZVT scheme can save approximately 40% of the power loss compared with the regular hard-switching operation.**

Keywords—zero-voltage-transition; soft-switching; bridgeless PFC; single-phase PFC

I. INTRODUCTION

As the current drawn by a grid-connected load increases, the power factor and total harmonic distortion (THD) become important design targets for the equipment. Power factor correction (PFC) has become an essential part in the circuit of the high power grid-connected equipment such as electric vehicle (EV) chargers. Compared with boost based PFC, the bridgeless PFC can achieve higher efficiency because the power loss in the diode bridge can be saved. Increasing the switching frequency helps decrease the volume of the passive filter components, thus increase the power density of the system, especially with wide-bandgap-devices [1]-[3]. Zero-voltage-transition (ZVT) techniques reduce the power loss during the turn-on transitions of switches which helps improve the system efficiency under cases where the switching frequency is high [10]-[21]. Such soft-switching techniques can also reduce the electromagnetic interference (EMI) generated by the converter.

ZVT schemes have been introduced for the full-bridge converter without any additional circuit in [10] and [11]. The drawback of this scheme is the large filter inductor current ripple required to reverse the switching pole current. ZVT schemes with auxiliary circuits have also been introduced for full-bridge converter to realize the zero-voltage-switching (ZVS) turn-on of the main switches. The auxiliary resonant commuted pole (ARCP) ZVT schemes [12] and [13] add two separate auxiliary circuits to the system to achieve ZVS when unipolar PWM modulation is used for full-bridge converter. In this scheme, the dc link capacitor is split into two in order to create a midpoint of the dc voltage. The voltage balancing issue needs to be handled between the two dc link capacitors. The resonant ac-link converters proposed in [19]-[21] have less components in the auxiliary circuit than ARCP converters, however, is only suitable for bipolar PWM modulation which requires larger grid-side filter. There are other types of ZVT auxiliary circuit for full-bridge converter including triangular resonant snubber based circuit in [14] and [15], and coupled inductor based circuit in [16]-[18]. Although the mechanism of these ZVT auxiliary circuits are similar, the exact configuration in terms of where the auxiliary circuit is connected to the main circuit are different which result different overall performance of the system.

In this paper, a simple ZVT auxiliary circuit is proposed for the full-bridge based single-phase PFC. The auxiliary circuit which consists of a small auxiliary inductor and two active switches are connected across the grid-side filter inductor in the main circuit. The ZVT scheme allows hybrid PWM modulation [22] which reduces the requirement for the grid-side filter. The effectiveness of the proposed scheme is validated through hardware experiment. The circuit operation is described in Section II. The control structure of the system is given in Section III. The hardware experiment results of the proposed circuit and the conclusion of this paper are given in Section IV and V.

II. PROPOSED CIRCUIT AND CIRCUIT OPERATION

The full-bridge based single-phase PFC with the proposed ZVT auxiliary circuit is shown in Fig. 1. Hybrid PWM modulation scheme is used where Q_1 and Q_2 are the high frequency leg. A LCL-filter is used for the grid current ripple attenuation. The ZVT auxiliary circuit is connected across the filter inductor L so that it can be used to inject current to the switching pole A. The auxiliary inductor L_{aux} has a very small inductance value. By proper operating the circuit, ZVS turn-on can be achieved for Q_1 and Q_2 to improve the system efficiency while keep the same grid current quality.

In the positive half cycle of the line period, Q_3 is constantly off and Q_4 is constantly on. The filter inductor current i_L flows into switching pole A which causes natural ZVS turn-on for switch Q_1. By switching S_2 in a proper manner, the ZVS turn-on for Q_2 can also be achieved. The timing diagram of the actions of all the switches is illustrated for the positive half cycle of the

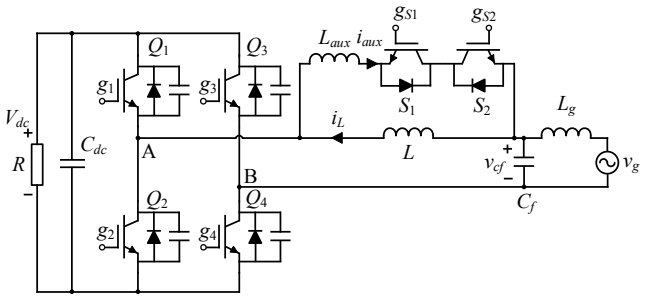

Fig.1 Proposed ZVT circuit for full-bridge based bridgeless PFC

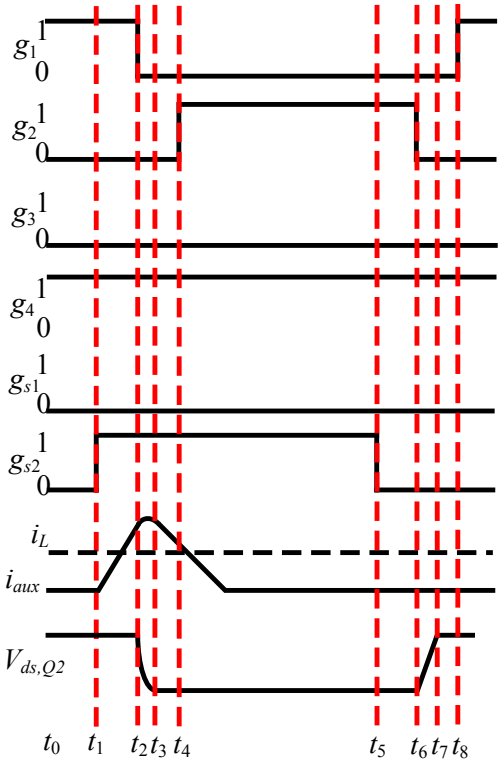

Fig.2 Timing diagram for the circuit operation

line period in Fig. 2. The corresponding commutation states are illustrated in Fig. 3. The description of each commutation state is given as following:

[t_0~t_1]: Q_1 is on and Q_2 is off. Before the ZVS branch is turned on, the main inductor current is flowing through the channel of Q_1 and Q_4.

[t_1~t_2]: The auxiliary branch is activated by turning on S_2. The auxiliary inductor is charged by the voltage V_{dc}–V_{Cf}. By the end of this period, the auxiliary branch current becomes higher than the main inductor current so that the current at point A is reversed.

[t_2~t_3]: This states and the flowing states happen during the deadtime where g_1 and g_2 are both set as low. After g_1 is set low, the auxiliary inductor starts to resonate with the drain-to-source capacitance of Q_1 and Q_2 until $V_{ds,Q2}$ reaches zero. The change of the filter inductor current can be neglected due to the relatively large inductance.

[t_3~t_4]: The current starts to flow through the body diode of Q_2 since $V_{ds,Q2}$ has reached zero. The auxiliary inductor starts to be discharged by $-V_{Cf}$. Q_2 can be ZVS turned on before the auxiliary inductor current drops lower than i_L.

[t_4~t_5]: Q_2 is ZVS turned on and the current flows through the channel of Q_2. i_{aux} continues to decrease until it reaches zero and is blocked by the body diode of S_1. S_2 is turned off at the end of this period.

[t_5~t_6]: During the rest of the duty cycle of Q_2, Q_2 is on and Q_1 is off.

[t_6~t_7]: Q_2 is turned off. The filter inductor current starts to discharge and charge the drain-to-source capacitance of Q_1 and Q_2 respectively until $V_{ds,Q1}$ reaches zero.

[t_7~t_8]: The filter inductor current flows through the body diode of Q_1 so that it can be ZVS turned on at the end of deadtime.

As can be seen from the circuit operation, the ZVS turn-on is achieved for Q_2 by reversing the switching pole current before the switch is turned on. Both turn-on and turn-off of the auxiliary switch S_2 are ZCS, thus the switching loss in the auxiliary branch is low. The auxiliary circuit is used to achieve the ZVS turn-on of Q_1 in the negative half cycle of the line period. The circuit operation is similar to what has been described except that auxiliary switch S_1 will be switching instead of S_2.

It is worth noticing that i_{aux} has to be larger than i_L at t_4 and drop to zero before t_5. This is ensured by carefully define the length of [t_1~t_2] and [t_5~t_6]. During the positive half cycle, the charging and discharging voltages of the auxiliary inductor are V_{dc}–V_{Cf} and $-V_{Cf}$ respectively. Similarly, these two voltages become $-(V_{dc}+V_{Cf})$ and $-V_{Cf}$ for the negative half cycle. To maximize the time given for discharging the auxiliary inductor which is [t_4~t_5], the length of [t_5~t_6] needs to be minimized. The peak value of the auxiliary inductor current is controlled by the charging time [t_1~t_2]. It needs to be high enough so that i_{aux} will still be larger than i_L at t_4. It cannot be too high in case the auxiliary inductor is not able to be fully discharged before t_5. There are other disadvantages of having high auxiliary inductor current or long charging time [t_1~t_2] including high power loss in the auxiliary branch and significant impact on the grid side current control.

III. CONTROL STRUCTURE OF THE SYSTEM

The control structure of the system with the proposed ZVT auxiliary circuit is shown in Fig. 4. A PLL is used to generate the phase angle of the grid voltage and is used to calculate the grid current reference. The grid current is regulated in closed-loop by a PI controller and several proportional-resonant (PR) controllers. The first harmonic PR controller is used to ensure zero error tracking of the sinusoidal current reference. The second harmonic PR controller is added to the loop so that the double frequency ripple in the dc-link voltage doesn't affect the grid side current. It has been found that ZVT branch can inject some low frequency harmonics to the main circuit. Thus two extra PR controllers are added to the system to suppress third

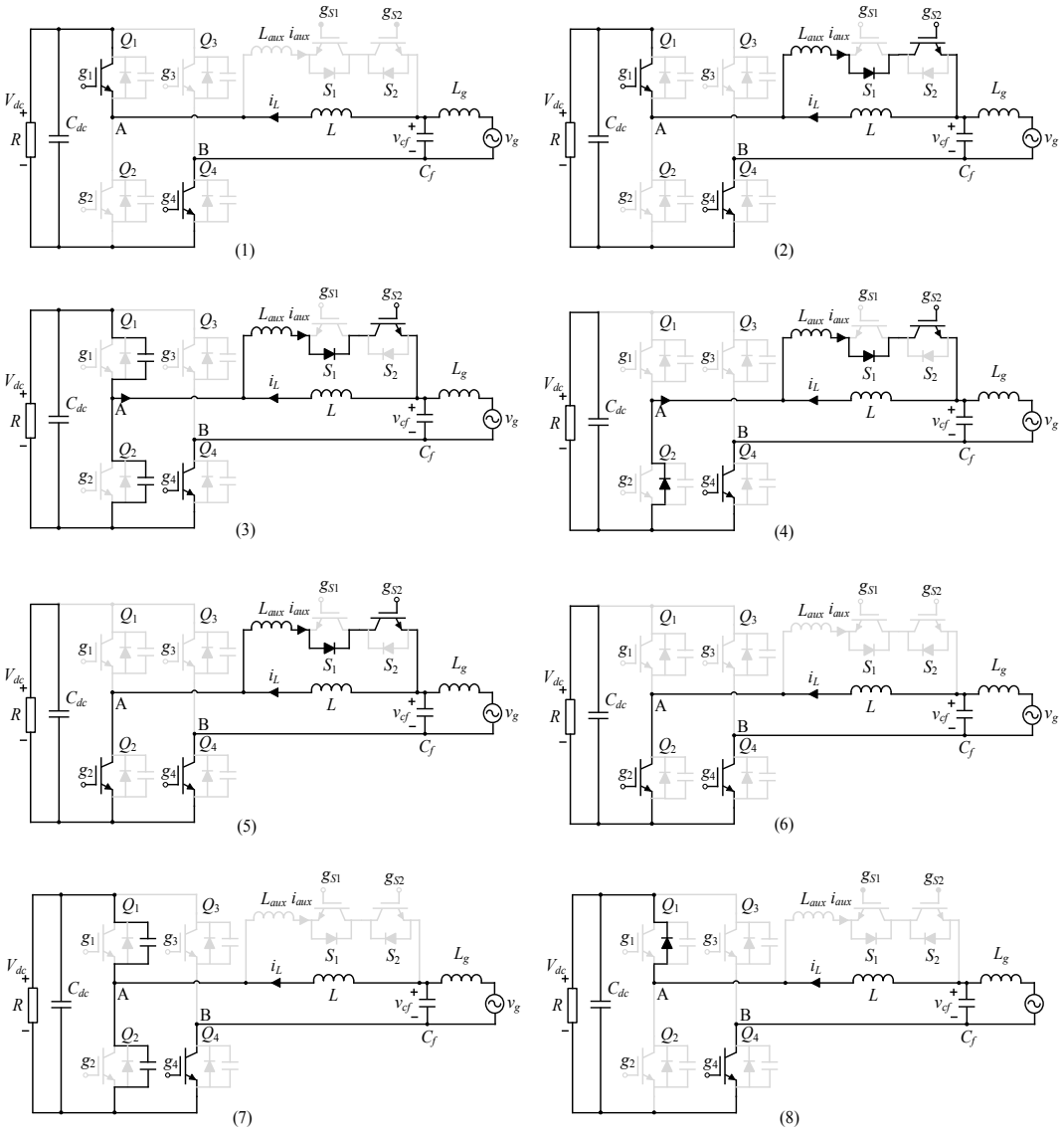

Fig.3 Commutation states of the circuit

and fifth harmonic components in the grid current in order to achieve low THD. A feedforward of sinusoidal duty with the designed modulation index is added into the duty to improve the system response speed. The gate pulses for the mains switches are generated based on hybrid PWM modulation scheme. Deadtime is also added to the gate pulses between two complementary switches. The gate pulses for the auxiliary switches are generated based on the duty of the main switches and the phase angle of the grid voltage.

As mentioned in Section II, the charging voltage for the auxiliary inductor varies as the grid voltage varies in line frequency. The charging voltage waveform in a line period is plotted in Fig. 5. The goal is to charge the auxiliary inductor until the current becomes larger than the main filter inductor current so that the current at the switching pole is reversed. Thus the charging time of the auxiliary inductor namely the length of interval [t_1~t_2] can be calculated as following:

$$T_a = t_2 - t_1 = \frac{k_1\left|\cos(\theta)\right| + k_2}{1 - m\left|\cos(\theta)\right|} - k_3 \tag{1}$$

where m is the modulation index, k_1, k_2 and k_3 are the parameters that can be determined by the specific system specifications and parameters. k_1 is determined by the magnitude of the main filter inductor current. k_2 is determined by the magnitude of the reverse current needs to be injected to the switching pole, that is i_{aux}–i_L. This value depends on the deadtime of the main switches in the actual hardware implementation and switch parasitic capacitance and auxiliary inductor value. Thus the value of k_2 is tuned in the hardware experiment. k_3 is added into the charging time calculation in order to compensate the turn-on delay of the auxiliary switch and the delay introduced by the gate driver. The waveform of the charging time given m=0.8, k_1=k_2=1, k_3=0 is plotted in Fig. 5.

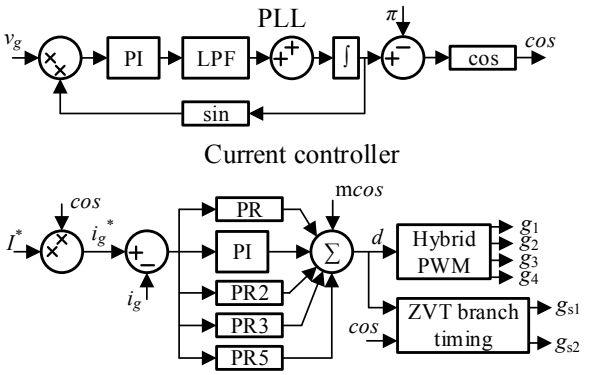

Fig.4 Control structure of the system

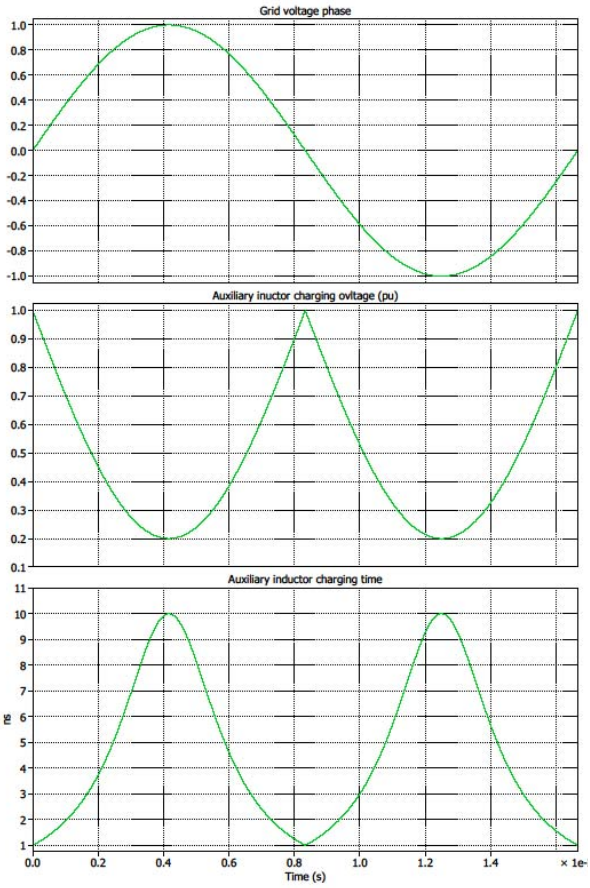

Fig.5 Adaptive charging time for the auxiliary inductor

IV. HARDWARE IMPLEMENTATION AND EXPERIMENT RESULT

The proposed ZVT technique has been validated through hardware experiment. The SiC MOSFET C2M0080120D from CREE is used for the main and auxiliary switches. A SiC schottly diode is placed in parallel with each of the switches in order to reduce the diode recovery loss. Ferrite core with Litz

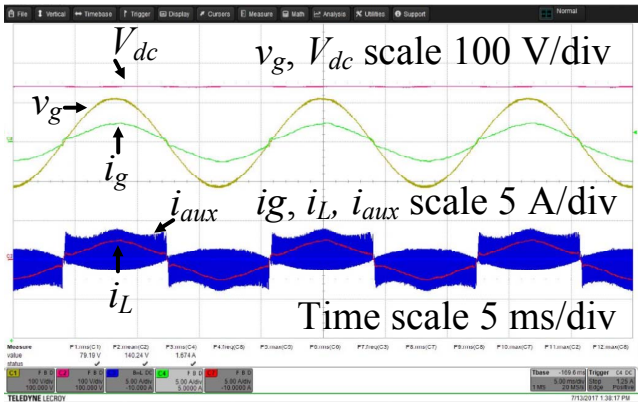

Fig.6 Fundamental PFC waveforms

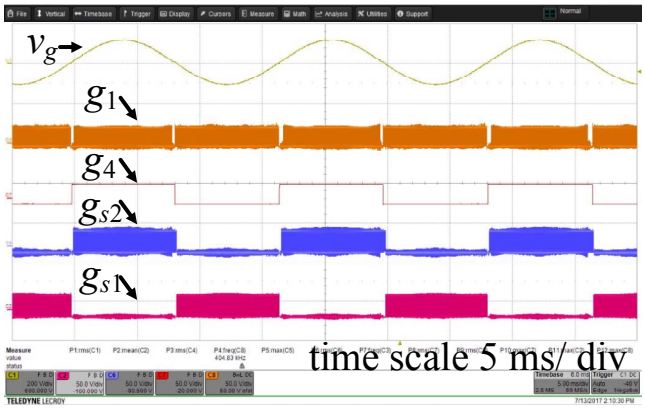

Fig.7 Gate signals for the main switches and auxiliary switches

wire is used for the main filter inductor. The experiment specifications are listed in Table I. The switching frequency used in the experiment is 400 kHz. The deadtime for the main switches is set to 180 ns. TI TMS320F28335 DSP is used for implementing the real-time control of the circuit. The timing used for turning on the auxiliary switch (S_1 or S_2) corresponding to the grid voltage angle is given as following:

TABLE I. HARDWARE IMPLEMENTATION SPECIFICATIONS

AC input voltage (V_g)	80 V
DC output voltage (V_o)	140 V
AC input current (I_g)	1.67 A
DC-link capacitor (C_{dc})	1800 uF
Filter inductor (L)	220 uH
Filter inductor (L_g)	22 uH
Filter capacitor (C_f)	200 nF
Auxiliary inductor (L_{aux})	200 nH
Switching frequency	400 kHz

$$T_a = t_2 - t_1 = \frac{40\left|\cos(\theta)\right| + 37}{1 - 0.8\left|\cos(\theta)\right|} - 146\,(ns) \tag{2}$$

Fig. 6 shows the grid voltage, grid current, dc-link voltage, main filter inductor current and auxiliary inductor current. The grid current THD is 5%. As can be seen from the waveform, the

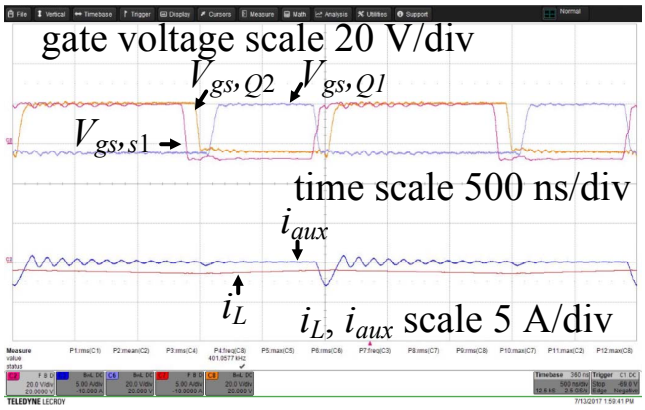

Fig.8 Timing waveform of the main switches and auxiliary switches

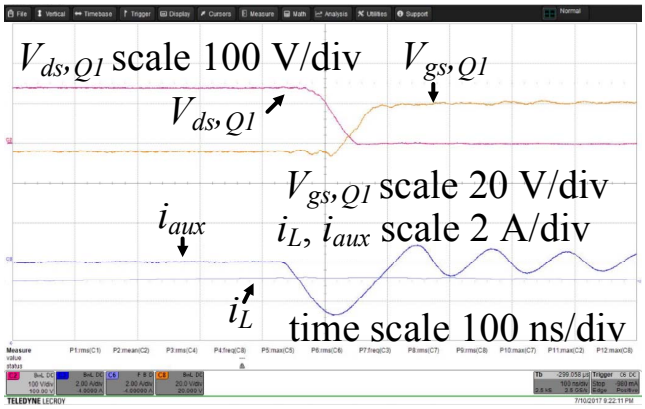

Fig.9 ZVS turn-on transition of the main switch Q_1 during negative half cycle

auxiliary inductor current is suppressed around zero crossing by the adaptive charging time despite of the highest charging voltage. The gate voltage of two of the main switches (Q_1 and Q_3) and the auxiliary switches are shown in Fig. 7 along with the grid voltage. It shows the hybrid PWM modulation waveform and the corresponding active auxiliary switch for each of the half cycle in a line period. The switching cycle level waveform in the negative half cycle including the gate voltage of Q_1 and Q_2, the active auxiliary switch S_1, i_L and i_{aux} are given in Fig. 8. It shows a good match with circuit operation illustrated in Fig. 2. The drain-to-source voltage of the target main switch Q_1 during the turn-on transition is shown in Fig. 9. It shows that the drain-to-source voltage drops to zero before the switch is turned on, thus the ZVS turn-on is achieved. The overall efficiency of the converter is measured by YOKOGAWA WT3000 power analyzer. The overall efficiency of the circuit with traditional hard-switching operation is 95.53% at the specification given in Table I. With the proposed ZVT scheme, the overall efficiency of the system is increased to 97.36%. The overall loss is reduced to 60% of the hard-switching operation of the full-bridge PFC by using the proposed ZVT scheme.

V. CONCLUSIONS

A ZVT technique for the full-bridge based single-phase PFC which supports hybrid PWM modulation is proposed in this paper. A simple auxiliary circuit is placed across the filter inductor so that it can discharge the main switch drain-to-source capacitance during turn-on transitions to realize ZVS turn-on. The switching loss at the auxiliary switches is low since both the turn-on and turn-off are ZCS. The proposed ZVT technique has been validated through experimental result. Compared with traditional hard-switching operation of the circuit, the overall loss is reduced by 40% by applying the proposed scheme.

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