Primary-Side Feedback Control IC Design for Flyback Converter with Energy Saving Burst Mode

Chun-Yu Huang
Department of Electrical Engineering
Tainan, Taiwan

Tsorng-Juu Liang, *Fellow, IEEE*
Advanced Optoelectronic Technology Center (AOTC)/Green Energy Electronics Research Center (GREERC) National Cheng Kung University
Tainan, Taiwan
Email: tjliang@mail.ncku.edu.tw

Kai-Hui Chen
Department of Electrical Engineering
Tainan, Taiwan

Cheng-Yuan Li
Department of Electrical Engineering
Tainan, Taiwan

***Abstract*—The advantages of the flyback converter with the primary-side regulation (PSR) are small size and high efficiency at light load. However, when the PSR flyback converter operates in burst mode, the controller is not able to sense the output information. Therefore, it is not easy to control the output voltage precisely. An integrated circuit design for AC-DC flyback converter using primary-side controller with burst mode energy saving is proposed in this paper. As the load decreases, the flyback converter operates from discontinuous conduction mode to frequency reduction mode. At extremely light load, the flyback converter operates in burst mode. With the proposed control, the burst-on time is detected by the voltage across the auxiliary winding, and the burst-off time can be estimated to control the output voltage ripple. In the proposed control circuit, a capacitor is charged by a constant current source during the burst-on time, and the capacitor voltage is transferred to a controlled current. Therefore, the required burst-off time can be obtained by using the controlled current to charge another capacitor until it reaches the reference voltage. Finally, this controller is fabricated with TSMC 0.25 µm CMOS high voltage mixed signal general purpose process. The flyback converter with the input voltage range of 90-130 V_{rms}, the output voltage of 15 V, and the output power of 30 W is implemented to verify the feasibility of the proposed controller.**

***Index Terms*—Flyback converter, Primary-side regulation, Burst mode.**

I. Introduction

There are more and more portable electronic devices such as notebooks, digital cameras and smart phones in people's life. Therefore, the power consumption of the battery chargers on these devices increases rapidly. Generally, the battery charger operates in standby mode or no-load mode at most of the time. How to save the power in standby mode becomes an important issue in many countries. To overcome the challenge of strict standards, the novel technologies should be found to increase the efficiency of the battery charger. It can be achieved by employing frequency reduction to reduce the power consumption in light load, and it can use burst mode in standby mode [1]-[4].

In the battery charger, the single-stage flyback converter is widely used due to its electrical isolation and simple structure. Conventionally, an optocoupler and secondary-side circuits are used to feedback the output voltage. With the secondary-side regulation, the output voltage can be regulated precisely [5]-[9]. However, it suffers from larger amount of components, higher cost, and higher power consumption on the feedback circuit and optocoupler, especially at light load. Confronting the stringent standards, the flyback converter with secondary-side regulation is not suitable because of the higher power consumption at light load.

Fig. 1 shows the flyback converter with the primary-side control. Compared with the secondary-side regulation, the secondary-side feedback circuit and optocoupler are removed. In the flyback converter with the primary-side regulation, the output voltage is sampled by the auxiliary winding during the conduction time of the secondary-side diode. Therefore, the output voltage feedback can be achieved [10]-[15].

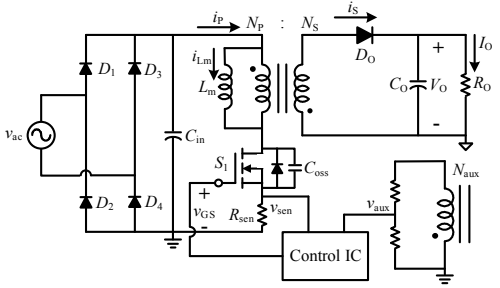


Fig. 1 Flyback converter with primary-side control

However, the information of output voltage and output current cannot be obtained by the controller, when the flyback converter operates in the burst-off time. Therefore, the output voltage ripple cannot be controlled. This paper proposes a circuit to determine the burst-on time and burst-off time to control the output voltage ripple in burst mode.

II. Fundamental Concepts of Flyback Converter and Burst Mode Methods

Typically, there are two control methods of burst mode, one is the constant burst-on time, and the other is the constant burst mode frequency [16]-[19]. Fig. 2 shows the waveforms of the gate signal according to load variations with the constant

burst-on time. However, the variable burst mode frequency can create an audible noise at very light load. To solve the audible noise problem by variable burst mode frequency at very light load, maintaining the constant burst mode frequency can prevent the audible noise.

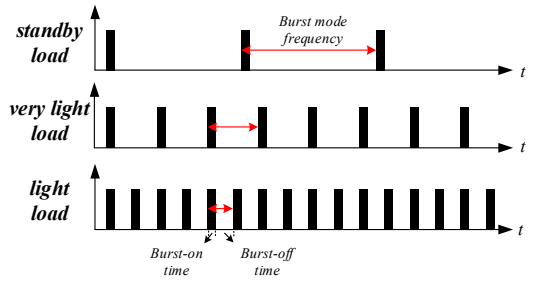


Fig. 2 Waveforms of gate signal according to load variations with constant burst-on time

The waveforms of the gate signal according to load variations with the constant burst mode frequency are shown in Fig. 3. Using the constant burst mode frequency control method can avoid the audible noise by designing the burst mode frequency which is far away the frequency of the most sensitive to human ears.

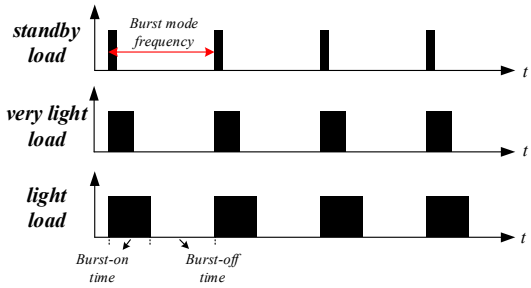


Fig. 3 Waveforms of gate signal according to load variations with constant burst mode frequency

The schematic of the flyback converter with primary-side regulation scheme and the key waveforms of the flyback converter at DCM operation are shown in Fig. 4 and Fig. 5, respectively. As shown in Fig. 4 and Fig. 5, the following equations describe the estimation of the output voltage and current by auxiliary winding.

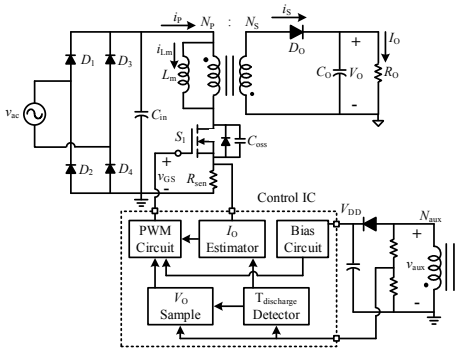


Fig. 4 Flyback converter with primary-side regulation

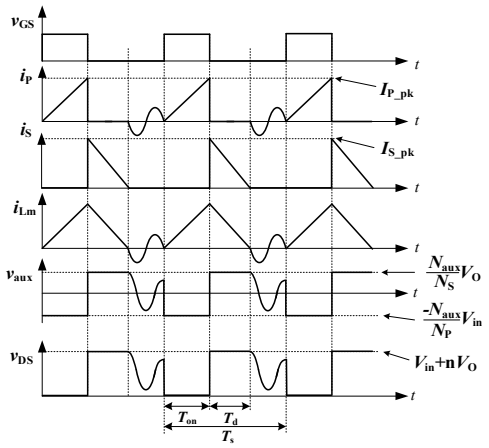


Fig. 5 Waveforms of flyback converter at DCM operation

When the power switch S_1 is turned off, the diode D_O is conducted, and the energy stored in L_m transfers to the output through the transformer windings. During this period, the auxiliary winding voltage v_{aux} is proportional to the output voltage V_O.

$$v_{aux} = \frac{N_{aux}}{N_S} \cdot V_O \tag{1}$$

The peak current of secondary-side winding I_{S_pk} is n times of the peak current of primary-side winding I_{P_pk}, where n is primary to secondary turn ratio N_P/N_S, and the equation is expressed in Eq. (2).

$$I_{S\_pk} = n \cdot I_{P\_pk} \tag{2}$$

The average current of secondary-side winding I_{S_ave} can be expressed in Eq. (3), where T_d is the conduction time of the secondary-side diode D_O and T_s is the switching period.

$$I_{S\_ave} = \frac{1}{2} \cdot I_{S\_pk} \cdot T_d \cdot \frac{1}{T_s} \tag{3}$$

Based on the amp-second balance of the output capacitor C_O, the output current I_O is equal to the average current of secondary-side winding I_{S_ave}. Then,

$$I_O = I_{S\_ave} = \frac{1}{2} \cdot n \cdot I_{P\_pk} \cdot T_d \cdot \frac{1}{T_s} \tag{4}$$

From Eq. (4), the output current I_O can be estimated from the peak current of primary-side winding I_{P_pk} and the conduction time of the secondary-side diode T_d.

III. Fundamental Concepts of the Proposed Control and Function Blocks

In this paper, the flyback converter operates in DCM at heavy load. In order to reduce the switching loss at light load, the frequency reduction mode is used. As the on-time of the power switch decreases to the limitation, the flyback converter enters to frequency reduction mode at light load. When the switching frequency drops to the minimum, the flyback converter will be operated in burst mode at very light load conditions. The modes of operation is shown in Fig. 6.

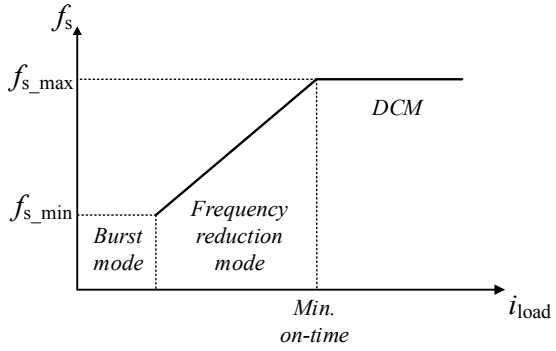


Fig. 6 Modes of operation

The output voltage according to load variations with proposed burst mode control and zoom-in waveforms of the output voltage in one burst mode cycle are shown in Fig. 7 and Fig. 8, respectively. In burst-on time, the output voltage increases until reaching to maximum output voltage. The auxiliary winding voltage is compared with a reference voltage, and the burst-on time is ended when v_{aux} reaches the reference voltage. However, there is no output information in burst-off time. To determine the burst-off time, the relationship between the burst-on time and the burst-off time is needed to proof.

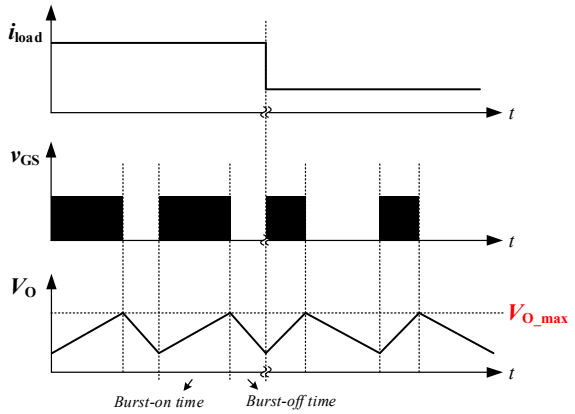


Fig. 7 Output voltage according to load variations with proposed burst mode control

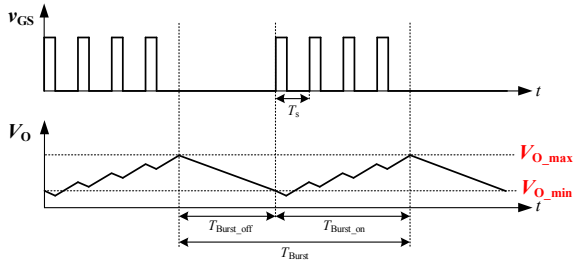


Fig. 8 Zoom-in waveforms of output voltage in one burst mode cycle

Based on the law of charge conservation, the total charges on the secondary-side diode are equal to that delivering to the load and stored on the output capacitor. The equation is expressed in Eq. (5), where Q is the charges from the primary-side to the secondary-side and n_{Burst} is the number of turning on the power switch in the burst-on time.

$$Q \cdot n_{Burst} = I_O \cdot T_{Burst\_on} + (V_{O\_max} - V_{O\_min}) \cdot C_O \quad (5)$$

Since there are constant duty and constant frequency in burst-on time, n_{Burst} can be expressed in Eq. (6), where T_s is a switching cycle in the burst-on time.

$$n_{Burst} = \frac{T_{Burst\_on}}{T_s} \quad (6)$$

As shown in Fig. 8, the slope of the output voltage in burst-on time is expressed in Eq. (7).

$$S_{Burst\_on} = \frac{V_{O\_max} - V_{O\_min}}{T_{Burst\_on}} \quad (7)$$

Combining Eq. (5) and Eq. (7), the slope of the output voltage in burst-on time can be derived as:

$$S_{Burst\_on} = \frac{Q}{T_s \cdot C_O} - \frac{V_O}{R_O \cdot C_O} \quad (8)$$

Eq. (8) illustrates that if R_O increases which also means the load decreases, the slope of the output voltage in burst-on time S_{Burst_on} increases.

In burst-off time, all the energy on the load is received by the output capacitor. It can be seen the RC discharging circuit. Then,

$$V_{O\_min} = V_{O\_max} \cdot e^{-\frac{T_{Burst\_off}}{R_O \cdot C_O}} \quad (9)$$

By Using the Taylor's Formula, Eq. (9) can be rewritten in Eq. (10).

$$V_{O\_min} \approx V_{O\_max} \cdot (1 - \frac{T_{Burst\_off}}{R_O \cdot C_O}) \quad (10)$$

As shown in Fig. 8, the absolute value of output voltage slope in burst-off time is expressed in Eq. (11).

$$S_{Burst\_off} = \frac{V_{O\_max} - V_{O\_min}}{T_{Burst\_off}} \quad (11)$$

Combining Eq. (10) and Eq. (11), the slope of the output voltage in burst-off time can be derived as:

$$S_{Burst\_off} = \frac{V_{O\_max}}{R_O \cdot C_O} \quad (12)$$

Eq. (12) demonstrates that if R_O increases, the slope of the output voltage in burst-off time S_{Burst_off} decreases. Hence, the burst-off time T_{Burst_off} increases with increasing R_O. Therefore, this relationship is used to determine T_{Burst_off} by the proposed controller.

Fig. 9 shows the system diagram of the primary-side regulation flyback converter with the proposed burst mode circuit. It is composed of diode conduction period detector, I_O estimator, burst-on time and burst-off time detector, mode

detector (Normal mode/Burst mode), oscillator, V_O sample, PWM and compensation, and HV buffer.

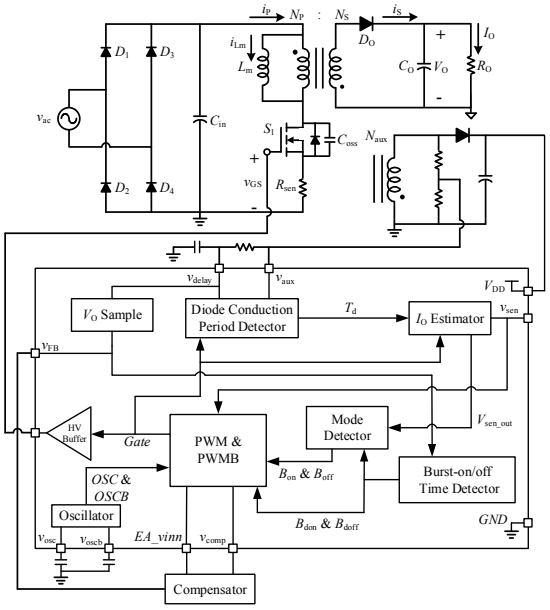


Fig. 9 Flyback converter with the proposed controller

(a) Diode conduction period detector

Fig. 10 and Fig. 11 show the circuit diagram and the waveforms in DCM operation of diode conduction period detector [20]-[21].

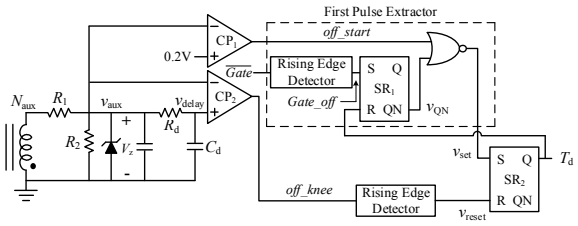


Fig. 10 Diode conduction period detector circuit

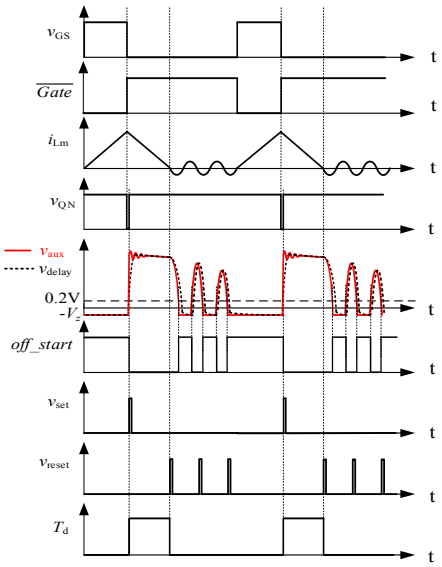


Fig. 11 Waveforms of diode conduction period detector.

When the power switch S_1 is turned off, the SR_1 is set by the inverse gate signal $\overline{Gate}$, and the secondary-side diode also starts to conduct. Therefore, the polarity of auxiliary winding is reversed. After the voltage v_{aux} exceeds 0.2 V, the output of CP_1 will be pulled low. Then, the signal T_d will change level from low to high. The output signal *off_knee* of CP_2 is change to high level, when v_{delay} is greater than v_{aux} by the half of comparator hysteresis. The signal *off_knee* triggers rising edge detector, and the rising edge detector outputs a pulse signal v_{reset} to reset SR_2. Therefore, T_d will change level from high to low. Because the magnetizing inductor L_m and output capacitor of power switch S_1 C_{oss} resonate after the secondary-side current i_S decreases to zero, the voltage v_{aux} may higher than 0.2 V more than one time. Therefore, the first pulse extractor is added to ensure that the output signal of SR_2 is set to high level only one time in a switching cycle.

(b) *Io* estimator

Fig. 12 and Fig. 13 illustrate the circuit diagram and theoretical waveforms of the output current I_O estimator.

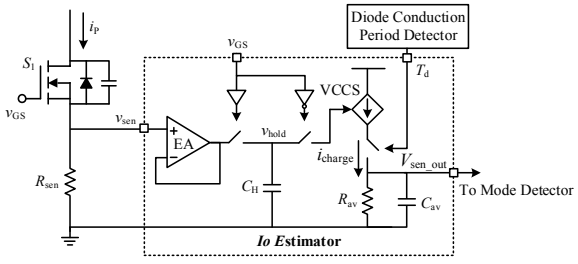


Fig. 12 Circuit diagram of the output current I_O estimator

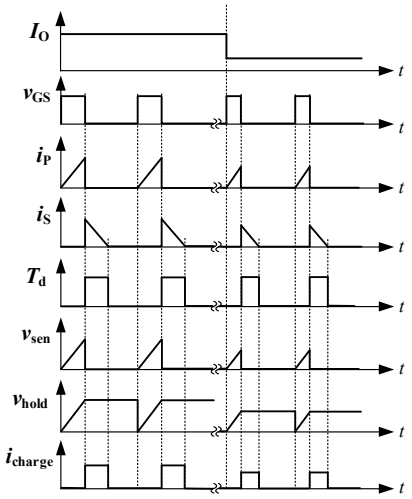


Fig. 13 Waveforms of the output current I_O estimator

The primary-side current i_p is obtained from the current sense resistor R_{sen}, which I_{P_pk} is held as V_{hold} with sample and hold circuit.

$$v_{sen} = R_{sen} \cdot i_P \tag{13}$$

$$v_{hold} = R_{sen} \cdot I_{P\_pk} \tag{14}$$

The voltage v_{hold} is converted to a current I_{charge} by the voltage controlled current source (VCCS) with transconductance K_{VI}. From Eq. (14), the equation of the current I_{charge} can be expressed in Eq. (15).

$$I_{charge} = K_{VI} \cdot R_{sen} \cdot I_{P\_pk} \tag{15}$$

The average current I_{charge_av} of I_{charge} in a switching cycle T_s is expressed in Eq. (16), and f_s is the switching frequency.

$$I_{charge\_av} = K_{VI} \cdot R_{sen} \cdot I_{P\_pk} \cdot T_d \cdot f_s \tag{16}$$

Based on the amp-second balance of C_{av}, V_{sen_out} is equal to the I_{charge_av} multiplied by R_{av}. The voltage V_{sen_out} can be derived in Eq. (17).

$$V_{sen\_out} = I_{charge\_av} \cdot R_{av} = \frac{2}{n} \cdot K_{VI} \cdot R_{sen} \cdot I_O \cdot R_{av} \tag{17}$$

Eq. (17) shows that V_{sen_out} is proportional to I_O, so the load information can be known from V_{sen_out}.

(c) V_O sample

The auxiliary winding voltage v_{aux} is reflected from the secondary-side output voltage V_O during the secondary-side diode conduction period. The V_O sample circuit and waveforms are shown in Fig. 14 and Fig. 15. Because the secondary-side diode is connected between the output load and transformer, there is a voltage drop at the auxiliary winding voltage v_{aux}. In order to reduce the sensing error, the auxiliary winding voltage v_{aux} is sampled when the secondary-side diode current i_S decreases to zero.

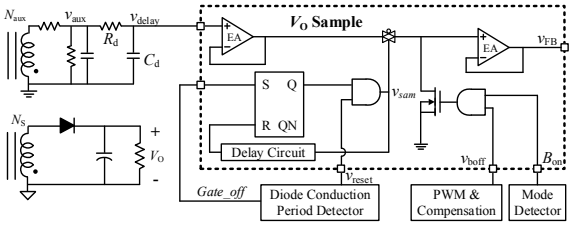


Fig. 14 Schematic of V_O sample circuit

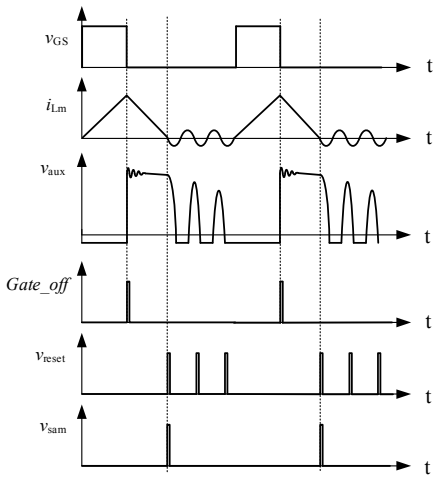


Fig. 15 Waveforms of V_O sample circuit

(d) Burst-on/off time detector

Fig. 16 shows the burst-on time detector circuit. The output voltage feedback v_{FB} increases slowly when the controller operates in the burst-on time. When the voltage v_{FB} is greater than the voltage V_{ref} by a half of comparator hysteresis, the output signal of comparator changes state to high level to generate a pulse signal B_{doff}. Therefore, the controller changes to burst-off time by the signal B_{doff}.

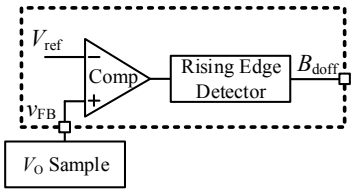


Fig. 16 Schematic of burst-on time detector circuit

The burst-off time detector circuit diagram and waveforms are shown in Fig. 17 and Fig. 18, respectively. When the controller operates in the burst-on time, the voltage v_{boff} is at low level. The capacitor C_x is charged by a current source $I_{charge1}$, and the voltage v_{Cx} increases linearly until the voltage v_{boff} changes state from low to high. The maximum voltage v_{Cx_max} of the capacitor C_x can be expressed in Eq. (18).

$$v_{Cx\_max} = \frac{I_{charge1} \cdot T_{Burst\_on}}{C_x} \tag{18}$$

Then, the voltage v_{Cx_max} converts to a current $I_{charge2}$ by the voltage controlled current source (VCCS) with transconductance K_{VI} to charge C_y, when v_{bon} is at low level. The current $I_{charge2}$ can be expressed as:

$$I_{charge2} = \frac{K_{VI} \cdot I_{charge1} \cdot T_{Burst\_on}}{C_x} \quad (19)$$

The voltage v_{Cy} increases linearly after it is higher than V_{ref}. Based on the law of charge conservation, the charge on the capacitor C_y is received by the current $I_{charge2}$. Then,

$$I_{charge2} \cdot T_{Burst\_off} = C_y \cdot V_{ref} \quad (20)$$

Combining Eq. (19) and Eq. (20), the burst-off time T_{Burst_off} can be derived in Eq. (21).

$$T_{Burst\_off} = \frac{C_x \cdot C_y \cdot V_{ref}}{K_{VI} \cdot I_{charge1} \cdot T_{Burst\_on}} \quad (21)$$

From Fig. 18, if the load decreases, the burst-on time will be shorter and the burst-off time detector circuit will make the burst-off time be longer.

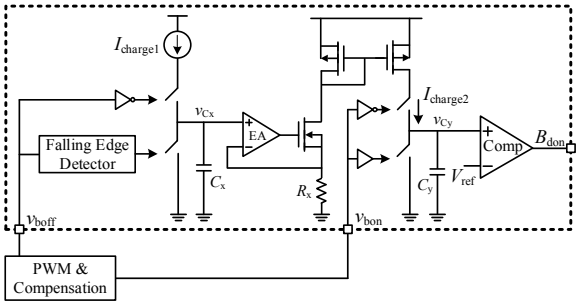


Fig. 17 Burst-off time detector circuit diagram

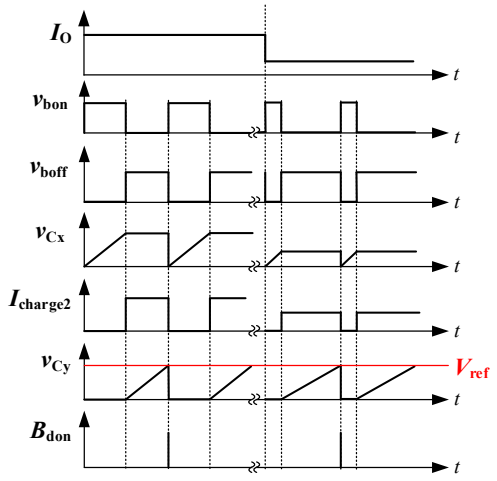


Fig. 18 Waveforms of burst-off time detector circuit

(e) Mode detector

Fig. 19 shows the mode detector circuit diagram. With I_O estimator circuit, when the output current I_O decreases, the voltage V_{sen_out} decreases either. After the voltage V_{sen_out} is lower than reference voltage V_{ref1} by a half of comparator CP_1 hysteresis, the SR latch SR_2 is set and output signal B_{on} changes state from low to high to operate in burst mode. With burst-off time detector circuit, when the load increases, the burst-on time increases. Therefore, after the charging time of capacitor C_x is so long that the voltage V_{Cx} is higher than the reference voltage V_{ref2} by a half of comparator CP_2 hysteresis, the SR latch SR_2 is reset and the signal B_{off} changes to high level to operate at normal mode.

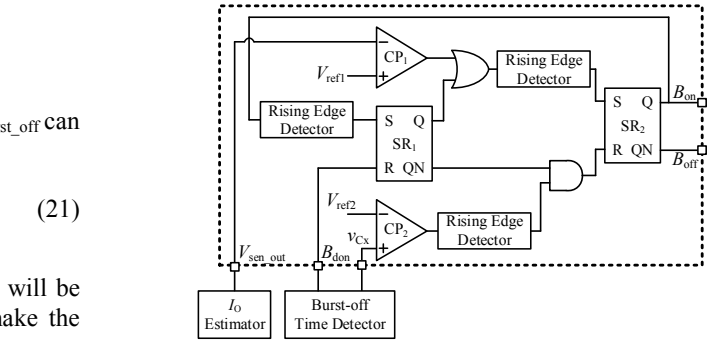


Fig. 19 Mode detector circuit diagram

IV. EXPERIMENTAL RESULTS

The system specifications and parameters are listed in Table 1 and Table 2.

TABLE I. SYSTEM SPECIFICATIONS

Specification	Value	Unit
RMS Input AC voltage (v_{ac})	90 ~ 130	V_{rms}
Output voltage (V_O)	15	V
Output power (P_O)	30	W

TABLE II. COMPONENT PARAMETERS

Parameter	Value	Unit
Transformer turns ratio N_P:N_S:N_{aux}	6:1:1	
Magnetizing inductor (L_m)	340	μH
Maximum switching frequency (f_{s_max})	100	kHz
Input capacitor (C_{in})	82	μF
Output capacitor (C_o)	1	mF
Sensing resistor (R_{sen})	1	Ω

The photograph of the proposed IC is shown in Fig. 20, and it is tested with flyback converter to verify the feasibility.

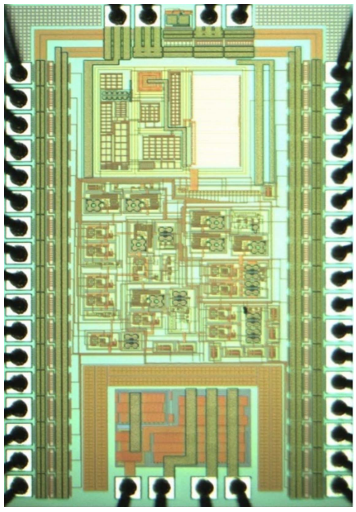


Fig. 20 Photograph of the proposed control IC.

The experimental waveforms of diode condition period detector is shown in Fig. 21. The function works well and agrees with the simulation results.

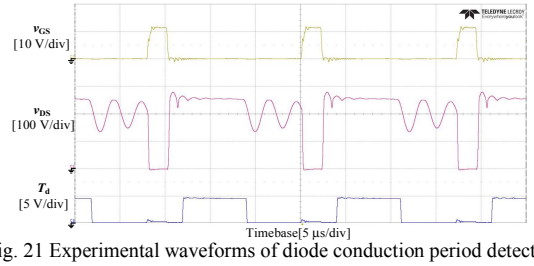


Fig. 21 Experimental waveforms of diode conduction period detector

The experimental waveforms of burst-on/off time detector is shown in Fig. 22. As shown, the signal B_{don} is triggered when the voltage v_{Cy} reaches to 0.5 V, and the flyback converter operates in the burst-on time. When the signal B_{doff} is triggered, the flyback converter changes to the burst-off time.

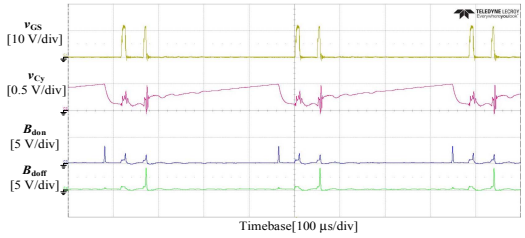
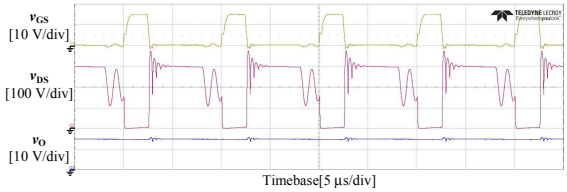
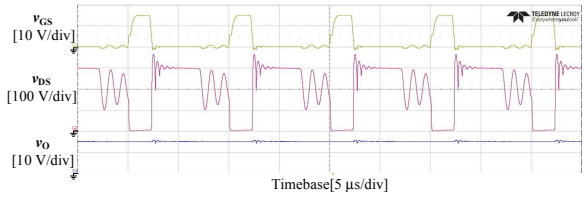


Fig. 22 Experimental waveforms of burst-on/off time detector

The experimental waveforms of the flyback converter in normal mode under different load conditions are shown in Fig. 23. As shown, the output voltage is about 15 V.



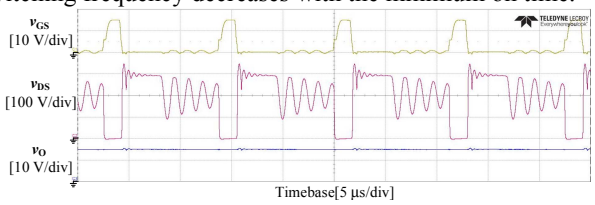
(a) 100% load (v_{ac} = 110 V_{rms})



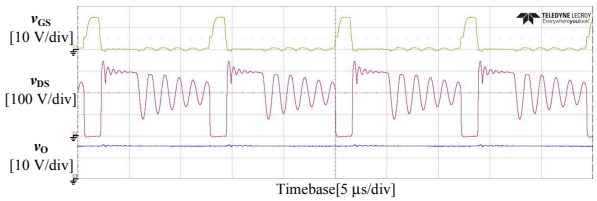
(b) 75% load (v_{ac} = 110 V_{rms})

Fig. 23 Experimental waveforms of flyback converter in normal mode under different load conditions (a) 100% load (b) 75% load

The experimental waveforms of the flyback converter in frequency reduction mode under different load conditions are shown in Fig. 24. As shown, when the load decreases, the switching frequency decreases with the minimum on time.



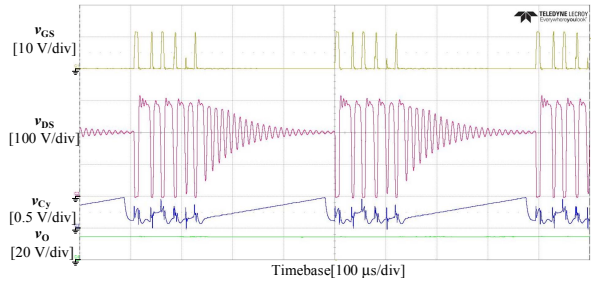
(a) 40% load (v_{ac} = 110 V_{rms} & f_s = 89 kHz)



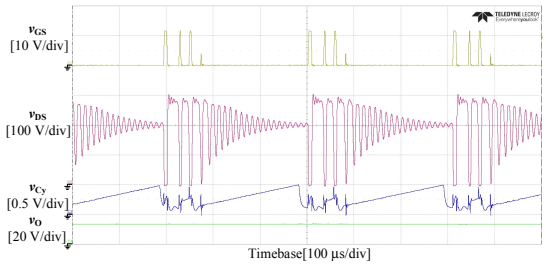
(b) 30% load (v_{ac} = 110 V_{rms} & f_s = 80 kHz)

Fig. 24 Experimental waveforms of flyback converter in frequency reduction mode under different load conditions (a) 40% load (b) 30% load

The experimental waveforms of the flyback converter in burst mode under different load conditions are shown in Fig. 25. As shown, the flyback converter operates in burst mode below the 10% load. With the decreasing load, the burst-on time decreases.



(a) 10% load (v_{ac} = 110 V_{rms})



(b) 5% load (v_{ac} = 110 V_{rms})

Fig. 25 Experimental waveforms of flyback converter in burst mode under different load conditions (a) 10% load (b) 5% load

Fig. 26 shows the measured efficiency curve of the flyback converter under different load conditions. As shown, the efficiency decreases with the decreasing output power. As a result, the switching loss dominates at light load condition. The maximum efficiency is 87.72% when the output power is at 30 W. The experimental results are measured by WT3000, YOKOGAWA.

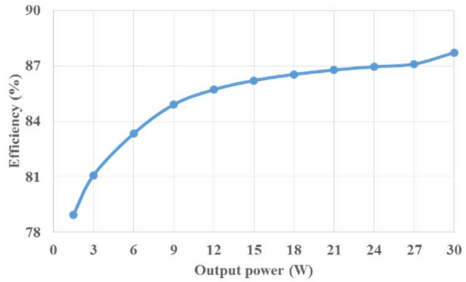


Fig. 26 Measured efficiency curve of flyback converter under different load conditions

V. CONCLUSIONS

A primary-side control IC for AC-DC flyback converter with burst mode energy saving is proposed in this paper. To improve light load efficiency, the frequency reduction mode and burst mode is adopted. In the proposed control IC, the output voltage is sensed through the auxiliary winding, so the output voltage can be regulated precisely by V_O sample circuit. When the on-time of the power switch drops to the minimum, the flyback converter changes the operation to frequency reduction mode. With I_O estimator, the output current can be estimated by the primary-side information, and the proposed control IC can estimate the load to operate in normal mode or burst mode. Furthermore, in burst mode, the burst-on time and burst-off time can be estimated by a simple way which is without the secondary-side feedback control. Therefore, the output voltage ripple can be controlled in burst mode, and the efficiency can be improved at light load.

REFERENCES

[1] H. D. Hsu, T. J. Liang, B. D. Liu, and K. H. Chen, "Design of a Green Mode PWM Control IC," in *Circuits and Systems (APCCAS), 2008 IEEE Asia Pacific Conference on*, pp. 1876-1879, 2008.

[2] L. Jiana, W. Xiaobo, C. Hai, and Y. Xiaolang, "Design of High Efficiency Green Mode SMPS Regulator," in *Circuits and Systems for Communications (ICCSC), 2008 4th IEEE International Conference on*, pp. 564-567, 2008.

[3] P. Luo, L. Luo, Z. Li, J. Yang, and G. Chen, "Skip Cycle Modulation in Switching DC-DC Converter," in *Communications, Circuits and Systems and West Sino Expositions, 2002 IEEE International Conference on*, vol. 2, pp. 1716-1719, 2002.

[4] L. Fuhua, W. Hanxiang, L. Zhenghao, and X. Weiguo, "Design of an Off-Line AC/DC Controller Based on Skip Cycle Modulation," in *Integrated Circuits (ISIC), Proceedings of the 2009 12th International Symposium on*, pp. 228-231, 2009.

[5] T. H. Chen, W. L. Lin, and C. M. Liaw, "Dynamic Modeling and Controller Design of Flyback Converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 35, no. 4, pp. 1230-1239, Oct. 1999.

[6] Y. Panov and M. M. Jovanović, "Small-Signal Analysis and Control Design of Isolated Power Supplies with Optocoupler Feedback," *IEEE Trans. on Power Electron.*, vol. 20, no. 4, pp.823-832, Jul. 2005.

[7] W. Kleebchampee and C. Bunlaksananusorn, "Modeling and Control Design of a Current-Mode Controlled Flyback Converter with Optocoupler Feedback," in *2005 International Conference on Power Electronics and Drives Systems*, 2005.

[8] C. J. Chang and C. L. Chen, "An Isolated Output-Feedback Scheme with Minimized Standby Power for SMPS," *IEEE Trans. on Power Electron.*, vol. 28, no. 11, pp. 5140-5146, Nov. 2013.

[9] Y. K. Lo, J. Y. Lin, C. F. Wang, and C. Y. Lin, "Analysis and Design of a Dual-Mode Flyback Converter," in *Sustainable Energy Technologies (ICSET), 2010 IEEE International Conference on*, pp. 1-3, Dec. 2010.

[10] X. Chen, T. Jiang, S. Zhao, H. Zeng, and J. Zhang, "Evaluation of Primary Side Control Schemes for Flyback Converter with Constant Current Output," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, pp. 1859-1863, 2013.

[11] J. Zhang, H. Zeng, and T. Jiang, "A Primary-Side Control Scheme for High-Power-Factor LED Driver with TRIAC Dimming Capability," *IEEE Trans. on Power Electron.*, vol. 27, no. 11, pp. 4619-4629, Nov. 2012.

[12] P. L. Huang, D. Chen, C. J. Chen, and Y. M. Chen, "An Adaptive High-Precision Overpower Protection Scheme for Primary-Side Controlled Flyback Converters," *IEEE Trans. on Power Electron.*, vol. 26, no. 10, pp. 2817-2824, Jan. 2011.

[13] H. H. Chou, Y. S. Hwang, and J. J. Chen, "An Adaptive Output Current Estimation Circuit for a Primary-Side Controlled LED Driver," *IEEE Trans. on Power Electron.*, vol. 28, no. 10, pp. 4811-4819, Oct. 2013.

[14] C. N. Wu, Y. L. Chen, and Y. M. Chen, "Primary-Side Peak Current Measurement Strategy for High-Precision Constant Output Current Control," *IEEE Trans. on Power Electron.*, vol. 30, no. 2, pp. 967-975, Feb. 2015.

[15] X. Xie, J. Wang, C. Zhao, Q. Lu, and S. Liu, "A Novel Output Current Estimation and Regulation Circuit for Primary Side Controlled High Power Factor Single-Stage Flyback LED Driver," *IEEE Trans. on Power Electron.*, vol. 27, no. 11, pp. 4602-4612, Nov. 2012.

[16] "LTC3442 Micropower Synchronous Buck-Boost DC/DC Converter with Automatic Burst Mode Operation" Linear Technology, 2013.

[17] "Deep Burst Mode Operation with Feedback Impedance Modulation for Reducing Standby Power Consumption of Switched-Mode Power Supplies", Fairchild Semiconductor, 2012.

[18] B. H. Lee, Y. D. Kim, and G. W. Moon, "Single Switching Double Powering Converter for Reducing Power Consumption of AC/DC Adapter in Standby Mode." in *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on*, pp. 199-204, 2011.

[19] H. S. Choi and D. Y. Huh, "Techniques to Minimize Power Consumption of SMPS in Standby Mode," in *Power Electronics Specialists Conference (PESC), 2005 IEEE 36th*, pp. 2817-2822, 2005.

[20] J. S. Li, T. J. Liang, K. H. Chen, Y. J. Lu, and J. S. Li, "Primary-Side Controller IC Design for Quasi-Resonant Flyback LED Driver," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, pp. 5308-5315, 2015.

[21] Y. T. Lin, T. J. Liang, and K. H. Chen, "IC Design of Primary-Side Control for Flyback Converter," in *Future Energy Electronics Conference (IFEEC), 2013 1st International*, pp. 449-453, 2013.