A Digital Detecting Method for Synchronous Rectification Based on Dual-Verification for LLC Resonant Converter

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***Abstract*—GaN HEMT has a higher voltage drop than conventional silicon based power MOSFETs during the time of reverse conduction, which is an unneglectable interval in *LLC* converter with synchronous rectification (SR). To further improve the efficiency of the *LLC* resonant converter, this paper presents a SR detecting scheme base on an adaptive drain-source voltage sensing strategy to eliminate both the body diode conduction and reverse current from the load to the source. Compared to the current SR detecting methods, the turning off time of the SR can be stabilized by the proposed dual-verification technique instead of switching between the body diode conduction and the reverse current from the load to the source. The principle and the algorithm are discussed and optimized based on the operating modes and the turning off transition of the SR. A prototype based on GaN HEMT is built and tested to verify the proposed method. The experimental results show that the proposed SR detecting scheme eliminates the current from the load to the power source, thus, the reliability of the converter can be improved. Moreover, compared to the current best technique, the efficiency of the converter is further improved by 0.2%.**

Keywords—LLC resonant converter, synchronous rectification, digital control, dual-verification.

I. INTRODUCTION

The LLC series resonant half/full bridge converters are now very popular for those applications with power level above 120W, because of achieving both zero voltage switching (ZVS) and zero current switching (ZCS) for the power switches on primary side and secondary side, respectively [1-5]. The synchronous rectifiers (SR) are employed to replace the secondary side diode rectifiers to further improve the efficiency by decreasing conduction loss and parasitic capacitances, especially in the large current applications [6-9]. However, the body diode conduction and the current from the load to the power source have always been issues when SR is applied, since these two issues decrease both the efficiency and the reliability of the converter. Moreover, the power switches nowadays are evolving from silicon (Si) to wide bandgap materials such as GaN devices. Since the voltage drop of GaN HEMTduring the time of reverse conduction is much higher than that of Si MOSFETs, reducing the body diode conduction and the current from the load to the power source become more necessary.

Presently, based on the sensing method, the SR driving scheme in LLC resonant converter can be divided into 3 classes: current sensing technique; analog voltage sensing with self-driven technique; and digital sensing technique achieved by FPGA/microcontroller (MCU) [10-18]. Although the current sensing is the most accurate method, the power loss of the resistance introduced by the extra current detector is quite impressive. Thereby, judging the SR shutdown time by detecting the drain-source voltage VDS(SR) turns to be the most proper method. However, the analog voltage sensing technique with self-driven has complicated circuits [10-11], which deteriorates the power density and leads to gate-source parasitic oscillation. Also, this technique cannot fit all the secondary side rectifier circuits.

The digital voltage sensing technique has been widely investigated in recent years for 3 advantages: simple circuit to improve the power density; accurate at high frequency to reduce the ratio of the body diode conduction; and fast algorithm is required to prevent the reverse conduction [10-14].

A digital SR driving scheme is proposed to detect the conduction of the body diode and shutdown the power MOSFET adaptively [15]. However, the efficiency is influenced by the two steady-states switching between the body diode conduction and the reverse conduction. Also, the two steady-states switching mechanism would amplify the body diode conduction loss and the reverse conduction loss in high frequency applications. The proposed SR driving scheme in [15] has been optimized for the high frequency applications by adding an extra ripple detector [16]. However, the fundamentals of the proposed method are not improved, thus the efficiency is still deteriorated.

To overcome the limitations of these approaches, this paper presents a SR detecting scheme based on an adaptive $V_{DS(SR)}$ sensing strategy to eliminate both the body diode conduction and reverse current. The core of the consideration is a dual-verification both before and after the turning off behavior. With the verifications, the proposed driving scheme can achieve the complete channel conduction in an ideal condition. When this strategy is applied in a MCU with limited clock frequency, the reverse current can be eliminated, thus, the *LLC* resonant

converter can achieve higher efficiency. The key issues such as the sampling strategy, the operating under different conditions are also discussed.

This paper is organized as follows. Section 2 describes the principle of the proposed SR driving scheme in a *LLC* resonant converter; Section 3 analyzes the performance and implementations of the sample strategy; and finally, the experimental performance is presented in Section 4 with the proposed solutions.

II. THE ADAPTIVE SR DRIVING SCHEME

A synchronous *LLC* resonant full-bridge converter is illustrated in Fig.1. The power switches are configured to form a square-wave voltage with alternating 50% duty cycles for each switch. A small dead time is inserted between the consecutive transitions, both to prevent the possibility of cross-conduction and to allow time for achieving ZVS. D_1~D_4 and C_1~C_4 are the body diodes and the output capacitances of M_1~M_4, respectively. The secondary side of the proposed converter is a Class D synchronous rectification structure based on center-tapped transformer. The secondary side includes the power switches M_5~M_6, the body diodes D_5~D_6, the output capacitances C_5~C_6 and the filter capacitor C_f.

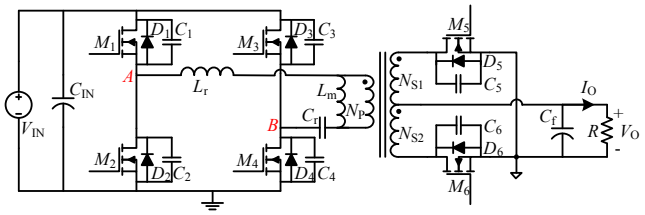

Fig. 1 Full-bridge LLC resonant converter with the synchronous rectification

The desired SR gate driving signal has been proposed in [15]. The SRs are turned ON synchronously with the main switches to cover the three different modes. However, the OFF time of the SR gate driving signals are not in phase with the gate driving signals of the primary switches.

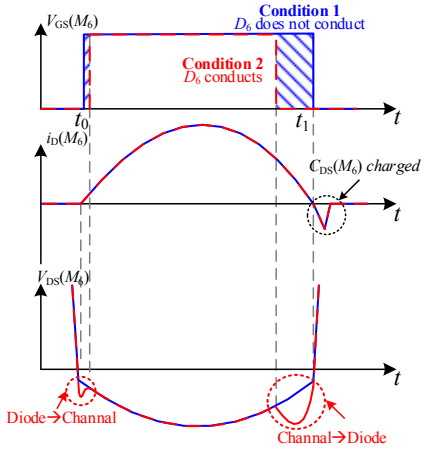

Fig. 1 Conduction loss influenced by the OFF time of VGS(M6)

When SRs are turned OFF too early, the body diodes would conduct, as shown in Fig. 2. Compared to the condition 1, the $V_{GS(M6)}$ in condition 2, which indicates the SR is turned OFF too late, leading to the body diode conduction. Furthermore, when GaN HEMT are employed as SRs, these issues become more critical, since the voltage drop of GaN HEMT during the reverse conduction is higher than that of Si power MOSFETs.

To overcome the drawbacks of the SR driving scheme in [15-16], a dual-verification VDS(SR) sampling strategy is proposed, as shown in Fig. 3. Compared with the current solutions, the body diode conduction detecting comparator is replaced by an operational amplifier. Thus, one or more internal A/D converters (ADCs) are employed to process the analog signals. The R_0 and C_0 constitute a low pass filter, which eliminates the noise at the footprint of the MCU. If the filter is designed properly, the influence of the filter can be ignored during the analysis.

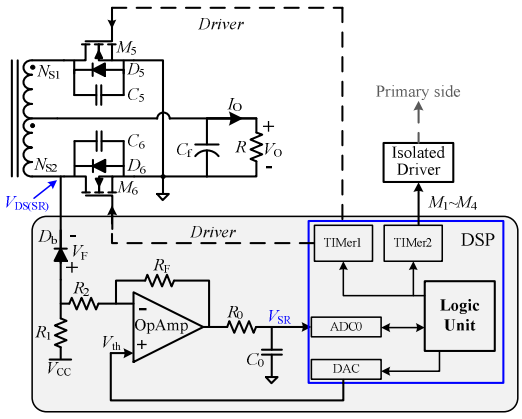

Fig. 3 The proposed dual-verification SR driving scheme

The dual-verification is considered to sample the V_{SR} right before and after the turning OFF transition of the SR, as illustrated in Fig. 4. The first and second sampled SR voltage are defined as $V_{SR(1)}$ and $V_{SR(2)}$, respectively.

Fig. 4 (a) shows the initial state of the SR gate driving signal, which is turned off too early, then the body diode conducts for quite a long time. In this case, $V_{SR(1)} < V_{SR(2)}$, and the two voltages are both negative. Thus, the ON time of the SR gate driving signal would increase a longer time step Δt in the next period.

Fig. 4 (b) shows the next period of the initial state. Compared with the initial state, the conduction of the body diode is reduced. However, since the body diode conduction still exists, the time step Δt would still be added in the next period.

A few periods later, $V_{SR(1)} > V_{SR(2)}$. This relationship means the body diode conduction is eliminated completely. However, if $V_{SR(1)}$ is positive or $V_{SR(2)}$ is in the V range, the ON time of the SR is also improper, as illustrated in Fig. 4 (d). In this case, the current flows from the load to the power source, which decreases reliability and efficiency of the converter.

The only condition that achieves the desired SR gate driving is shown in Fig. 4 (c). In this condition, $V_{SR(1)}$ is negative while $V_{SR(2)}$ is positive. Moreover, the two sampled voltages both

have low levels. In the ideal condition, the time between the two sampling is narrow enough, since the turning OFF time of the SR is between the two samples, the SR is turned OFF exactly at zero current in the ideal condition.

a)

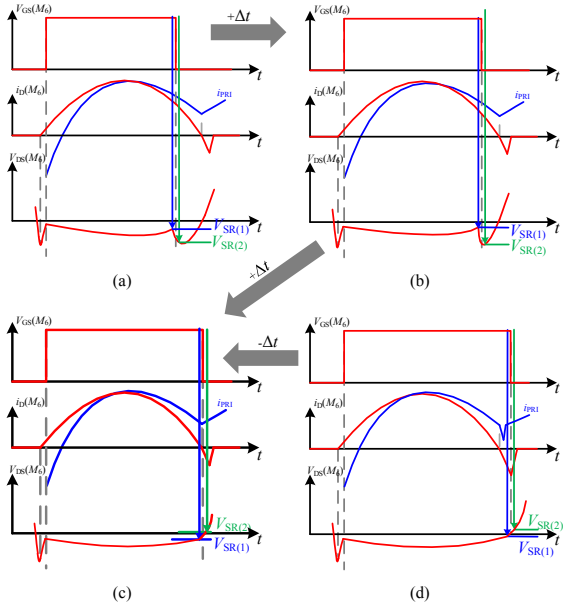

Fig. 2 The turning OFF process of the SR to eliminate the body diode conduction; (a) The initial state of the SR gate signal; (b) The body diode conduction is reduced; (c) The ideal condition of the proposed control strategy; (d) The reverse current condition when the SR is turned OFF late

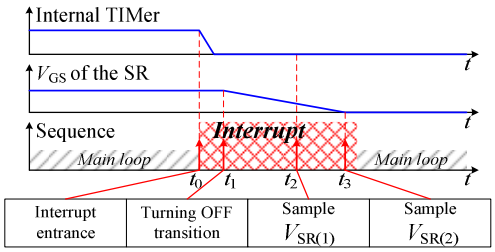

Fig. 5 The sequence of the program and the turning OFF transition of the SR

b)

Unfortunately, both the speed and the accuracy of the MCU is limited. Thus, there exists a delay between the two sampling, hence, the sampling strategy and controlling algorithm should be considered and optimized. The desired algorithm of the sampling is shown in Fig. 5.

An interrupt achieved by a TIMer is applied to achieve the sampling and turning OFF. First, the interrupt is triggered at the falling edge of the TIMer. Although the internal TIMer is turning OFF, the SR is still ON because of the parasitic delay and the discharging process of the gate-source capacitance. Thus, the first sampling is before or during the turning OFF state. Second, another sampling is set after the turning OFF state, the time inserted between the two samplings should consider the clock of the ADC, the delay of the circuit/program and the turning OFF transition. The turning off procedure of the SR and the characteristics of the ADC/TIMer would be analyzed in detail in section 3 based on Fig. 5.

III. Investigation of the Proposed SR Driving Scheme

A. The voltage range of the sampled drain-source voltage

The SR sampling circuit is shown in Fig. 3, the parameters should be designed to ensure that the voltage can reflex the state of the SR accurately. During the most OFF state time, the drain-source voltage across M_6 is high enough, which means the blocking diode D_b is reversely biased. The sampled V_{SR} is calculated as

$$V_{SR(OFF)} = \frac{R_2 V_{CC} + R_1 V_{th}}{R_1 + R_2} \tag{1}$$

During the ON state and the rest time of the OFF state, the drain-source voltage of M_6 is low, as shown in Fig. 2, thus D_b is forwardly biased. The sampled V_{SR} in this interval is calculated as

$$V_{SR(ON)} = \left(1 + \frac{R_F}{R_2}\right) V_{th} - \frac{R_F}{R_2}\left(V_{DS(SR)} + V_F\right) \tag{2}$$

In equation (2), V_F represents for the forward voltage drop of D_b. Compared with $V_{SR(ON)}$, $V_{SR(OFF)}$ should be significantly high, so that the MCU can detect the turning off transition according to the sampled V_{SR}.

The sampled V_{SR} in different states has been calculated in equation (1) and (2), respectively. To distinguish the V_{SR} during the turning OFF transition, a coefficient m is defined to reflex the ratio of $V_{SR(ON)}$ and $V_{SR(OFF)}$, thus, a relationship can be built

$$V_{th} > \frac{R_2 V_{CC} + m\left(R_1 + R_2\right)\frac{R_F}{R_2}\left(V_{DS(max)} + V_F\right)}{m\left(R_1 + R_2\right)\left(1 + \frac{R_F}{R_2}\right) - 1} \tag{3}$$

In equation (3), $V_{DS(max)}$ represents for the maximum value of the drain-source voltage during the turning OFF transition. Thus, the minimum value of V_{th} can be decided in different cases.

B. Turning off procedure and the time delay

STM32F4 series MCU is chosen to illustrate the proposed SR detecting and judging mechanisms. The maximum clock frequency of the ADC is 36MHz, the minimum sample time is 3 periods, and the conversion time is 12 periods, the resolution time of the ADC is 416ns. In high frequency applications, this resolution is unacceptable. Fortunately, the STM32F4 has at least 2 ADCs, also, these ADCs can be configured as alternate mode, as illustrated in Fig. 6. Since there are only 5 periods between the 2 ADCs, the resolution of the ADCs can be calculated as

$$t_{delay-ADC} = \frac{1}{36(MHz)} \times 5(cycle) = 138(ns) \tag{4}$$

The resolution of the ADC can be further improved by employing a high speed external ADC, however, the cost of the ADC would be impressing. Thus, considering the sampling time to fit the proposed algorithm becomes more realistic.

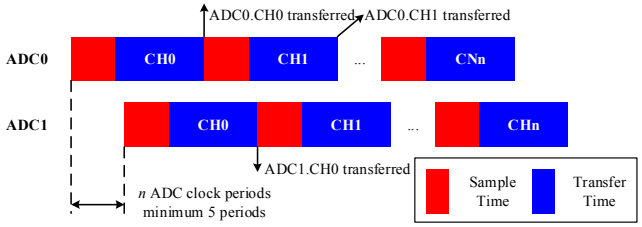

Fig. 6 The operating diagram of the ADCs under alternate mode

The different shutdown times of a GaN HEMT is simulated in Fig. 7 when the drain current varies. The destination of the simulation is verifying the possibility of the proposed SR driving scheme under MHz switching frequency. The V_{DS} remains for about 20ns despite the drain current varies between 0~4A, and starts to rise 120ns later than the V_{GS} dropping moment. Also, the gate driver circuit introduces tens nanoseconds to the SR. According to these considerations, there are about 140ns delay between the SR turning off command and the $V_{DS(SR)}$ rising. Thus, the strategy of the sampling can be optimized as:

(1) Start the interrupt, execute the SR turning off command;

(2) Sample $V_{SR(1)}$ when SR is still on;

Sample $V_{SR(2)}$, since there are 138ns between the sample commands, the SR just starts rising.

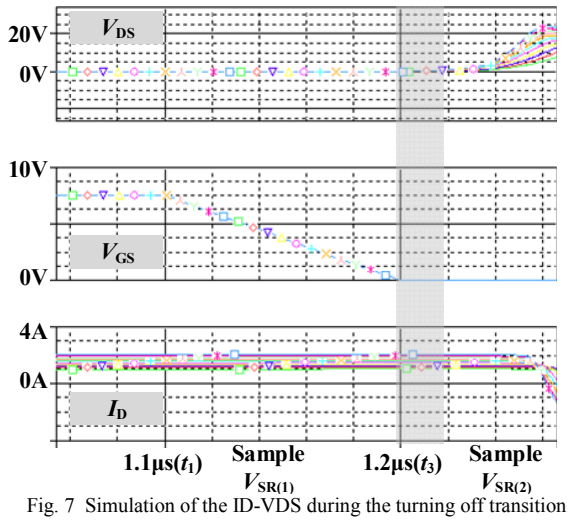

Fig. 7 Simulation of the ID-VDS during the turning off transition

C. Algorithm of the control program

The algorithm of the control program consists of an interrupt for controlling the devices and the main loop for calculating and judging, as illustrated in Fig. 8. The devices controlled by the interrupt are TIMer and the ADCs, for generating the SR driving signal and sampling V_{SR}, respectively.

When the count (CNT) register of the TIMer reaches the threshold (CCR), the interrupt is triggered. At the beginning of the interrupt, a command is executed to shut OFF the SR. Since the parasitic parameters of the circuits and the gate-drive circuit bring delays, the SR starts turning OFF after tens nanoseconds. Assume the delay is t_1, V_{GS} of the SR starts to fall at t_1, V_{GS} falls to 0 at t_2. During the t_1~t_2 interval, V_{GS} of the SR is shutting OFF, while SR is still ON. Thus, sampling $V_{SR(1)}$ during the transition is proper. Moreover, the sampling time of $V_{SR(1)}$ decides the accuracy of the proposed algorithm. When the converter is in steady-state, $V_{SR(1)}$ should be calculated as negative, and the amplitude is the production of the $R_{DS(on)}$ and the secondary current I_S. Since $R_{DS(on)}$ and I_S are both low, $V_{SR(1)}$ is a significant low value.

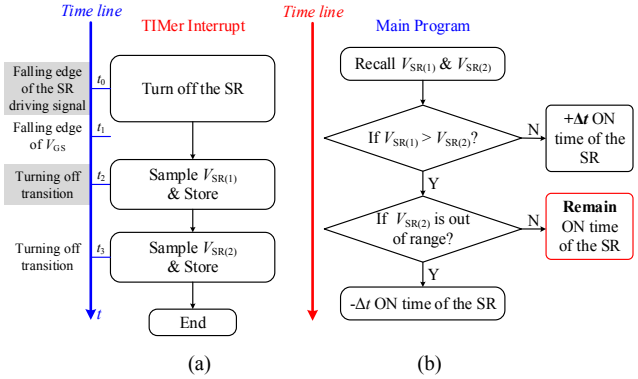

Fig. 3 The algorithm of the control program (a) The interrupt achieved by the TIMer; (b) The main program

As soon as SR is turned OFF, $V_{SR(2)}$ is sampled. In the steady-state, $V_{SR(2)}$ should be positive and in a proper range. Thus, SR is turned OFF at the most efficient time. When $V_{SR(2)}$ is detected as negative, the body diode is conducted, which means the SR is turned off too early. When $V_{SR(2)}$ is detected to be positive but out of range, the current flows from the load to the power source, which indicates the SR is turned off too late.

In fact, the most efficient turning OFF time is unique, as shown in Fig. 4 (c). The other turning OFF times can be detected accurately and regulated accordingly. Compared with the method proposed in [15], the dual-verification technique proposed in this paper has only one steady-state, as shown in Fig. 8(b).

However, the resolutions of actual MCU and FPGA is limited, hence, the turning OFF the SR at the specific best time seems to be impossible. The control program must be optimized to fit the different applications. The most important issue is to compromise between the body diode conduction and the reverse current. Both the two conditions deteriorate the efficiency by introducing extra power loss. Meanwhile, the reverse current does not only decrease the efficiency, but also influence the reliability of the converter and the output range. Based on this consideration, the body diode conduction is preferred, and the reverse current should be eliminated completely.

D. The operation at light load condition and the control strategy

The principle of the proposed SR control when $f_S < f_r$ has been discussed. However, since the *LLC* resonant converter can also operate when $f_S \geq f_r$, the turning OFF strategy of the SR should be further investigated. Furthermore, the control strategy according to the switching frequency of the *LLC* resonant converter can be concluded.

To decrease the switching loss and the reverse recovery at light load condition, the turning OFF time should be slightly delayed compared to the primary side gate driving signal. With the strategy shown in Fig. 4, the body diode conduction and the reverse current can also be detected and eliminated well. In this case, the waveforms of the secondary current and the SR gate signal are shown in Fig. 9. Thus, the proposed driving scheme can be applied in both the ZVS region and the SRC region of the *LLC* resonant converter.

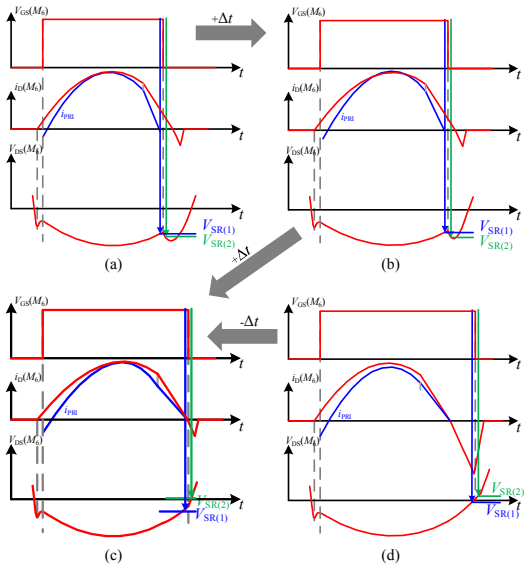

Fig. 9 The turning OFF process of the SR to eliminate the body diode conduction when fS > fr; (a) The initial state of the SR gate signal; (b) The body diode conduction is reduced; (c) The ideal condition of the proposed control strategy; (d) The reverse current condition when the SR is turned OFF late

IV. Experimental Results

A 200W LLC resonant converter is built to verify the proposed SR detecting scheme. The form of the prototype is 12V/17A output, other parameters are listed in Table 1. The main parameters of the prototype are listed in Table 2. The photograph of the prototype is shown in Fig. 10.

Table 1 Parameters of the prototype

Parameter	Value
V_{IN}	350~400V
V_{OUT}	12V
I_{OUT}	1~17A
f_S	600~1000kHz

Table 2 List of the key parameters

Components	Part Number	Parameters
M_1~M_4	GS66502B (GaNSystems)	650V/7.5A
M_5~M_6	GS61004B (GaNSystems)	100V/45A
Gate Driver for M_1~M_4	Si8273 (Silicon Labs)	Isolated Gate Driver
Gate Driver for M_5~M_6	IR4427 (Infineon)	Dual Low-Side Gate Driver
MCU	STM32F407 (STMicroelectronics)	168MHz clock frequency, 84MHz TIMer frequency 36MHz ADC frequency
		FPU inside

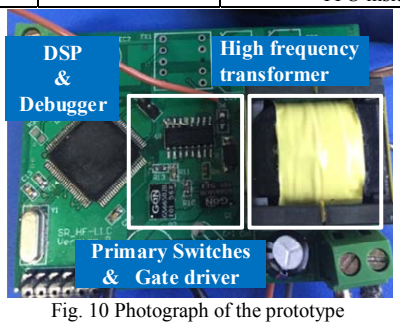

Fig. 10 Photograph of the prototype

The clock frequency of the MCU is 168MHz, and the clock frequency of the TIMer is 84MHz, thus, the minimum time resolution of the TIMer Δt is 12ns.

The key voltages of the primary side at full load condition are tested, as shown in Fig. 11. Since the drain-source voltage $V_{DS(PRI)}$ has decreased to 0 before the gate-source voltage $V_{GS(PRI)}$ starts to rise, the ZVS of the primary side power switches are achieved. Based on the $V_{GS(PRI)}$ of the primary side, the primary side current at different load conditions are tested, as shown in Fig. 12(a)(b). It is proved that the *LLC* resonant converter is operating under the ZVS operating region. In this condition, the SR is turned off earlier than the primary switches at full load condition.

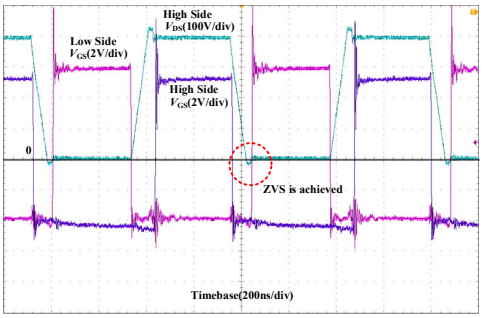

Fig. 11 Test waveforms of the primary side at full load condition

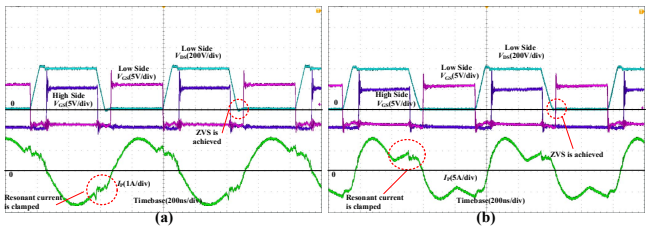

Fig. 4 Comparison of the VGS(PRI) and resonant current at (a) 20% load (b) full load

The $V_{DS(SR)}$ and secondary side current are also tested and compared, as shown in Fig. 13. The body diode conduction has been reduced to the minimum by the proposed dual-verification algorithm, and the reverse current is eliminated according to the test results.

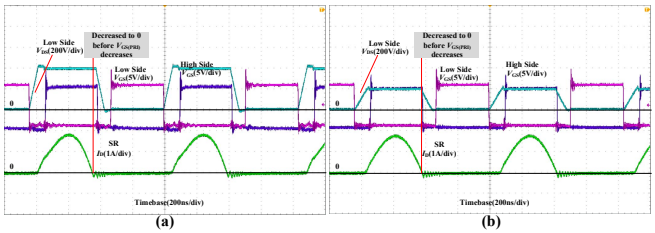

Fig. 13 Test waveforms of VDS(SR) and VGS(SR) at full load condition

However, the oscillation still exists after the SR is turned OFF. The reason is the parasitic capacitance C_{oss} of the SR has to be charged after the turning OFF transition to build the off-state voltage, thus the leakage inductance of the transformer, the parasitic inductance of the PCB and the C_{oss} form a RLC network, the resonant frequency is $1/2\pi\sqrt{LC}$.

The $V_{GS(SR)}$, $V_{DS(SR)}$ are also tested and compared in inductive operating region, as shown in Fig. 14 (a)~(d), the SR is exactly shut OFF when the resonant current is clamped by the magnetizing current. Also, it should be noted that high frequency oscillation, which is caused by the parasitic parameters on the PCB, can be observed at $V_{DS(SR)}$.

This characteristic challenges the conventional SR drive ICs even more, since the constant threshold voltages are far more easily to be triggered accidently and cause a long-time body diode conduction. However, since the proposed SR detecting technique samples at specific time position, the influence of the parasitic oscillation can be eliminated, thus the reliability of the converter can be ensured.

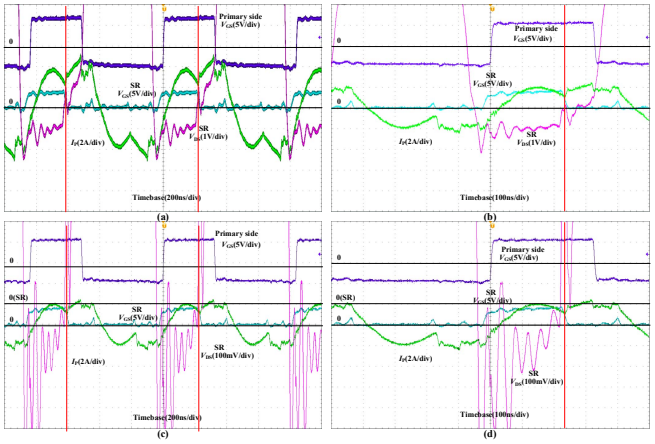

Fig.14 Test results in a high frequency LLC resonant converter based on GaN HEMT

Furthermore, at light load condition, the $V_{GS(PRI)}$ and $V_{GS(SR)}$ are also tested with I_P, as shown in Fig.15. Since the magnetizing current no longer clamps the resonant current, the LLC resonant converter is operating under SRC mode. The gate driving signal of the SR is turned off after the primary switch. However, the primary switch is turned off with larger load current, the miller platform lasts longer than the SR, thus, the primary switch remains on by the time the SR has been turned off exactly.

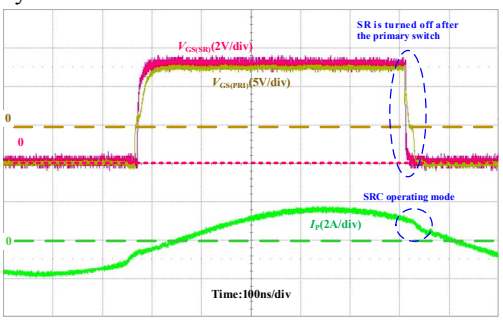

Fig. 15 Comparison of the $V_{GS(PRI)}$ and $V_{GS(SR)}$ at full load condition

At last, the efficiency of the converter with the proposed dual-verification SR detecting method is tested, as shown in Fig. 16. Compared with the *LLC* converter with the SR detecting techniques proposed in [15], the efficiency over the entire load range is improved over 0.2%.

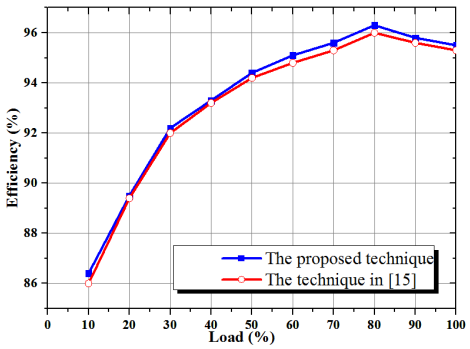

Fig. 5 The efficiency curve over the entire load range

V. CONCLUSION

A dual-verification SR detecting method in high frequency applications is proposed in this paper. Compared with the conventional SR detecting techniques, the proposed detecting method samples the V_{DS} for two times during the turning off transition of the SR. The circuit configuration, the algorithm inside the MCU are discussed, as well as the application in all the operating modes of the *LLC* resonant converter. A GaN HEMT based prototype is built and tested, the experimental results show that the proposed SR detecting method can reduce the reverse conduction time, meanwhile, the current from the load to the power source is eliminated. Compared with the conventional SR detecting techniques, the proposed dual-verification SR detecting method improves the efficiency of the converter over 0.2%. Also, the proposed SR detecting method is proved to be effective in MHz level applications.

ACKNOWLEDGMENTS

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