Integrated Switched-Capacitor-Based Cold-Start Circuit for DC-DC Energy Harvesters with Wide Input/Output Voltage Range and Low Inductance in 40-nm CMOS

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***Abstract*— This paper outlines an integrated switched-capacitor (SC)-based cold-start circuit for dc-dc energy harvesters that uniquely combines a low cold-start voltage, wide input/output voltage and low inductance value in the boost stage. The proposed design specifically targets size-constrained, self-powered Internet-of-Things applications. The proposed design is an SC circuit built from low-threshold-voltage devices operating in the sub-threshold region and provides the drive voltage for high-threshold-voltage devices of the boost dc-dc converter. The SC circuit is an NMOS-based Dickson charge pump driven synchronously with a series of cross-coupled voltage doublers and voltage multiplying gate drivers. The SC circuit, which is integrated together with a boost converter as the dc-dc energy harvester, has been implemented in a 40-nm CMOS process for future system-on-chip integration. The measured results show that with a 4.7 μH boost converter inductance, the design can start up from typical input voltages as low as 190 mV while offering up to 2.4 V input and 5 V output voltage compatibility.**

I. Introduction

Self-powered energy harvesters are essential in size-constrained internet-of-things (IoT) applications. In these applications, the harvested ambient energy is stored in capacitor banks as the preferred energy storage element [1]–[5]. The absence of a battery, combined with the low output voltage of generators such as photovoltaic (PV) cells or thermoelectric generators (TEG), necessitates a low-voltage boost cold-start circuit. Moreover, wide input voltage range is required to accommodate a variety of energy sources in IoT applications. For instance, single- and three-cell PV energy sources provide voltages in the range of 0.8 V and 2.4 V, respectively.

Several solutions can be found in the literature for solving the cold-start problem from low input voltages in energy harvesting applications [6]–[14]. The existing designs can be generally classified as a DC-DC boost converter with: I) external excitation such as mechanichally-assisted or transformer-based solutions, [6], [7], and II) integrated charge pump circuits [8]–[14]. However, the latter approach is preferred due to its higher drive capability, smaller form factor, and lower cost. The most recent existing DC-DC boost energy harvesters with charge-pump-based cold-start circuitry are summarized and compared in Table I. As seen in Table I, [8]–[10] do not offer an operating voltage range higher than 1.25 V. On the other hand, the designs proposed by [11]–[14] offer wider input/output voltage range but with higher cold-start voltages.

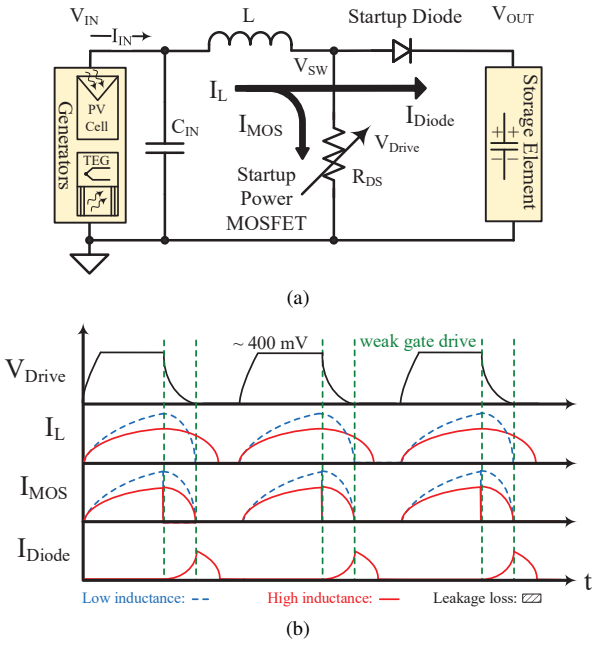

Fig. 1. (a) Schematic of a boost converter circuit, and (b) corresponding voltage and current waveforms for a weak gate-drive supply.

Considering the shortcomings of the existing solutions, this paper demonstrates an integrated charge-pump-based cold-start architecture for DC-DC boost energy harvesters. The proposed charge-pump topology, denoted as the voltage-doubler-linked Dickson charge pump (VDL-DCP), incorporates the following unique features:

- a Dickson charge pump (DCP) [15] with actively boosted gate signals to improve efficiency,
- an auxiliary cross-coupled voltage doubler (VD) [16] to generate gate-drive power, and
- voltage-multiplying gate drivers of the DCP that make use of preceding and/or following auxiliary VD stages to drive DCP switches.

As compared to the exiting solutions, the presented design can achieve a lower cold-start voltage, with smaller inductance value and higher operating voltage range, without the need for an external excitation or other start-up aids such as post-fabrication threshold voltage tuning.

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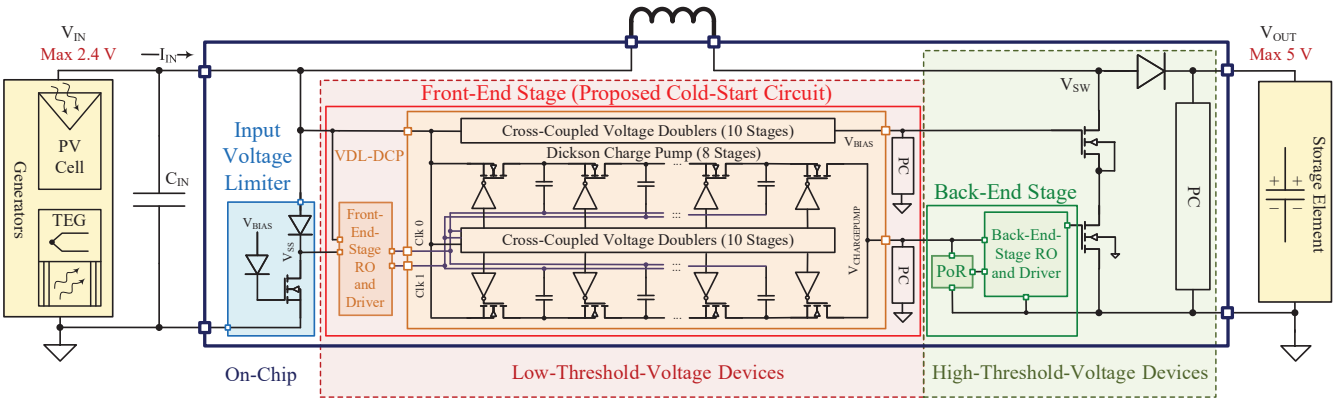


Fig. 2. Top-level block diagram of the proposed cold-start circuit integrated with a boost converter as the dc-dc energy harvester (RO: ring oscillator, PC: power clamp, PoR: power-on-reset, VDL-DCP: voltage-doubler-linked Dickson charge pump).

TABLE I
COMPARISON OF EXISTING DC-DC BOOST ENERGY HARVESTERS WITH CHARGE-PUMP-BASED COLD-START CIRCUITRY.

Rep. Ref.	**[8]**	**[9]**	**[10]**	**BQ25505 [11], [12]**	**MB39C831 [13]**	**ADP5090 [14]**	**This Work**		
Year	2012	2015	2016	2013	2013	2014	2017		
Tech. node (nm)	65	130	130	N/R	N/R	N/R	40		
Max. input volt. (V)	1	1	**1**	**5.1**	4.75	3.3	**2.4**		
Max. output volt. (V)	1	1.1	**1.25**	**5.5**	5.5	5.2	**5**		
Startup volt. (mV)	95	220	**70**	**330**	350	380	**230**	**190**	**170**
Inductance value (μH)	6.8	10	**200**	**22**	4.7	22	**0.5**	**4.7**	**20**
Active die area (mm^2)	0.17	0.15	0.6	N/R	N/R	N/R	0.3		

This paper is organized as follows. Section II presents design challenges for low-voltage cold-start circuitry. Sections III and IV present the proposed cold-start design and the measured experimental results, respectively. Section V summarizes final conclusions.

II. Design Challenges of Cold-Start Circuits

Modern CMOS technologies offer a combination of devices with low threshold voltage (V_{th}) (~100 mV) which have a blocking voltage (BV_{DS}) of ~1.2 V, alongside those with higher V_{th} (~500 mV) which have higher BV_{DS} (~2.5 V). Although it is possible to fabricate devices having both low V_{th} and high BV_{DS}, such devices are likely to have more off-state leakage and are detrimental for power-constrained applications. Nonetheless, using devices with low V_{th} can reduce the cold-start voltage, while using those with high BV_{DS} are needed to increase the operating voltage range. To address this challenge, a mixed-device design approach is commonly used, in which the dc-dc energy harvester comprised of high-V_{th} devices is driven with an auxiliary switched-capacitor (SC) converter (cold-start circuit) built from low-V_{th} devices [9], [11]–[14], [17]. Although the concept is straight-forward, realizing it with a low inductance value presents a design challenge to the SC converter. When the power MOSFET in the boost converter is driven by a low-amplitude signal with a slow rise/fall time, as shown in Fig. 1, the charge drawn from the input capacitor is completely dissipated in the power transistor instead of being delivered to the output, unless the inductance is sufficiently high. Although this phenomenon can be mitigated by using larger inductance values and/or low-V_{th} devices, doing so would either increase the system size or decrease the maximum operating voltage.

III. Switched-Capacitor Based Cold-Start Circuit

In this paper, an integrated SC-based cold-start architecture for dc-dc energy harvesters is presented. The design is optimized to support low cold-start voltage and wide operating voltage range, while minimizing inductance value. The top-level block diagram of the proposed cold-start circuit, integrated with a boost converter as the dc-dc energy harvester, is shown in Fig. 2. The study-system includes: 1) a front-end stage, which is the proposed SC-based cold-start circuit, 2) an input voltage limiter that protects the front-end stage from exposure to voltages exceeding device limits, i.e., 1.2 V in this process, and 3) a back-end stage which contains the gate driver and power transistors of the boost converter.

1) *Front-End Stage (Cold-Start Circuit):* A cold-start circuit with a DCP architecture is commonly used to power the back-end stage during system start-up [18]–[20]. The DCP must provide μA's of current with an input supply voltage that is lower than the V_{th} of DCP charge-transfer switches. However, the switches of the DCP must operate with a low on-state resistance and therefore must be driven at high gate voltages. This is impossible with a conventional DCP design and a very low input supply voltage. To address this issue, the VDL-DCP architecture shown in Fig. 3, is presented in this paper.

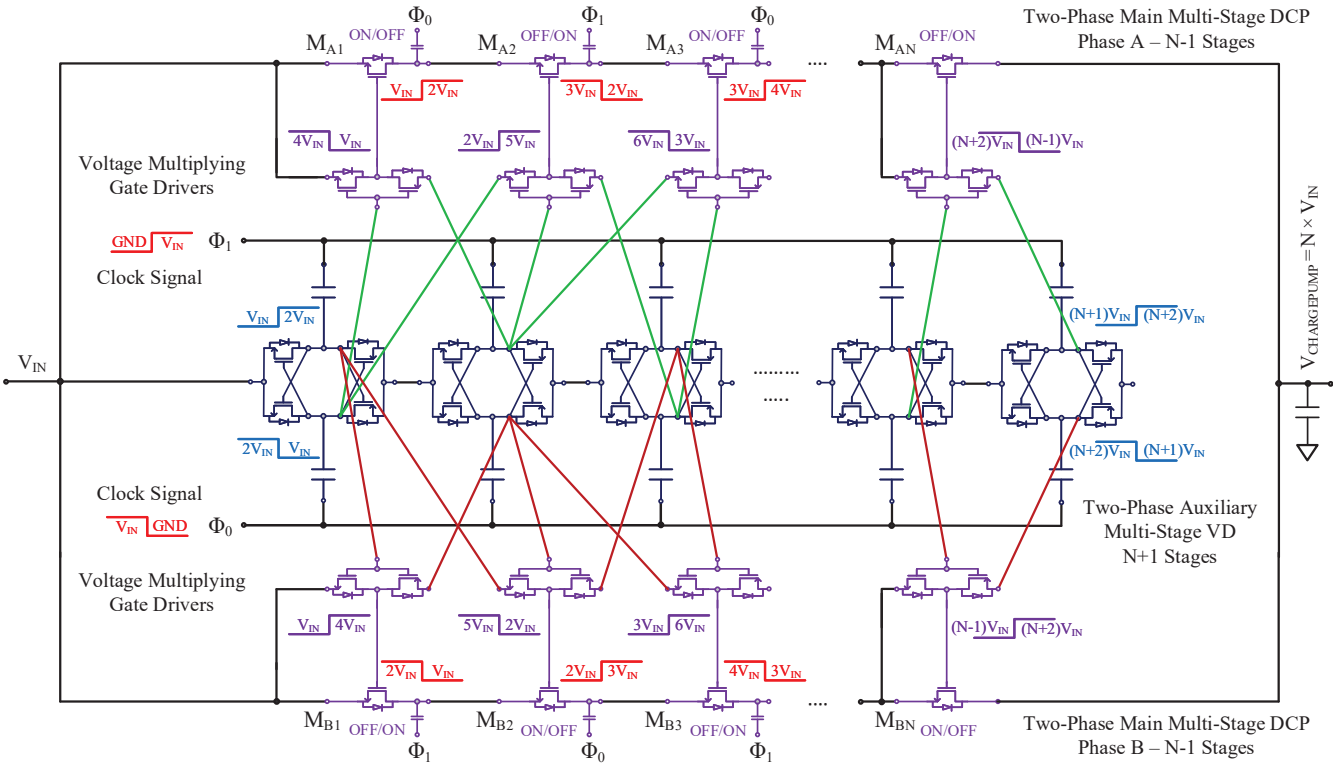


Fig. 3. Schematic of the proposed voltage-doubler-linked Dickson charge pump (VDL-DCP).

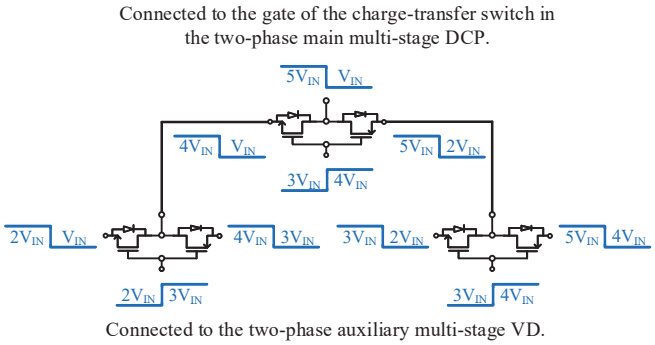


Fig. 4. Schematic of the cascaded driver stages.

Considering charge-pump output voltage of $V_{CHARGEPUMP} = N \times V_{IN}$, the proposed design consists of the following three main building blocks:

a) Two-phase main multi-stage DCP with N-1 stages.
b) Two-phase auxiliary multi-stage VD with N+1 stages.
c) Voltage-multiplying gate drivers to drive DCP switches.

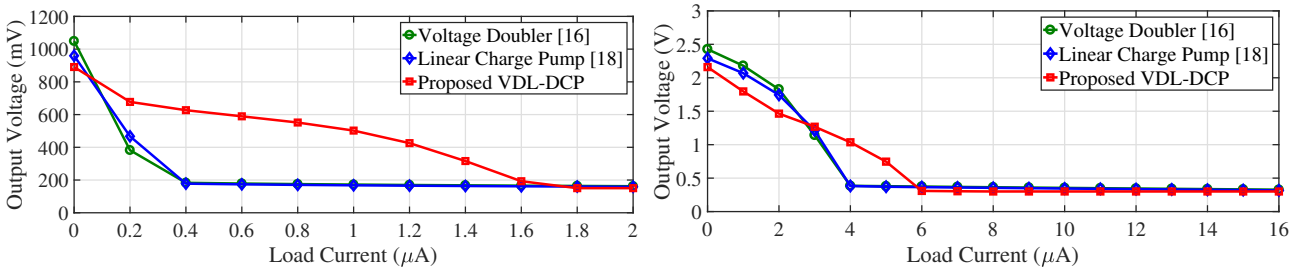
To understand the operation of the three blocks, the steady-state voltages of the unloaded system in the two clock states are depicted in Fig. 3. It should be noted that the system operates with slightly different voltage levels under loaded conditions. The charge pump input voltage is V_{IN} and the charge pump clock signals are Φ_0 and Φ_1, which are typically generated by a free-running oscillator.

The load current is delivered by the two-phase main multi-stage DCP shown in Fig. 3. Each stage of the DCP is (ideally) increasing the output voltage level by the input voltage, V_{IN}. In case of an energy harvesting application, multiple DCP stages have to be placed in series to achieve a sufficiently high output voltage from the available low input voltage.

To improve the efficiency of the DCP, the gates of the NMOS charge-transfer switches are controlled actively through a two-phase auxiliary multi-stage VD as shown in Fig. 3. The cross-coupled VD is only providing gate-drive power for the DCP switches and is supplying a fixed load. Therefore, it can be optimized to create the maximum possible gate drive voltage swing. The number of stages for the auxiliary VD depends on the number of stages in the DCP and the required gate voltage swing. As shown in Fig. 3, for a DCP with N-1 stages and gate voltage swing of $3 \times V_{IN}$, the auxiliary VD requires N+1 stages.

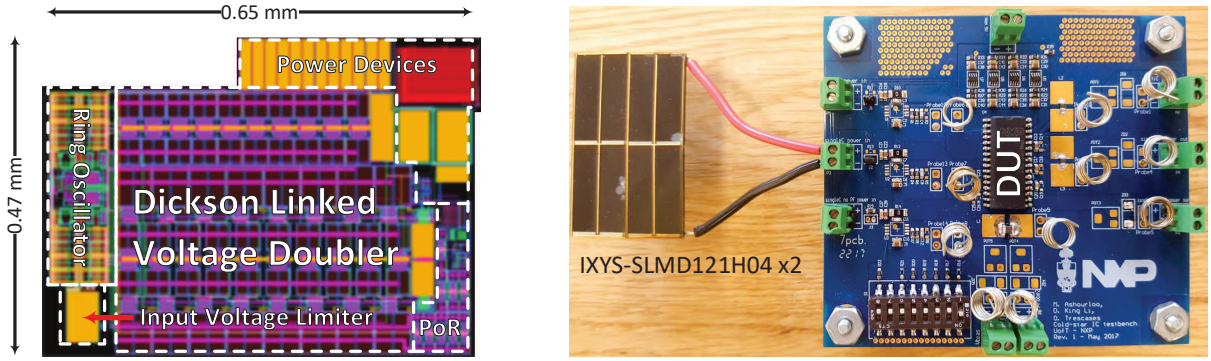
The gate-driver circuit shown in Fig. 3 drives the DCP charge-transfer switches. It combines signals from multiple auxiliary VD stages to maximize the gate voltage swing in the DCP and consequently, maximizing its efficiency at low input voltages of V_{IN}. As shown in Fig. 3, the charge-transfer switches of the DCP are controlled with a gate swing of three times the input voltage, V_{IN}. However, it is possible to cascade the driver stages to increase the gate voltage swing as shown in Fig. 4. In this case, one additional auxiliary VD stage is needed. Therefore, with N-1 DCP stages, N+2 auxiliary VD stages are required.

The simulated performance of the VDL-DCP using a 40-



(a) (b)

Fig. 5. Simulated various SC topologies with input supply voltages of a) 150 mV, and b) 300 mV (oscillator frequency = 1 MHz, total charge pump capacitance = 240 pF, and number of stages = 8).



(a) (b)

Fig. 6. (a) Implemented design in a 40-nm CMOS process, and (b) its experimental test board with solar power input.

nm CMOS process is shown in Figs. 5(a) and 5(b) for 150 mV and 300 mV input supply voltages, respectively. Even with an input voltage as low as 150 mV, the proposed VDL-DCP can provide four times more current than prior arts [16], [18] before its output voltage collapses. Compared to the architectures proposed by [16], [18], the VDL-CP is an all-around improvement for low input voltage applications. Although the proposed architecture requires more area to accommodate the gate drivers, the VDL-DCP achieves a higher power output using the same amount of capacitance, as demonstrated through the simulations.

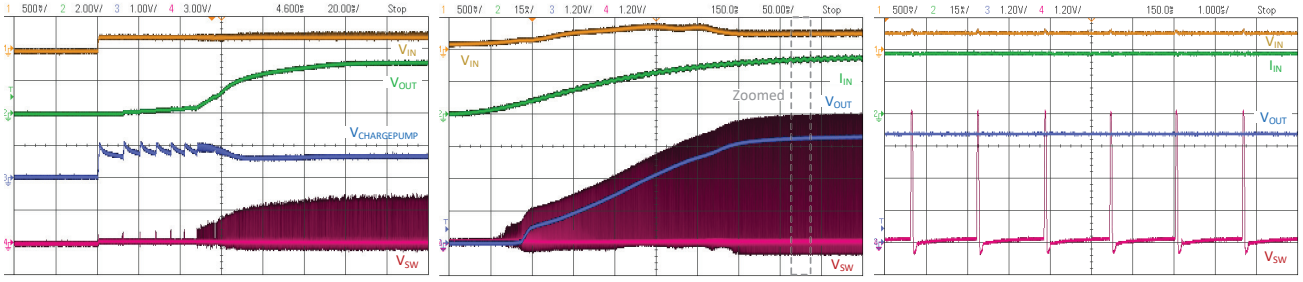
2) *Input Voltage Limiter:* The input voltage limiter is a current shunt circuit that activates whenever the input voltage exceeds the safety threshold of the front-end stage, i.e., 0.8 V in this work. This block is composed of a diode-connected MOSFET in series with a shunt MOSFET whose gate is powered by the output voltage of the charge pump circuit in the front-end stage, as shown in Fig. 2. It is designed to disable the front-end stage (cold-start circuit) once start-up is completed, and allows input voltages as high as 2.4 V to be applied in normal operation.

3) *Back-End Stage:* The back-end stage presented in Fig. 2 is composed of: 1) a power-on-reset (PoR) circuit, 2) a ring oscillator (RO), and 3) an inverter-based gate driver. The PoR circuit is designed to activate the RO when the output of the front-end stage (cold-start circuit) exceeds the threshold needed to properly drive the boost converter's cascoded power MOSFET. Once the back-end-stage RO is activated, the boost converter operates in open loop.

IV. Experimental Results

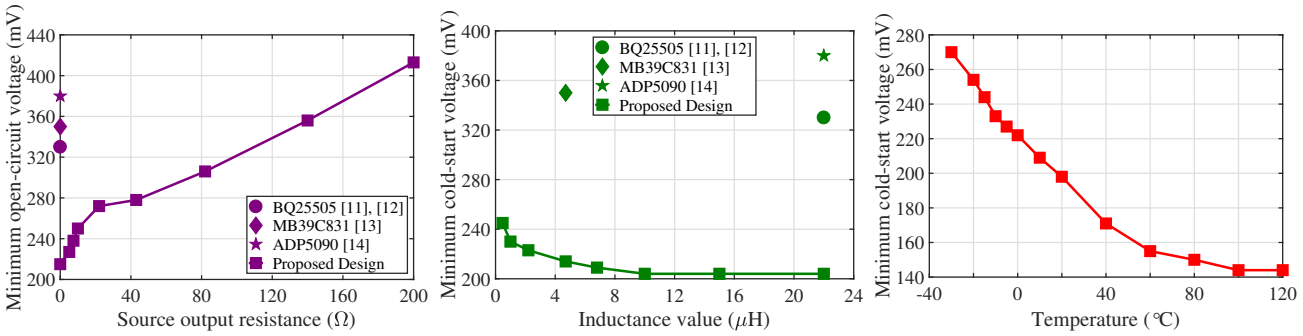
The proposed cold-start circuit integrated with a boost energy harvester has been implemented in a 40-nm CMOS process for future IoT system-on-chip integration. The layout and test board of the fabricated circuit, are shown in Figs. 6(a) and 6(b), respectively. Each DCP and cross-coupled VD stage have been implemented with 13.3 pF and 5.2 pF pumping capacitance, respectively. The performance of the design, measured with an ideal voltage source and solar power inputs, are presented in Fig. 7. After start-up, for output voltages higher than 0.8 V, the closed-loop controller can take over the control of the boost converter, which is beyond the scope of this work.

The performance of a cold-start circuit is most often reported solely based on its minimum cold-start voltage when connected to an ideal voltage source. This figure-of-merit is useful for comparison purposes, however, it fails to capture the real-world performance of the cold-start circuit, since low-voltage energy generators, such as a PV cell or a TEG, have a significant output impedance. Thus, to conduct a more thorough, quantitative evaluation of the proposed design, its performance is investigated for different values of source output resistance, R, as shown in Fig. 8(a). Furthermore, the effect of the inductance value on the minimum cold-start voltage is demonstrated in Fig. 8(b). As expected, the



(a) (b) (c)

Fig. 7. Performance of the proposed cold-start circuit measured for L = 4.7 μH and C_{OUT} = 1 μF: a) with voltage source at a start-up voltage of 220 mV, b) with PV cells at 2.3 V open-circuit voltage and 30 mA short-circuit current, and c) zoomed-in version of (b) after start-up (switching frequency = 640 kHz).



(a) (b) (c)

Fig. 8. Measured dependency of the start-up voltage on: (a) input resistance (L = 4.7 μH, and C_{OUT} = 1 μF), (b) inductance (R = 0 Ω, and C_{OUT} = 1 μF), and (c) temperature (R = 0 Ω, L = 4.7 μH, and C_{OUT} = 1 μF).

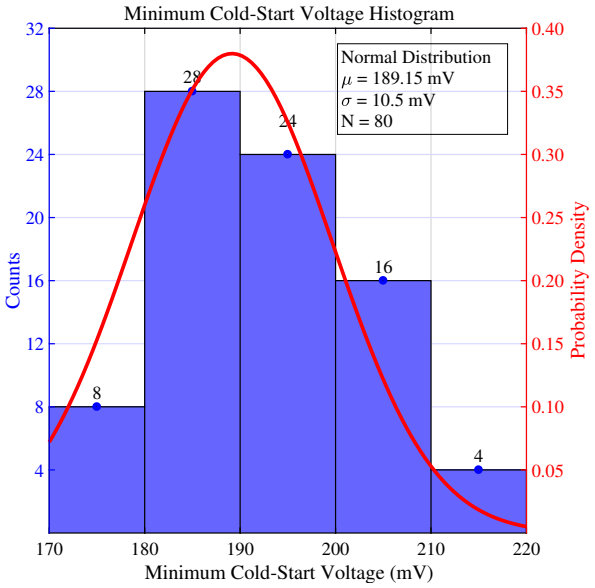


Fig. 9. The statistical distribution of the measured minimum cold-start voltage in 80 samples (R = 0 Ω, L = 4.7 μH, and C_{OUT} = 1 μF).

measurement results show that lower cold-start voltages can be achieved with higher inductance values. As shown in Figs. 8(a) and 8(b), compared to the existing solutions that offer an output voltage range up to 5 V, the proposed design is superior in terms of cold-start voltage and inductance value. The converter start-up voltage ranges from $144-270$ mV, for a temperature range of -30 to 120 °C, as shown in Fig. 8(c). This proves the temperature stability of the design, and is well correlated with the expected sub-threshold operation of the low-V_{th} devices.

The statistical distribution of the measured minimum cold-start voltage for 80 samples is shown in Fig. 9. The measured results revealed that the process variation leads to variations of the minimum cold-start voltage with a mean of 189.15 mV and a standard deviation of 10.5 mV, ranging from a minimum of 170 mV to a maximum of 220 mV.

V. Conclusions

In this paper, a switched-capacitor-based cold-start circuit for dc-dc energy harvesters has been presented. The measurement results for the proposed cold-start circuit integrated with a boost energy harvester in a 40-nm CMOS process reveal that the design can successfully start up from typical input voltages as low as 190 mV, while using a 4.7 μH external inductor. The design offers up to 2.4 V input and 5 V output voltage capability. This new architecture facilitates the implementation of wide-voltage-range, small-form-factor, and low-cost energy harvesters for IoT applications.

ACKNOWLEDGEMENTS

This work was supported by NXP Semiconductors.

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