An improved Analysis method of Loss for the LCLC Multi-Resonant Three-Port Bidirectional DC-DC Converter

Bo chen, Yifeng Wang, Ping Wang, Wei Li, Fuqiang Han, Liang Yang
School of Electrical and Information Engineering
Tianjin University
Tianjin, China
wayif@tju.edu.cn

***Abstract*—In this paper, a new topology of LCLC multi-resonant three-port bidirectional DC-DC converter(MR-TPC) is proposed. It can improve the efficiency and reduce the peak current by introducing 3rd harmonic component of the resonant current. Even at the light-load state, MR-TPC still achieves high efficiency. Besides, an improved loss analysis method is also proposed for the MR-TPC with fully consideration of the influence of 3rd and higher harmonics on the losses, and thus enhances the calculation precision. To verify the theoretical analyses, experiments have been conducted, and the obtained results indicated that (a) the MR-TPC exhibited excellent performance with more than 96% efficiencies among wide load range; (b) the proposed loss analysis method is quite helpful to an accurate evaluation on the loss distribution.**

Keywords—bi-directional DC-DC converter; three-port converter; soft switching; multi-resonant converter; loss distribution;

I. INTRODUCTION

Acting as a significant part of the distributed power generation system, the isolated three port DC-DC converter (TP-BDC) is beneficial for its high efficiency, completely galvanic isolation, and thereby has become a research hotspot presently [1-3]. In [4-7], the triple-active-bridge structure (TAB) is claimed with characteristics of ZVS and bidirectional operation. However, it is only suitable for low frequency applications. This idea is further expanded in [8-10], where the series-resonant three-port-converter (SR-TPC) is proposed. The SR-TPC not only retains all the advantages of TAB, but achieves high power density through promoting operating frequency as well. Unfortunately, its efficiency suffers from progressive reduction at light load. To deal with this deficiency, high order harmonic injection can be a potential solution, where the 3rd or higher order harmonics are employed to deliver active powers. Whereas, few literatures have utilized this technology into the TP-BDC.

Loss analysis is of great importance due to its guiding significance for the efficiency estimation and magnetic design. However, the conventional loss analysis only concerns the influence of 1st harmonic, while the impacts of higher order harmonics are neglected. Consequently, considerable deviation will be introduced in the case of the high order harmonic injection, which has not been focused among current papers [11-12].

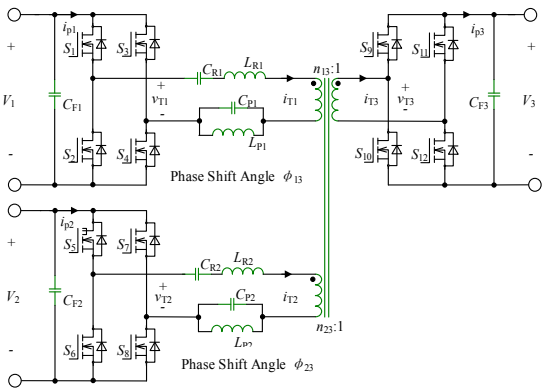


Fig. 1. The topology structure of MR-TPC.

In this paper, a new topology of MR-TPC is proposed as shown in Fig.1. It can transfer 1st and 3rd harmonic power simultaneously and thus reduces the peak current, which presents elevated efficiency and broadened ZVS range among full load range. Moreover, an improved method of loss analysis is established, which enhances the calculation accuracy. At last, experimental results are also presented and verified the feasibility of the theoretical analyses.

II. OPERATION PRINCIPLE

The resonant structures of SR-TPC and MR-TPC are shown in Fig.2, respectively. The resonant cavity of SR-TPC consists of two resonant elements with one resonant frequency f_r. While, in MR-TPC, the resonant cavity is composed by 4 resonant elements with three resonant frequencies f_r, f_{r2}, f_{r3}. The parallel resonant frequency of L_{P1} and C_{P1} is defined as f_{r2}; f_r and f_{r3} represent the other two series resonant frequencies. And the parameters of resonant elements must be designed seriously to meet the requirements of $f_{r2}=2f_r$, $f_{r3}=3f_r$. In this way, both 1st and 3rd harmonic power can be transferred through the resonant tank. Besides, owing to the superposition of the two order harmonic powers, the resonant current presents the saddle-shaped waveform as shown in Fig.3.

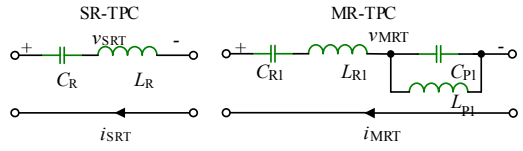


Fig. 2. Resonant structure of MR-TPC and SR-TPC

Compared to SR-TPC, the 3rd frequency component is introduced in MR-TPC, so that the power circulation resulting from the high frequency component of the square wave voltage and the resonant current is reduced. Thus, MR-TPC can reduce the loss of conduction, contributing higher efficiency. In addition, due to the superposition of 3rd frequency component, peak value of the resonant current has been reduced effectively, which can reduce the demand for current stress. At the same time, the range of ZVS is widened by MR-TPC.

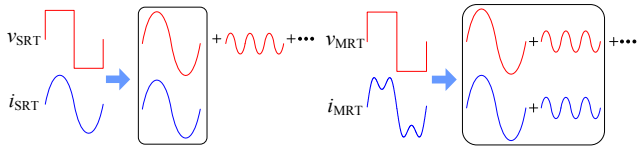


Fig. 3. Resonant current of MR-TPC and SR-TPC

III. Power Loss Modeling

A. Loss of switch

As the main part of the loss in the converter, the calculation of the switching loss is relatively complicated. Switching loss can be divided into conduction loss P_{sw_con}, reverse conduction loss P_{sw_SD}, output capacitor loss P_{sw_oss}, turn-off/on loss $P_{sw\_on/off}$ and drive loss P_{sw_G}, as shown in (1).

$$P_{sw} = P_{sw\_oss} + P_{sw\_SD} + P_{sw\_con} + P_{sw\_G} + P_{sw\_on/off} \quad (1)$$

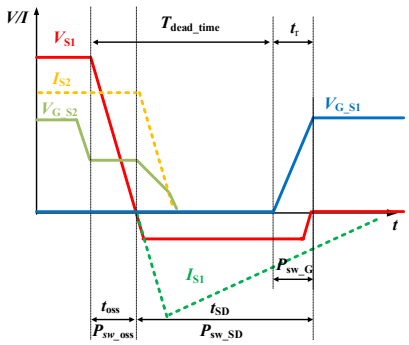


Fig. 4. Waveforms during the turn-on transition

The voltage and current waveforms of switch S1 and S2 during the turn-on transition are shown in Fig. 4. In Fig.4, v_{S1} represents the drain-source voltage of S1; v_{G_S1} and v_{G_S2} are the gate voltages of S1 and S2; V_{pl} is defined as the Miller platform voltage. i_{S1} and i_{S2} are the current flowing through the switches; t_{db} means the dead band time; t_r and t_{oss} represent the gate voltage rise time and the output capacitance discharge time of the switch; t_{SD} is defined as reverse conduction time.

At first, S_2 turns off and then v_{G_S2} begins to drop until it reaching V_{pl}, the output capacitor C_{oss} of S1 starts to discharge as C_{oss} of S2 begins to charge. Meanwhile, v_{S1} steady declines, while v_{S2} is increasing during this period. In order to ensure ZVS implementation, v_{S1} must be reduced to 0 before S1 receiving the trigger sign, namely the v_{G_S1} is high level. As stated in the [31], t_{oss} is described as (2), where I_{off} is turn-off current; Q_{S1} and Q_{S2} are the output charge of S_1 and S_2:

$$t_{oss} = \frac{Q_{S1} + Q_{S2}}{I_{off}} \quad (2)$$

If $t_{oss} < t_{db}$, the ZVS will be achieved and the corresponding losses P_{sw_on} and P_{sw_oss} can be avoided. In contrast, when $t_{oss} > t_{db}$, P_{sw_on} and P_{sw_oss} cannot be removed, which will damage to overall efficiency of converter and they are calculated as follow:

$$P_{sw\_oss} = f_{sw} \cdot \int_0^{V_{in}} v_{DS} C_{oss}(v_{DS}) \mathrm{d}v_{DS} \quad (3)$$

$$P_{sw\_on} = f_{sw} \cdot \int_0^{t_x} v_{DS}(t) i_{DS}(t) \mathrm{d}t \quad (4)$$

Where, i_{DS} and v_{DS} are the current and drain-source voltage of switch during the turn-on transition; t_x means the overlap time between v_{DS} and i_{DS}; C_{oss} is defined as the output capacitance value, and the nonlinear relationship between C_{oss} and v_{DS} is exhibited in Fig.5 as the datasheet described. Thus, the method of piecewise integral is used to obtain the more precise results.

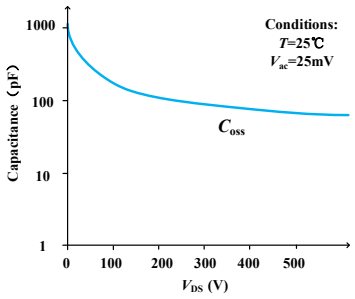


Fig. 5. Nonlinear curve between C_{oss} and V_{DS}.

With v_{S1} down to 0, I_{S1} starts to run through body diode of S1 until its driving signal arriving. During this period, a reverse voltage is resulted as the current flow through the body diode, leading to P_{sw_SD}, as the (5) shown. Where, turn-on voltage of diode V_{SD} can be checked from the datasheet of switch, and the time of reverse conduction t_{SD} can be calculated by t_{oss}, t_{db} and t_r:

$$P_{sw\_SD} = f_{sw} \cdot \int_0^{t_{SD}} V_{SD}(t) i_{SD}(t) \mathrm{d}t_{SD} \quad (5)$$

Also, during the turn-off transition, it is necessary to guarantee that current flowing through the body diode leads the gate driving signal arrival of S1. So, ZVS can be realized as the Fig.4 shown. And, the Miller platform does not exist during the turn-on transition of S1 due to ZVS condition. Meanwhile, the switch drive loss P_{sw_G} is also an ignored part of switch loss, which can be expressed as (6) with the ZVS condition.

$$P_{sw\_G} = f_{sw} V_{GS} \left(Q_G - Q_{GD} \right) \tag{6}$$

Where, Q_G is the charge required for gate conduction, and Q_{GD} is the charge required for Miller platform. However, in this study and experiments, an additional auxiliary power supply is employed as the driving power for experiments. Therefore, the corresponding loss P_{sw_G} is not involved in the analysis of efficiency and loss.

For P_{sw_con}, the conventional calculation method is no more satisfied for MR-TPC, since it only concerns the effect of the fundamental component, and ignores the effect of higher order harmonics. However, the loss caused by the superposition of the 3rd harmonics and higher order harmonics will become an indispensable part of the total loss. To make the calculation more accurate, P_{tra_cu} is calculated by summing the losses from 1st to 28th harmonics. Therefore, the improved calculation method is proposed for P_{sw_con}, shown as:

$$P_{sw\_con} = \sum_{n=1}^{28} I_n^2 R_{ds} \tag{7}$$

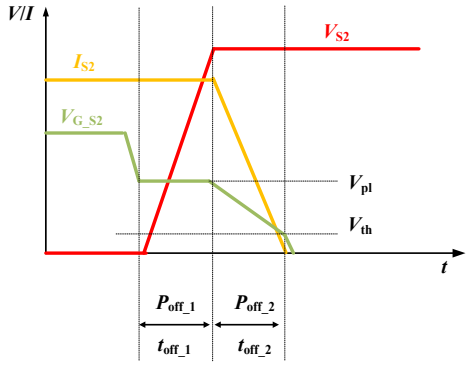


Fig. 6. Waveforms during the turn-off transition

Similar to the turn-on transition, the corresponding voltage and current waveforms during the turn-off transition of the converter is also given as Fig.6 exhibited. In this picture, v_{S2} represents the source-drain voltage of S2, V_{th} is defined as the gate threshold voltage of the switch. Unfortunately, the P_{sw_off} cannot be avoided. And this part of the loss becomes the most important factor affecting the efficiency of the converter. Therefore, in order to accurately calculate this part losses, P_{sw_off} is divided into two parts [13]. In part one, i_{S2} keeps constant, while v_{S2} increases linearly during the time, t_{off1}. In part two, v_{S2} keeps constant, while i_{S2} decreasing linearly in t_{off2}. As a result, P_{sw_off} can be expressed as:

$$P_{off} = \frac{f_{sw} I_{off} V_{in}}{2} (t_{off1} + t_{off2}) \tag{8}$$

$$t_{off1} = \frac{Q_{GD} R_{Goff}}{V_{pl}} \quad , \quad t_{off2} = \frac{Q_{GS} (R_{Goff} + R_{s1})}{\left(V_{pl} + V_{th} \right) / 2} \tag{9}$$

Where Q_{GS} is the storage charge between the gate and source; R_{sl} and R_G represent the source equivalent series impedance and the gate equivalent impedance respectively.

B. *Loss of transformer*

The loss of transformer P_{tra} can be generally divided into core loss P_{tra_core} and copper loss P_{tra_cu}. And, P_{tra_core} is estimated by the Steinmetz equation [14], written as:

$$P_{core\_tra} = k V_{eq} f_{sw}^{\alpha} B_{max}^{\beta} \quad , \quad B_{max} = \frac{I_{max} L_m}{2 n_{lp} A_{eq}} \tag{10}$$

P_{tra_cu} of transformer is produced by windings. In this part, the 3rd harmonic also contributes a great influence on P_{tra_cu}, which can be not ignored. On the other hand, the skin effect and proximity effect need be considered, because the AC equivalent resistance R_{ac} is larger than its DC resistance R_{dc}. Thus, the Dowell equation is used, and AC-to-DC resistance ratio at the n harmonic frequency is given [15-16]. The P_{tra_cu} can be rewritten as:

$$P_{cu\_tra} = R \sum_{n=0}^{28} FR \cdot I_n^2 \tag{11}$$

$$FR(n, p, x) = x \cdot \frac{e^{2x} - e^{-2x} + 2\sin(2x)}{e^{2x} + e^{-2x} + 2\cos(2x)} + 2x \cdot \frac{p^2 - 1}{3} \cdot \frac{e^{x} - e^{-x} + 2\sin(x)}{e^{x} + e^{-x} + 2\cos(x)} \tag{12}$$

Where p is defined as the number of layers in magnetic component winding; x is an intermediate variable and described as (13), in which the foil is used as the coil in this study and experiments. h_{foil} represents the thickness of the foil; $\delta(n)$ means the skin depth of n^{th} harmonics frequency.

$$x = \frac{h_{foil}}{2\delta(n)}, \quad \delta(n) = \sqrt{\frac{2\rho_{Cu}}{2\pi n f_{sw} \mu_0}} \tag{13}$$

C. *Others*

For the core loss of inductance P_{L_core}, the calculation method is like P_{tra_core}. The influence of 3rd harmonics should also be considered for inductance and capacitance when dealing with P_{L_cu} and P_c. They can be calculated as:

$$P_{L\_cu} = R_L \sum_{n=0}^{28} FR \cdot I_{L\_n}^2 \tag{14}$$

$$P_{Cr} = \sum I_{C\_n}^2 \cdot \frac{\tan(\delta)}{2\pi f_{sw} C_r} \tag{15}$$

Where, tan(δ) represents the dissipation coefficient of capacitance, which can be found from the datasheet.

IV. LOSS ANALYSIS FOR SR-TPC AND MR-TPC

Based on the above analysis, theoretical calculations are carried out for MR-TPC and SR-TPC in the conditions of 1000W, 500W. The parameters of MR-TPC and SR-TPC are summarized in Table I for both theoretical analysis and experiments. The dead band time t_{db} is set to 150ns.

TABLE I. THE PARAMETERS OF MR-TPC AND SR-TPC

Component	MR-TPC	SR-TPC
Switch	SiC MOSFET	
Transformer	Core:EE85*2, n(BUS:BAT:SC)=14:5.25:7	
Inductance	L_r= 34u, L_p =31.87u	L_r =127.5u
Capacitance	C_r=37n, C_p=22n	C_r=22n

A. 1000 W Output Condition

In the condition of 1000W, the phase-shift control strategy is adopted, and f_{sw} is set to 110 kHz. By this way, the corresponding loss distribution is given based on the theoretical analysis mentioned above, as shown in Fig.7. As the picture described, MR-TPC realized ZVS while SR-TPC did not. This is possibly attributed to that the superposition of 3rd harmonic current increase I_{off} so that the charging and discharging of C_{oss} can be completed in t_{db}. In addition, introduction of 3rd harmonic current reduces the peak current, which will alleviate the loss caused by core of magnet and inductance. Since ZVS is realized, P_{sw_on} and P_{sw_oss} are 0 for MR-TPC, while they are unavoidable for SR-TPC as f_{sw} is set to 110 kHz. P_{sw_off} has become the main factor affecting the efficiency. But MR-TPC causes more losses in P_{sw_off} than SR-TPC because MR-TPC has higher I_{off} with 3rd harmonic current superposition. Fortunately, the 3rd harmonic current introduction also brings the optimized effects in the parts of P_{tra_core}, P_L and ZVS realized range. As MR-TPC can achieve ZVS when f_{sw} is set to 110 kHz, the f_{sw} must be lifted to 125 kHz and ZVS can be harvested for SR-TPC. However, the price is that the higher frequency reduces the overall efficiency of the converter.

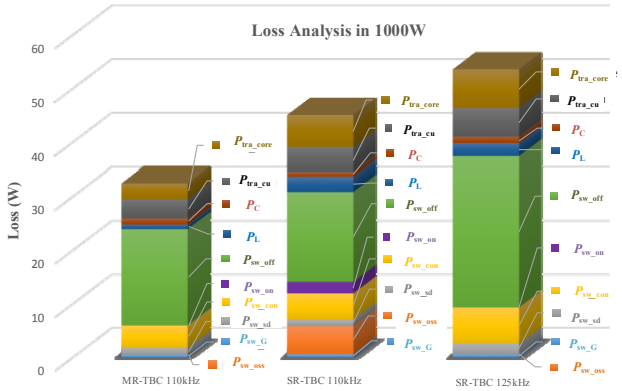


Fig. 7. Loss calculation of MR-TPC and SR-TPC under 1000 W

As a result, in the case of 1000 W, MR-TPC has better efficiency and wider ZVS range than SR-TPC due to the introduction of 3rd harmonic current.

B. 500 W Output Condition

In 500W, with I_{off} decreasing, and the condition of realizing ZVS becomes more severe. To obtain higher I_{off}, the f_{sw} need be increased. When f_{sw} is equal to 145 kHz, ZVS can be achieved by MR-TPC, while SR-TPC need more than 160 kHz. Unfortunately, efficiency would be sacrificed if f_{sw} is set to 145 kHz. In contrast, although ZVS cannot be acquired for the MR-TPC with f_{sw}=130 kHz, the C_{oss} discharge is almost completed. And it can be regarded as the quasi ZVS. So, the loss analysis is implemented in the situation of 130 kHz and 150 kHz by the SR-TPC and MR-TPC, as shown in Fig. 8.

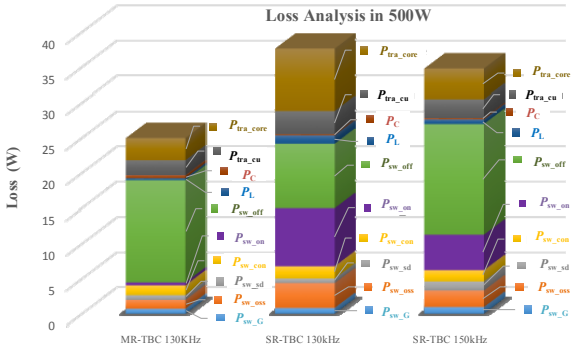


Fig. 8. Loss calculation of MR-TPC and SR-TPC under 500 W

As Fig.8 described, P_{sw_on} is unavoidable in the three situations. However, when f_{sw} is set to 130 kHz, P_{sw_on} generated by MR-TPC is limited and smaller than SR-TPC. This is attributed to larger I_{off} and the quasi ZVS, contributing to better P_{sw_on} and P_{sw_oss}. However, similar to the case of 1000 W, with the superposition of 3rd harmonic current, the MR-TPC also caused more turn-off loss and P_{sw_off} is more severe than SR-TPC at the same f_{sw}. This is another research target which need to be prefect in the future. Fortunately, MR-TPC has a better improvement effect in the other parts as a trade-off such as P_{tra}, P_L and P_{sw_oss}. And, the MR-TPC has harvested a better overall efficiency, compared to SR-TPC.

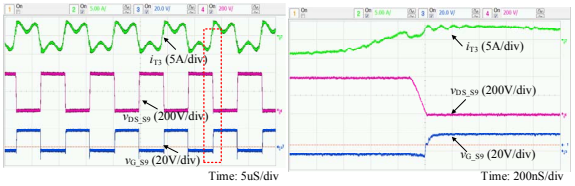
As the results of theoretical analysis shown under two cases, although MR-TPC causes more turn-off losses by the introduction of 3rd harmonic current, MR-TPC harvests palmary overall efficiency and widen ZVS range.

V. EXPRIMENTAL RESULTS

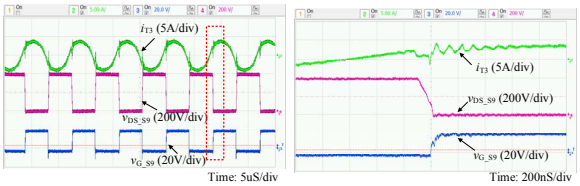
In order to prove the precise of theoretical calculation, 1000W prototypes of MR-TPC and SR-TPC are built. And the corresponding experiments of 1000W and 500W are implemented.

A. 1000 W Output Condition

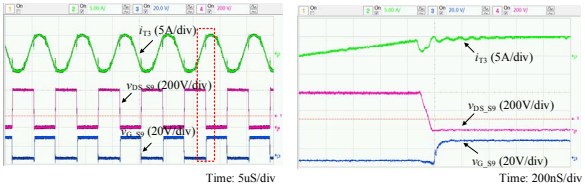
Consistent with theoretical analysis, the working frequency f_{sw} is set to 110 kHz for MR-TPC, while 110 kHz and 125kHz for SR-TPC. And the experimental waveforms are exhibited as shown in Fig.9, and the right figure is the enlarged view of the red dash part of the left picture.



(a) MR-TPC 110kHz



(b) SR-TPC 110kHz



(c) SR-TPC 125kHz

Fig. 9. Experimental results of MR-TPC and SR-TPC under 1000 W.

As the pictures shown, ZVS are realized in case (a) and (c). And, the resonant current show saddle-shaped for MR-TPC while it presents sinusoidal SR-TPC. These phenomena are consistent with the results of theoretical analysis. Besides, benefit from introduction of 3rd harmonic function, the peak of resonant current is constraint for MR-TPC which is 4.17A, while it is 4.42A in SR-TPC. This will cause different losses in P_{tra} and P_L as the analysis mentioned above. Besides, the traditional and improved analysis methods are provided in Fig.10 shown. As a result, the efficiency is calculated as 97.15% used by traditional methods and the deviation is 1.1%. The accuracy of the new method increased by 0.5 %. And the efficiency calculation and experimental results are shown in TABLE II.

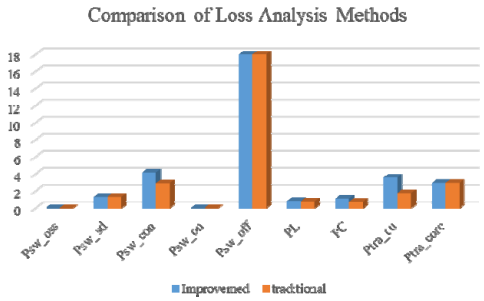


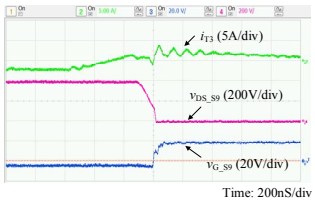
Fig. 10. Comparsion of Loss Analysis Methods

TABLE II. EFFICIENCY BETWEEN MR-TPC AND SR-TPC IN 1000 W

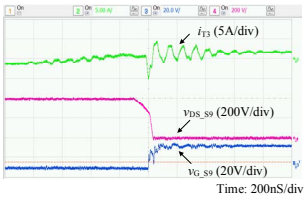
Prototype	Experiment Efficiency	Calculation Efficiency	Deviation
MR-TPC 110kHz	96.08%	96.75%	0.67%
SR-TPC 110kHz	95.17%	95.66%	0.49%
SR-TPC 125kHz	93%	94.7%	1.7%

B. 500 W Output Condition

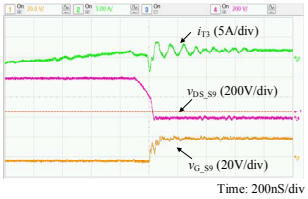
In the experiments of 500 W, based on the analysis above, 130 kHz is selected as the f_{sw} for MR-TPC and 130 kHz and 150 kHz are adopted for SR-TPC as references. The corresponding waveforms of BUS ports are shown in Fig 11.



(a) MR-TPC 130kHz



(b) SR-TPC 130kHz



(c) SR-TPC 150kHz

Fig. 11. Experimental results of MR-TPC and SR-TPC under 500 W.

As Fig.11 described, ZVS are not achieved in three groups of experiments. But, the current oscillation in the (a) is much smaller than the others. This is consistent with the theoretical analysis, which i_{off} of MR-TPC is larger and the quasi ZVS is realized, contributing in limited P_{sw_on} and P_{oss}. On the other hand, a fierce current oscillation also adversely affects transformers and inductors, leading to extra loss. The efficiency of 3 groups is shown in TABLE II. And the accuracy has been increased by 0.88% from 96.02% to 95.14% by the new calculation method.

TABLE III. EFFICIENCY BETWEEN MR-TPC AND SR-TPC IN 500 W

Prototype	Experiment Efficiency	Calculation Efficiency	Deviation
MR-TPC 130kHz	94.45%	95.14%	0.69%
SR-TPC 130kHz	91.67%	92.82%	1.15%
SR-TPC 150kHz	93%	93.52%	0.52%

CONCLUSION

In this paper, a topology of MR-TPC is proposed, which can transfer both 1st and 3rd harmonic energy. By this way, higher efficiency can be harvested in full load rang, and the broaden range of ZVS is achieve. In addition, the converter can decrease the peak current, which reduced the demand for current stress and relieved the loss of magnet. At the same time, an improved loss analysis method is discussed. By the new method, the effect of higher harmonics on efficiency is considered, and a better precision is acquired. In the end, the experiments of 1000W and 500W are implemented to verify the accuracy of the theory. And the performance of MR-TPC is also be proved through experiments, whose highest efficiency can reach 96.08% at 1000W, and 94.45% at 500W.

References

[1] Song, Y., and Wang, B., "Survey on reliability of power electronic systems," *IEEE Trans. on Power Electron.*, vol. 28, no.1, pp. 591-604, 2013.

[2] Yang, S., Bryant, A., Mawby, P., Xiang, D., Ran, L., Tavner, P., "An industry-based survey of reliability in power electronic converters." *IEEE Transactions on Industry Applications*, vol. 47, no. 3, pp. 1441-1451, 2009.

[3] Cheng-Shan Wang, Wei Li, Yi-Feng Wang, Fu-Qiang Han, & Bo Chen, "A high-efficiency isolated LCLC multi-resonant three-port bidirectional dc-dc converter," *Energies,* vol.10*,* no.7, pp. 934, 2017.

[4] Duarte, J.L., Hendrix, M., Simões, M.G., "Three-Port Bidirectional Converter for Hybrid Fuel Cell Systems," *IEEE Trans Power Electron*, vol. 22 no. 2, pp. 480-487, 2007.

[5] Fontana, C., Buja, G., Bertoluzzo, M., Kumar, K., & Wang, Q., "Power and control characteristics of an isolated three-port DC-DC converter under DCM operations," *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, pp.4211-4216, 2016.

[6] Wang, L., Wang, Z., Li, H, "Asymmetrical Duty Cycle Control and Decoupled Power Flow Design of a Three-port Bidirectional DC-DC Converter for Fuel Cell Vehicle Application." *IEEE Trans. Power Electron*, vol. 27, no. 2, pp. 891-904, 2012.

[7] Ling, Z., Wang, H., Yan, K., & Gan, J. "Optimal isolation control of three-port active converters as a combined charger for electric vehicles," *Energies,* vol. 9*,* no. 9, pp.715, 2016.

[8] Li, X., Bhat, A.K.S, "Analysis and Design of High-Frequency Isolated Duan-Bridge Series Resonant DC/DC Converter," *IEEE Trans Power Electron.*, vol. 25, no. 4, pp. 850–862, Chennai, India 2010.

[9] Krishnaswami, H., Mohan, N., "Three-Port Series-Resonant DC-DC Converter to Interface Renewable Energy Sources with Bidirectional Load and Energy Storage Ports," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2289–2297, 2010.

[10] Shreelekha, K., Arulmozhi, S., "Multiport Isolated Bidirectional DC-DC Converter Interfacing Battery and Supercapacitor for Hybrid Energy Storage Application," *International Conference on Electrical, Electronics, and Optimization Techiniques*, pp. 2763-2768, 2016.

[11] Piris-Botalla, L., Oggier, G. G., Airabella, A. M., & García, G. O., "Analysis and evaluation of power switch losses for three-port bidirectional DC-DC converter," *IEEE International Conference on Industrial Technology* pp. 950-955, 2012.

[12] Itoh, K., Inoue, S., Ishigaki, M., & Sugiyama, T., "Loss estimation of an isolated three-port DC-DC converter for automotive applications," *Energy Conversion Congress and Exposition,* pp. 3667-3673, 2015.

[13] Guan, Y., Wang, Y., Xu, D., & Wang, W., "A 1 MHz half-bridge resonant dc/dc converter based on GAN FETs and planar magnetics," *IEEE Trans. Power Electron.*, vol. 32 no. 4, pp. 2876-2891, 2017.

[14] C. P. Steinmetz, "On the law of hysteresis," *Trans. AIEE*, vol. 9, pp. 3–64, 1892.

[15] J. A. Ferreira, "Improved analytical modeling of conductive losses in magnetic components," *IEEE Trans. Power Electron.*, vol. 9, no. 1, pp. 127–131, Jan. 1994.

[16] Yu, R., Ho, G. K. Y., Pong, B. M. H., Ling, W. K., & Lam, J, "Computer-aided design and optimization of high-efficiency LLC series resonant converter," *IEEE Trans. Power Electron*, vol. 27, no. 7, pp. 3243-3256, 2012.