Light-Load Efficiency Improvement for LLC Converter with Synchronous Rectification in Solid-State Transformer Application

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***Abstract*—Synchronous rectification technique can reduce secondary-side conduction loss of the LLC resonant converter. Typically, the control of synchronous rectifier (SR) relies on either voltage or current information; however, the detection circuit is sensitive to parasitic effects and high frequency noises. Since reliability is among top priorities in solid-state transformer application, open-loop controlled scheme becomes advantageous. Unfortunately, secondary-side current of LLC converter reaches zero-crossing-point (ZCP) earlier at light-load condition and the SR signal could turn off after ZCP. In that case, high circulating current appears in the secondary side and dramatically deteriorate efficiency. Therefore, a tuning method utilizing external primary-side output capacitor and dead-time extension is proposed to avoid late turn-off issue of open-loop controlled scheme. In this paper, the cause of ZCP shifting and late turn-off issue are explained first. Then a model for dead-time transient of LLC converter is derived as the theoretical basis of proposed tuning method. Finally, hardware testing results of a 4-kW LLC converter module are presented. With the proposed tuning method, the open-loop controlled synchronous rectification can improve the efficiency of the LLC converter module even at light-load condition.**

Keywords—LLC converter; synchronous rectifier; parasitic output capacitance; solid-state transformer

I. INTRODUCTION

The initial concept of solid-state transformer (SST) was to replace the conventional bulky and high-costed ac-to-ac transformer [1]. In medium voltage (MV) level, semiconductor devices with high voltage-blocking capability suffers from either low switching speed or serious switching noises [2]-[5]. As an alternative, one can cascade multiple converters to use relatively low-voltage devices instead [6]-[8]. The MV SST developed in Future Energy Electronics Center [8] consists of the following stages: (1) 3-level ac-dc boost converters in series configuration to handle MV front-end and correct power factor, (2) isolated dc-dc converters in parallel configuration to step down voltage and (3) a single-phase dc-ac inverter. Fig. 1 is the entire system configuration and Fig. 2 is the individual power module circuit.

The dc-dc stage in [8] is realized by LLC resonant converter, as depicted in Fig. 3(a), because of its galvanic isolation, high efficiency and capability of high-frequency operation [8]-[9]. However, traditional unidirectional LLC converter rectifies current through secondary-side diodes that generate large conduction loss. The loss breakdown of LLC

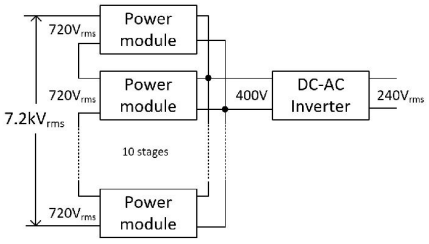


Fig. 1. System configuration of the SST in [8].

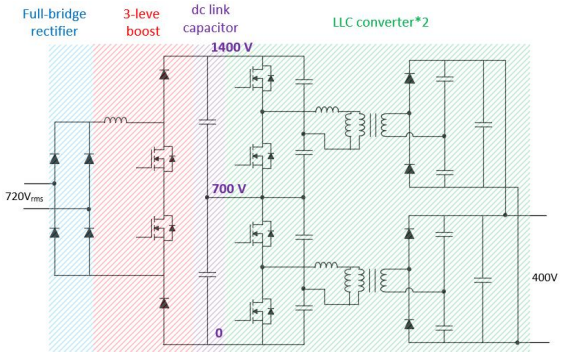
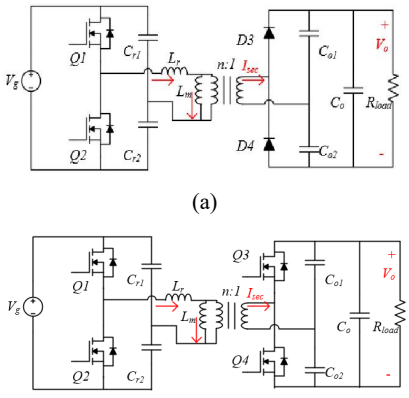


Fig. 2. Power module circuit.



(a)

(b)

Fig. 3. LLC converter: (a) without SR and (b) with SR.

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converter in [8] under nominal output power is illustrated in Fig. 4 and shows that about half of power loss is attributed to conduction loss of silicon diode rectifier.

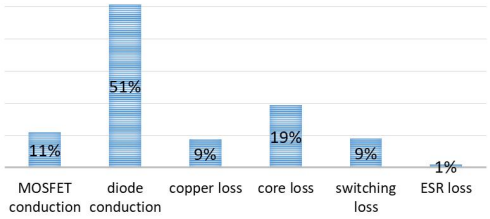

Fig. 4. Loss breakdown of LLC converter in 2.5-kW power module testing.

To reduce rectifier conduction loss of LLC converter, synchronous rectifier (SR) technique is widely used especially in low-output-voltage applications [10]-[13]. SRs are semiconductor switches with low on-resistance that take place of rectifier diode. Fig. 3(b) shows the circuit diagram of LLC converter in [8] after applying SRs. It is common that SR requires sensing circuit, for example, in the self-driven scheme utilizing V_{DS} of SRs [10]-[11] or drain current of SRs [13]. However, cycle-by-cycle SR control using detection circuit is not preferred because parasitic components, switching noises, electromagnetic interference and other non-ideal effect could degrade the reliability, which is among top priorities of a SST. Consequently, external driven method with open-loop signals is chosen instead. Fig. 5 shows the block diagram of the external driven method where SR control signals and primary-side control signals are isolated by fiber optics. Since device gate signals shown in Fig. 6 is open-loop-controlled, sensing circuit is not necessary.

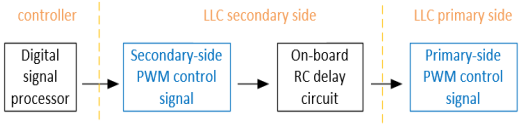

Fig. 5. External driven method.

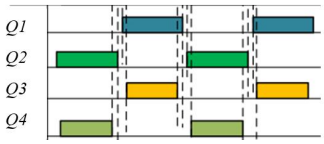

Fig. 6. Device gate signals.

In [8], LLC converter operates in region II [14] to avoid primary device turn-off loss, secondary rectifier hard commutation and obtain zero-voltage-switching (ZVS) [15]. Since switching frequency f_s is below series resonant frequency f_r, secondary-side current I_{sec} reaches zero-crossing-point (ZCP) at the end of power delivery stage, as shown in Fig. 7. The ZCP appears earlier at light-load condition; however, open-loop SR signals remain the same throughout entire load range. As a result, SR could be turned off after ZCP and allow high circulating current flowing, which is named as late turn-off issue.

The detailed mechanism for late turn-off issue is discussed in Section II. Then a tuning method is proposed in Section III to solve the problem. Section IV shows experimental results tested through a power module. Finally, Section V concludes the paper.

$$n(I_{Lr} - I_{Lm}) = I_{sec} \tag{1}$$

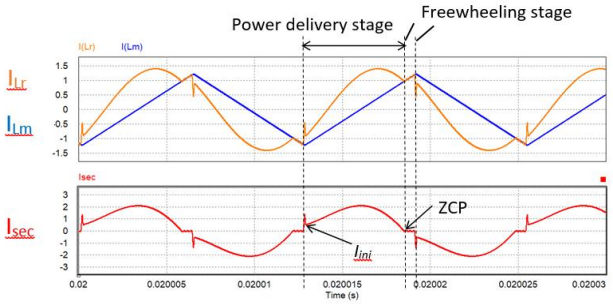

Fig. 7. Simulated steady-state current waveforms of LLC converter without SR ($f_s < f_r$).

II. Problem Statement

A. Zero-Crossing-Point Shifting

In Fig. 7, resonant current I_{Lr} follows magnetizing current I_{Lm} within freewheeling stage and I_{sec} is zero. Ideally, I_{sec} should also be zero at the beginning of the power delivery stage. However, output capacitance (C_{oss}) of devices has to be charged/discharged for turn-off/turn-on. Therefore, resonance appears within the dead-time of primary devices. The resonance affects the initial current I_{ini} for the power delivery stage.

From Fig. 8, I_{Lr} in the power delivery stage is a sinusoidal waveform with resonant frequency shown in (2). Since I_{Lm} is only controlled by the voltage-second of the transformer, according to (1), I_{Lr} has larger initial phase angle when I_{ini} is higher. As a result, I_{Lr} meets I_{Lm} in the power delivery stage earlier, which advances the ZCP of I_{sec}. The shifting of ZCP is illustrated in Fig. 9. Another way to understand ZCP shifting is by directly looking at I_{sec}. After rectifying, the mean of I_{sec} equals to output current I_o. In general, instantaneous I_{sec} becomes larger when I_{ini} gets higher. Therefore, conduction time is shortened and ZCP shows up early.

Under light-load condition, the ratio I_{ini}/I_o is greater, which implies the initial phase angle caused by I_{ini} is greater as well. Consequently, ZCP shifting is even more severe.

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2}$$

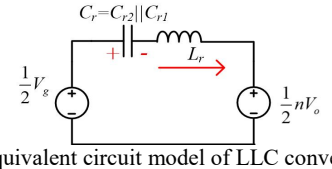

Fig. 8. Equivalent circuit model of LLC converter in the power delivery stage.

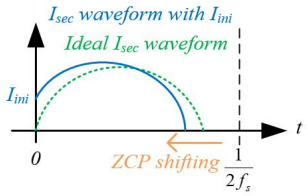

Fig. 9. Zero-crossing-point (ZCP) shifting.

B. Late Turn-Off Issue

ZCP shifting becomes an issue when SR with open-loop control is applied. Unlike the case using diode rectifier, SR allows I_{sec} flows into the other direction after ZCP. So if SR is not turned off before ZCP, energy will be transferred from the load back to the LLC converter, which generates large circulating energy and extra conduction loss. In addition, if one curtails on-time of the SRs to avoid late turn-off issue at light-load, then the benefit of SR declines at heavy-load. Therefore, a fundamental solution that reduces I_{ini} is preferred.

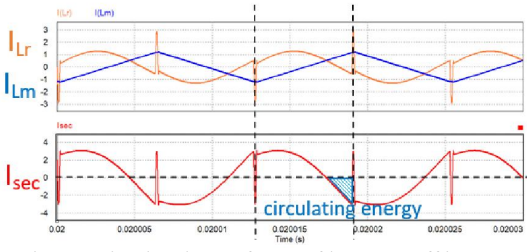

Fig. 10. Simulated waveforms of late turn-off issue.

III. Time-Domain Analysis and Tuning Method

To resolve late turn-off issue, the cause of I_{ini} should be analyzed in details. To begin with, the C_{oss} of the devices should be considered. C_{oss} affects voltage gain and ZVS of a resonant converter [16]-[18]. In [18], the transient analysis within dead-time is performed but only simplified results in terms of ZVS are provided. Fig. 11 shows experimental waveforms illustrating the transient within primary-side dead-time stage (when both Q1 and Q2 are turned off) and a high-frequency ringing can be observed especially in current waveforms, which has not been well studied. The high-frequency ringing has dominating impact on I_{ini} so it has to be suppressed.

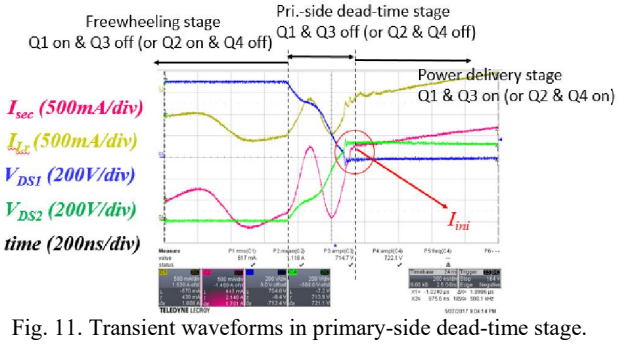

Fig. 11. Transient waveforms in primary-side dead-time stage.

Fig. 12 shows the equivalent circuit model of the LLC converter (Fig. 3(b)) in primary-side dead-time stage. All components are reflected to the primary side. C_p and C_s are primary and secondary-side device C_{oss} which are assumed to be linear. Resonant capacitors (C_{r1}, C_{r2}) and the other capacitors (C_{o1}, C_{o2}, C_o) have much larger capacitance so they are considered to be ineffective. At the beginning of the dead-time, resonant current and magnetizing current are I_r and I_m. The differential equations of the model are listed in (3) and the corresponding initial conditions are shown in (4). Solved by Laplace transform method, the s-domain result is shown in (5) and (6). Note that i_2 is the I_{sec} reflected to the primary side.

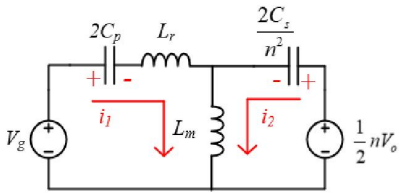

Fig. 12. Equivalent circuit model of LLC converter with SR in primary-side dead-time stage.

$$0=\frac{i_1}{2C_p}+L_r\frac{d^2i_1}{dt^2}+L_m\frac{d^2(i_1+i_2)}{dt^2},\ 0=\frac{n^2i_2}{2C_s}+L_m\frac{d^2(i_1+i_2)}{dt^2} \tag{3}$$

$$i_1(0)=I_r,\ i_2(0)=I_m-I_r,\ i_1'(0)=0,\ i_2'(0)=\frac{V_g}{2L_m} \tag{4}$$

$$I_2(s)=\frac{\frac{V_g}{4C_pL_mL_r}+\frac{I_ms}{2C_pL_r}+\frac{V_g}{2L_m}s^2+L_r(I_m-I_r)s^3}{(s^2+\omega_l^2)(s^2+\omega_h^2)} \tag{5}$$

$$\omega_l\approx\sqrt{\frac{1}{2L_m(C_p+\frac{C_s}{n^2})}},\ \omega_h\approx\sqrt{\frac{1}{2L_r}(\frac{n^2}{C_s}+\frac{1}{C_p})} \tag{6}$$

There are two basic frequencies in (5), ω_l and ω_h. Low-frequency ω_l is generated by the resonance between L_m and C_p, C_s/n^2 in parallel. In Fig. 11, the drop of V_{DS1} can be approximated by a quarter of ω_l-sinusoidal wave because ω_l implies how L_m discharges primary-side C_{oss}. Consequently, ω_l dominates the dead-time required for ZVS. On the other hand, high-frequency ω_h is caused by the resonance between L_r and C_p, C_s/n^2 in series, which is exactly the high frequency component needed to be suppressed. After applying inverse Laplace transform to (5), the amplitude of the ω_h-resonance is shown in (7). The final result in (7) is assumed to have I_r that equals I_m and the assumption is based on a prior freewheeling stage without parasitic effects.

$$\begin{aligned} i_{2,\omega_h}(t)&\approx(I_m-I_r)\cos\omega_ht-\frac{I_m}{2C_pL_r}\frac{\cos\omega_ht}{\omega_h^2}\\ &\approx-\frac{I_m}{2C_pL_r}\frac{\cos\omega_ht}{\omega_h^2}=\frac{-I_m}{(1+\frac{C_p}{C_s}n^2)}\cos\omega_ht\end{aligned} \tag{7}$$

From (7), if secondary-side device has larger C_{oss}, then the ω_h-resonance gets worse. On the contrary, increasing C_p helps alleviating the ω_h-resonance. Therefore, a tuning method is proposed to add external capacitor to the drain-source of Q1 and Q2. Similar approach can be found in [19] where external

capacitor is utilized to suppress the ringing in power delivery stage instead. Finally, the dead-time also has to be increased to guarantee the ZVS of Q1 and Q2, so the increment of C_p cannot be exaggerated.

IV. Experimental Results

The power module in Fig. 2 (except for the full-bridge rectifier at front) is built to verify the tuning method. The input voltage of the module is 600 VDC, and then boosted to 1.4 kV to supply two LLC converters with individual V_g of 700 V. The SR is silicon carbide (SiC) MOSFET and its performance is compared to the silicon diode rectifier in [8] as well. The photo of the LLC converter secondary-side circuit with SR is shown in Fig. 12 and the power stage parameters of the LLC converter are summarized in Table I.

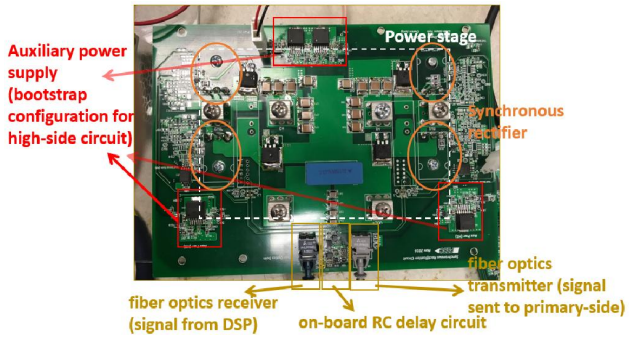

Fig. 12. Photograph of the LLC converter seconday-side circuit prototype with SiC SR.

TABLE I. Power Stage Parameters of LLC Converter

Input voltage (V_g)	700 V	Output voltage (V_o)	400 V
Output current (I_o)	0-10 A	Switching frequency (f_s)	84 kHz
Turns ratio (n)	21:12	Half-bridge capacitor (C_{o1}, C_{o2})	6.6 µF
Magnetizing inductance (L_m)	810 µH	Resonant capacitor (C_{r1}, C_{r2})	150 nF
Resonant inductance/ transformer leakage inductance (L_r)	11.2 µH	Series resonant frequency (f_r)	86.8 kHz
Primary-side switches (Q1, Q2)	C2M0080120D SiC MOSFET		
Secondary-side SR in new version (Q3, Q4)	SCT3022AL SiC MOSFET		
Secondary-side recitfier in original version (D3, D4)	60EPF06 silicon diode		

Fig. 13 shows the experimental steady-state waveforms of the LLC converter at nominal power level, which is 2.5 kW for a complete power module. At nominal power level, ZCP shifting and late turn-off issue are not severe. However, in light-load (500 W) testing waveforms, ZCP shifting is obvious, as shown in Fig. 14. Consequently, circulating energy depicted by blue diagonal stripe area is large. To solve the late turn-off issue, the tuning method proposed in the previous section is applied. Each primary-side device has a 120-pF ceramic capacitor added to the drain-source. In addition, primary-side dead-time is extended from 375 ns to 505 ns for the sake of ZVS. The light-load testing waveforms after tuning is shown in Fig. 15. I_{ini} drops from 2.1 A to 1.1 A and the circulating energy is greatly reduced, which concurs with the conclusion from the time-domain analysis.

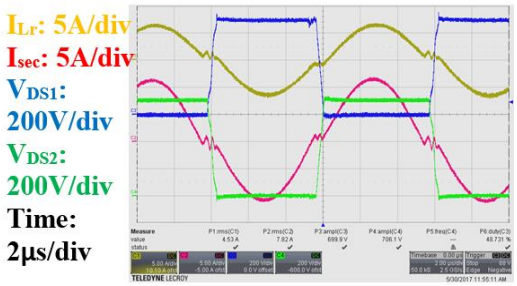

Fig. 13. Steady-state expereimental waveforms of LLC converter at nominal power level.

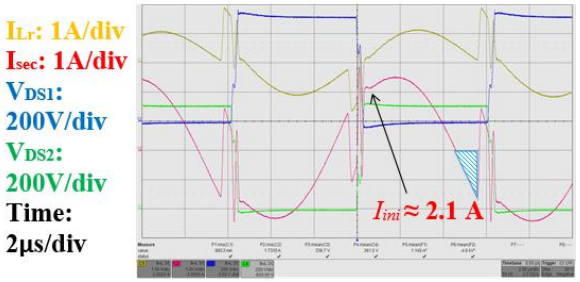

Fig. 14. Light-load steady-state waveforms before tuning.

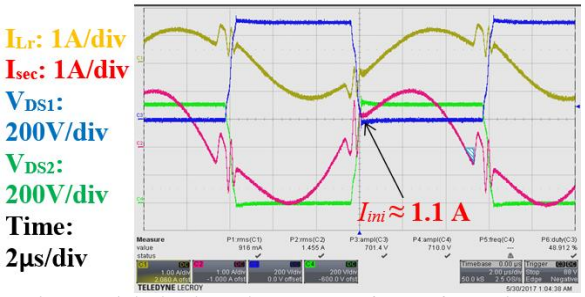

Fig. 15. Light-load steady-state waveforms after tuning.

Fig. 16 shows the power stage efficiency comparison. Without the tuning, light-load efficiency drops to 94%, which is almost 3% below the origin. With the tuning method, the SR improves the efficiency throughout the entire load range. At heavy-load condition, the entire power module reaches 98.5% peak efficiency, which is 0.3% higher than the version using original silicon diode rectifier. The power losses in gate driver and auxiliary circuits are not included in Fig. 16, but these losses together are no more than 1 W.

Finally, Fig. 17 shows the thermal image of the secondary-side circuit with SR in a 4-kW testing. Each SR has only a discrete TO-247 heatsink yet the temperature stays below 40°C. On the contrary, when the original silicon diode rectifier utilizes only discrete TO-247 heatsink, the temperature rises to above 80°C under the identical testing condition. Therefore, during the efficiency testing in Fig. 16, the secondary-side circuit without SR has a metallic plate as large heatsink. Although the temperature after thermal balance is not

measured in behalf of protecting the diodes, the difference is clear. Despite the need of extra driving circuit, SR technique has potential to reduce the cost and weight of the heatsink in a SST.

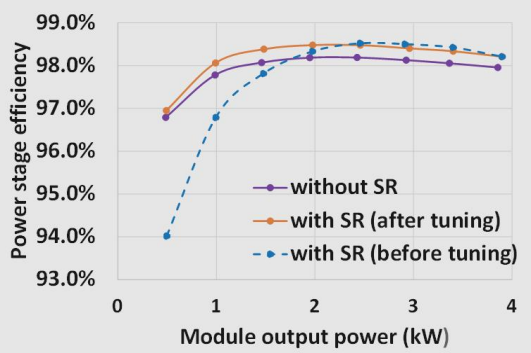

Fig. 16. Power stage efficiency comparison.

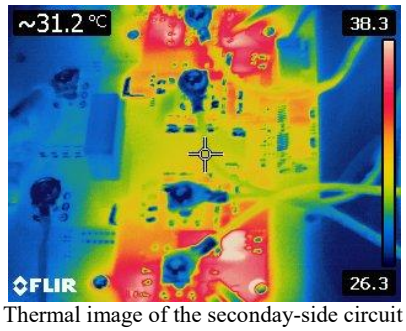

Fig. 17. Thermal image of the seconday-side circuit with SR under 4-kW testing.

V. CONCLUSION

Open-loop controlled scheme for synchronous rectification is advantageous in SST application due to its reliability. However, it has late turn-off issue caused by ZCP shifting. The mechanism of the problem is analyzed in this paper and a tuning method is proposed. Adding external capacitor on top of primary-side device C_{oss} helps alleviate late turn-off issue so the light-load efficiency is improved. However, the primary-side dead-time has to be prolonged as well. If the dead-time is over-extended, then the tuning method would backfire and hurts the efficiency at heavy load. Therefore, the external capacitor has to be carefully designed. A rule of thumb is to start the tuning from a value approximated to the device C_{oss}.

Typically, SR technique is used in the LLC converter for low-V_o and high-I_o applications, for example, a 380 V-12 V dc-dc converter in data center power architecture [20]. On the contrary, the synchronous rectification at higher-V_o condition is seldom mentioned. This paper provides experimental results of a 4-kW power module with V_o of 400 V and shows that SR improves the peak efficiency from 98.2% to 98.5%. In addition to energy-saving, the thermal image also implies the capability of SR technique to reduce the cost and weight of the heatsink in a SST.

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