Hybrid Buck Converter Optimization and Comparison for Smart Phone Integrated Battery Chargers

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***Abstract*—In this work, a hybrid switched-capacitor/PWM converter is analyzed and designed for battery charging in mobile electronics. Operation of the converter is reviewed to construct a complete analytical loss model based on FET extracted parameters for an integrated circuit implementation. The model is validated with experimental results and compared with other converter topologies in the same application. The loss modeling is used to optimize the physical scaling of the power transistors to minimize total losses.**

I. Introduction

Each year, new smartphones are released with faster processors, larger screens and more radios; in some cases supplanting computers as the device of choice. This results in an increasing energy demand from the batteries [1], [2] often requiring multiple charges per day [3], [4]. To address this, a common trend in charger design today is either charging for one hour to achieve an 80 percent state-of-charge or ten minutes to power a device for one day [5]. In order to reduce the charging time, an increased charging current is needed.

From the power electronics standpoint, the feasible charging current is limited by thermal constraints of the integrated chargers on the handset. Typical approaches are integrated buck converters where the power stage is integrated with the control and driving circuitry [6]–[8]. However, high current limits device sizing. In [9], a 10 A output integrated buck converter with a target on-chip loss is designed. Parasitic resistance introduced by the bond wires and metallization doubled the target loss. In addition, conduction losses in the inductor are considerable. Quasi single-stage converters [10], [11] reduce device voltage stress allowing the use of lower blocking voltage FETs. However, the use of more switches in the current path increases conduction losses. New USB Power Delivery adapters increase the input voltage to 9 V or 12 V to compensate for the voltage drop across the cable as well as allowing higher charging power [5], [12], [13]. This method necessitates a topology that is able to maintain high efficiency over a range of input voltages rather than being optimized for a fixed conversion ratio.

As shown in [14] the development of small and efficient inductors for power electronics has not kept pace with the advances of switch integration. As a result, performance of high current converters is often be limited by the magnetic component. Choosing the appropriate topology for a given application can mitigate this limit. A design space for various operating points between the buck, 3-level buck and 2:1 switched capacitor converter was given in [15].

The converter of Fig. 1 is derived through integration of a boost converter and 2:1 switched capacitor step-down converter, and thus referred to as a "hybrid buck" converter in this work. As a result of the integrated topology, the PWM inductor is stressed only to the input current, each FET blocks only the output voltage, and the converter maintains a current path from input to output which sees only one FET on-resistance. This converter was independently studied in [16], where it was implemented for a 15 W battery charger. It's small-signal performance was evaluated in [17], while its general merits in [18]. In both studies, the inductor is distributed in the input-voltage cable and the focus is developing control methods under this implementation. This will only affect the analysis of the control and so for the purpose of this paper, the inductor is implemented as a single, discrete component at the input.

This work looks to advance the design considerations for the hybrid buck in a standard CMOS process, as well as evaluate its advantages and drawbacks in comparison with traditional topologies. Section II details the operation of the hybrid buck converter including loss modeling. Section III discusses validation of the design through hardware testing. Section IV evaluates optimal device sizing. Section V compares the performance and operation range of the hybrid buck with the buck and the 3-Level buck in hardware to further validate the design.

II. Modeling

The hybrid buck converter is derived from a 2:1 switched capacitor (SC) converter as shown in Fig. 2. The 2:1 SC converter has input v_y and output v_{out}. Node V_x swings between V_{out} and $2V_{out}$. To form the hybrid buck, an inductor

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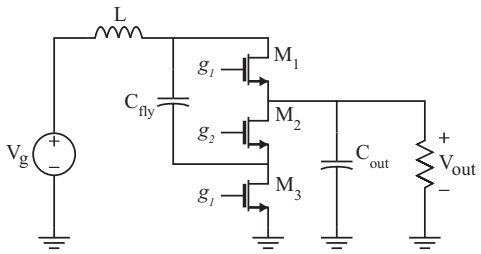

Fig. 1. hybrid buck converter schematic.

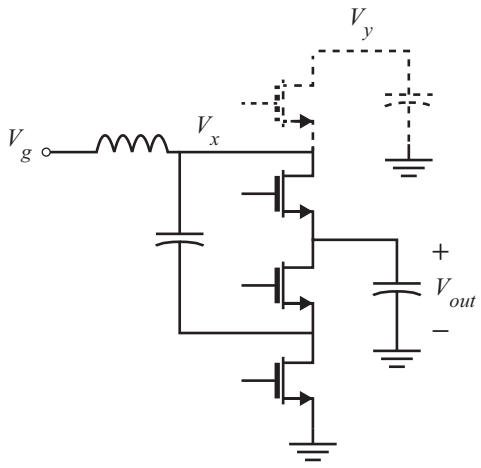

Fig. 2. hybrid buck converter derivation.

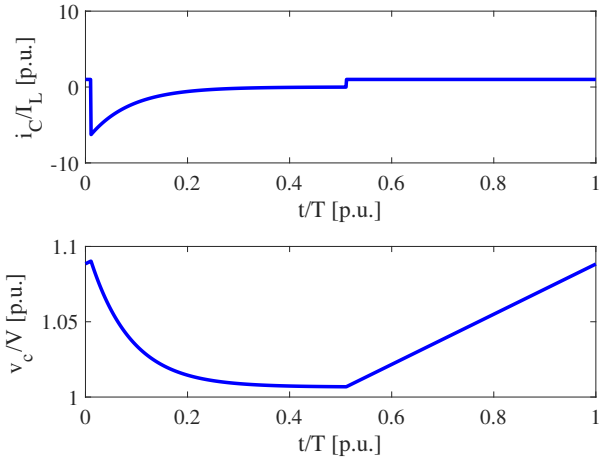

Fig. 3. hybrid buck converter key waveforms. Capacitor current and voltage in terms of inductor current and output voltage.

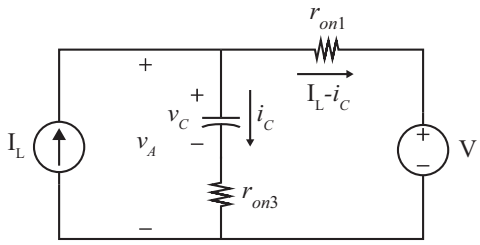

Fig. 4. Equivalent linear circuit for interval I.

is connected to this node, and the input is moved from v_y to the other terminal of the inductor. In this arrangement, the indcutor current is controlled by the duty cycle of the converter, and net volt-seconds applied to it are reduced relative to a traditional buck, decreasing the current ripple. In addition, as it is connected to the input port, the inductor conducts lower average current. After relocating the input, the top transistor no longer processes any power, and can be removed without affecting operation.

A. Operation

A schematic of the hybrid buck converter is shown in Fig. 1. During interval I, M_1 and M_3 are turned on from $0 < t < DT_s$. The flying capacitor, C_{fly}, is connected in parallel to C_{out}. During interval II, M_2 connects the flying capacitor in series between the inductor and the output from $DT_s < t < T_s$. By applying volt-second balance on the inductor the conversion ratio of the converter is

$$\frac{V}{V_g} = \frac{1}{2-D}. \tag{1}$$

As a consequence, the hybrid buck converter can only output voltages ranging from V_g to $0.5V_g$. The inductor current is found by power balancing between the input and output port,

$$I_L = \frac{I_{out}}{2-D}. \tag{2}$$

This result is a major improvement over other inductive step-down switching converters like the buck or the 3-level buck: while maintaining duty-cycle regulation of the output and step-down conversion, the magnetic component is stressed only to the input current. Additionally, the magnitude of the voltage applied to the inductor is reduced relative to the buck, allowing lower ripple and, consequently, ac losses in the magnetic component. Equation (1) uses small ripple approximation on C_{fly}, C_{out} and the inductor. This approximation is certainly true for the output capacitor and the inductor. However, during interval II inductor current flows through the flying capacitor to the output increasing its voltage as

$$\Delta v_c = \frac{I_L}{C_{fly}}(1-D)T_s \tag{3}$$

This is shown in Fig. 3. To examine this effect, each interval is analyzed using equivalent linear circuits as shown in Fig. 4 and Fig. 5, where the inductor and the output capacitor are replaced by equivalent DC sources and $r_{on,i}$ represents the on-resistance of switch M_i. At the beginning of Interval I, the initial voltage on the flying capacitor is V_1. Then, $v_A(t)$ is

$$v_A(t) = V + (I_L - i_C(t))\, r_{on1} \tag{4}$$

$$v_A(t) = V_1 + \frac{1}{C_{fly}} \int i_C dt + i_C r_{on3} \tag{5}$$

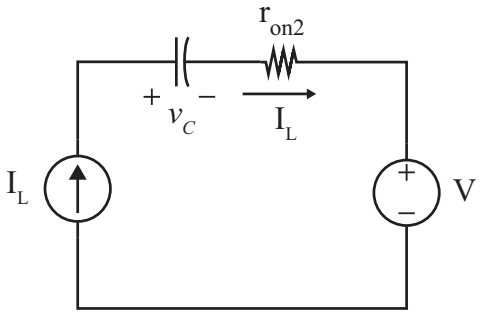

Fig. 5. Equivalent linear circuit for interval II.

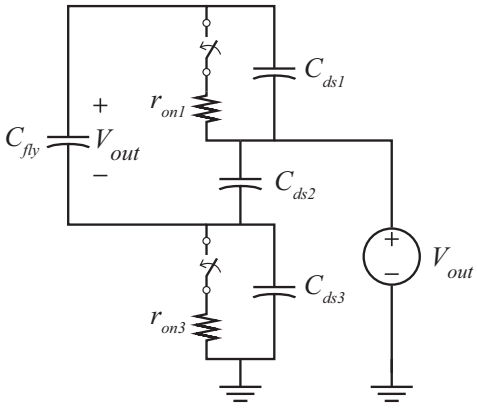

Fig. 6. Equivalent circuit to model C_{oss} losses. Each FET has to block the output voltage.

Combining these equations, V_1 and V_2 are

$$V_1 = V + I_L r_{on1} + \frac{\frac{I_L}{C_{fly}}(1-D)T_s}{1 - e^{-\frac{DT_s}{R_T C_{fly}}}} \quad (6)$$

$$V_2 = V + I_L r_{on1} + \frac{I_L(1-D)T_s}{C_{fly}} \left(\frac{1}{1 - e^{-\frac{DT_s}{R_T C_{fly}}}} - 1 \right) \quad (7)$$

where $R_T = R_{on1} + R_{on3}$. Considering an integrated circuit implementation where the on-chip area of each FET can be designed, $R_T = R_{sp}(1/A_1 + 1/A_3)$, where R_{sp} is the specific on-resistance per unit area and A_1 and A_3 are the areas of M_1 and M_3 respectively. If $DT_s >> R_T C_{fly}$, i.e. the flying capacitor discharges fully to the output within the interval, V_1 and V_2 can be simplified to

$$V_1 = V + I_L r_{on1} - \frac{I_L}{C_{fly}}(1-D)T_s \quad (8)$$

$$V_2 = V + I_L r_{on1} \quad (9)$$

These equations model the charge redistribution that occurs through M_1 and M_3 at the beginning of interval I, discharging the flying capacitor from V_1 to V_2 and delivering energy to the load.

B. Loss model

Power losses in the hybrid buck converter are

$$P_{loss} = P_{cap} + P_{cond} + P_{sw}. \quad (10)$$

The first term represents the losses on M_1 and M_3 associated with the charge sharing process. This contribution can be calculated by finding the energy lost in the switches in the equivalent circuit of Fig. 4.

$$P_{cap} = \left(\int_{V_2}^{V_1} C(v_c - V) dv_c \right) f_s = C \left(\frac{V_1^2 - V_2^2}{2} - (V_1 - V_2)(V - I_L r_{on1}) \right) f_s \quad (11)$$

The inductor current I_L also flows through M_1 during this interval and through M_2 during interval II. In addition, during the dead times, the body diode of M_2 conducts the inductor current. Then, conduction losses are

$$P_{cond} = I_L^2 R_{sp} \left(\frac{D}{A_1} + \frac{1-D}{A_2} \right) + 2V_f I_L t_d f_s \quad (12)$$

Switching losses consists of C_{oss}, overlap and gate losses. The former is calculated as follows: M_1 and M_3 turn on is modeled by the circuit of Fig. 6. Here, three simultaneous process occur:

1) Charging C_{ds2} to V_{out} through r_{on3}
2) Discharging C_{ds1} through r_{on1}
3) Discharging C_{ds3} through r_{on3}

Thus, losses associated to these three processes can be calculated as

$$P_{Coss} = \frac{1}{2} \left(C_{eq,E,sp} A_1 - C_{eq,E,sp} A_2 + 2C_{eq,Q,sp} A_2 + C_{eq,E,sp} A_3 \right) V^2 f_s \quad (13)$$

where $C_{eq,E,sp}$ and $C_{eq,Q,sp}$ are the equivalent energy and charge equivalent capacitance per unit area [19]. Overlap losses only occur on M_1, as M_2 will have soft turn on due to its body diode conduction and M_3 does not conduct the inductor current. Then,

$$P_{ov} = \frac{1}{2} V I_L Q_{sw,sp} A_1 \left(\frac{1}{I_{g,on}} + \frac{1}{I_{g,off}} \right) f_s \quad (14)$$

And finally, gate losses are

$$P_{gate} = V_{dr} Q_{g,sp} (A_1 + A_2 + A_3) f_s \quad (15)$$

where $Q_{sw,sp}$ is the gate switching charge per unit area, $I_{g,on/off}$ are the gate driver on/off currents, V_{dr} is the driving voltage of the switches and $Q_{g,sp}$ is the gate charge per unit area.

C. Flying capacitor sizing

In Section II-B, the loss associated with the capacitor charge sharing is described. For a given inductor current and a conversion ratio, the capacitor ripple will depend not only on the capacitance value but also on the switching frequency. As

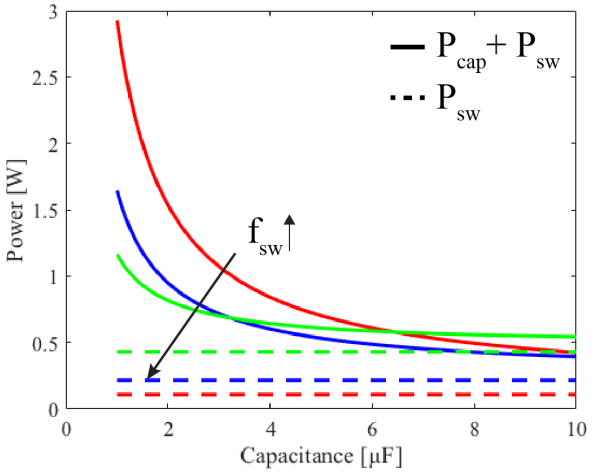

Fig. 7. Charge sharing losses as a function of the value of the capacitor for different frequencies.

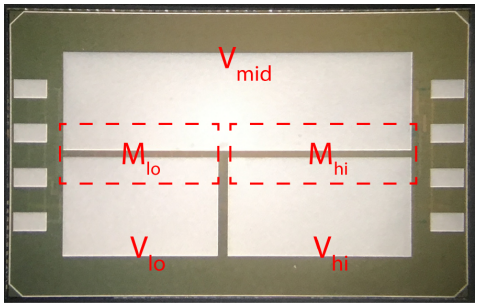

Fig. 8. Custom flip chip half bridge used to construct the hybrid buck converter.

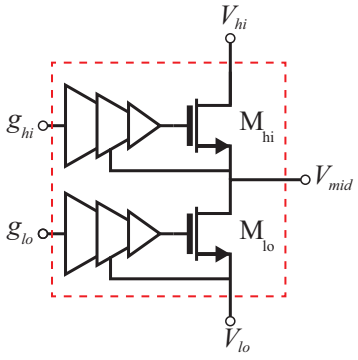

Fig. 9. Schematic of the half bridge used to construct the hybrid buck converter, constructed with 7 V LDMOS FETs with integrated gate drivers.

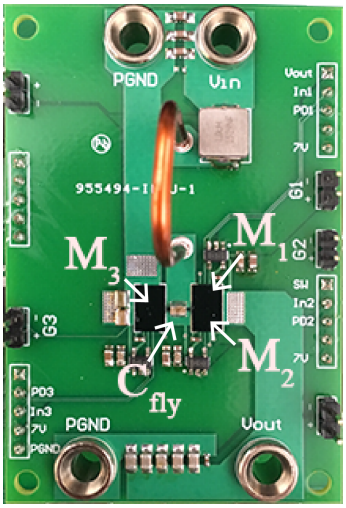

Fig. 10. Implemented hybrid buck converter.

the switching frequency reduces, the capacitor is charged for a longer time, increasing the charge sharing current during interval I. Fig. 7 shows how the charge sharing losses and switching losses ($P_{Coss} + P_{ov} + P_{gate}$) are affected by the value of the capacitor and for switching frequencies of 500 kHz, 1 Mhz and 2 MHz for $V_g = 6$ V and $V_{out} = 4$ V for $I_{out} = 5$ A. A smaller capacitance can be used if the frequency is increased, however, due to switching losses, there are trip points where increasing the operating frequency doesn't further reduce the losses. The optimization of switching frequency and capacitance has additional impacts on converter ripple and inductor selection. Thus, to facilitate comparison with alternate topologies the switching frequency and capacitance are considered constant in this work.

III. Experimental Validation

In order to validate the loss model constructed in Section II-B, a hybrid buck converter is built using two integrated half bridges (Fig. 8 and Fig. 9). This power stage is packaged as a custom flip-chip in order to reduce parasitic resistance and inductance introduced by bond wires in other packages, e.g. QFN [9]. Each FET is an 7 V LDMOS and has its own isolated gate driver. The driving voltage is provided by isolated power supplies and the input signals $g_{hi/lo}$ are generated by an FPGA and Digital Isolators. The integrated power stage outputs the gate-to-source voltage of each switch in order to monitor the corresponding waveforms. The high-side on-resistance is 3.5 mΩ and the low-side is 4.75 mΩ with $L = 1$ µH, $C_{fly} = 10$ µF, $C_{out} = 100$ µF. The converter is tested at $f_s = 1$ MHz, $V = 4$ V and up to an output current of 5 A. A picture of the implemented converter is shown in Fig. 10. The converter is constructed using two half-bridges, with one device unused. M_1 and M_3 are M_{hi} and M_2 is M_{lo} from the same IC of M_1. The flying capacitor forms part of the power loop between M_1 and M_2 that is minimized by placing it as close as possible to the switches while the power loop formed by M_2 and M_3 is decoupled by an inner layer loop to minimize the inductance [20]. In addition, these capacitors are 0508 in order to achieve minimal inductance and ESR. Fig. 11 shows the captured waveforms of the converter running at $V_g = 5$ V and $I_{out} = 1.5$ A. The capacitor voltage is AC coupled so that the linear charging of the flying capacitor during interval II ($M_{1,3}$ off and M_2 on) and exponential discharging during interval I can be seen.

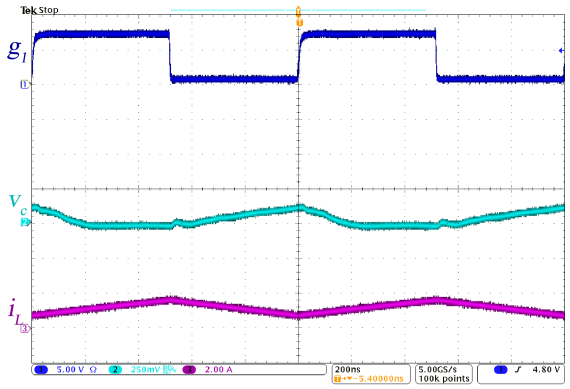

Fig. 11. hybrid buck converter charge sharing process. CH1: v_{gs1} - CH2: v_{fly} (DC Rej.) - CH3: i_L

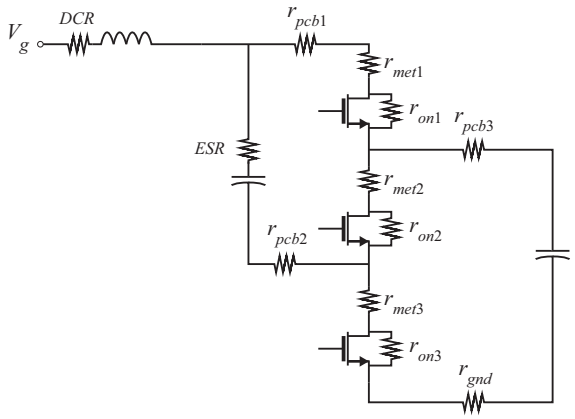

Fig. 12. Parasitics resistances involved in the converter.

In order to predict the losses of the converter using the model developed in Section II-B, the parasitic resistances involved in the current path for each interval are extracted by I-V measurements, i.e. with M_1 turned on, inject a current through the input of the power stage and measure the voltage across V_g and V_{sw} of Fig. 8. This measurement includes the solder joint, the internal metallization of the power stage and the on-resistance of the switch. Fig. 12 shows a schematic of the hybrid buck converter including the parasitic resistances involved in the current path. In this circuit, $r_{pcb,i}$ represents the parasitic resistance introduced by the pcb traces while $r_{met,i}$ are the parasitic resistance due to the solder joints and the metallization of the switches. Then, during interval I, the inductor current flows through $r_{pcb1} + r_{met1} + r_{on1}$ and the charge sharing current through $ESR + r_{pcb2} + r_{met3} + r_{on3} + r_{pcb1} + r_{met1} + r_{on1}$. Finally, during interval II, I_L flows through $ESR + r_{pcb2} + r_{on2} + r_{met2}$. Table I summarizes these expressions with the measured values.

The implemented hybrid buck converter of Fig. 10 is tested under three different input voltages up to 5 A of load current at $f_s = 1$ MHz while keeping the output voltage at 4 V. Fig. 13 plots power losses over the load current. The loss model matches the measurements over different input voltages.

TABLE I
RESISTANCES INVOLVED IN EACH PHASE FOR THE IMPLEMENTED HYBRID BUCK CONVERTER.

Phase	Devices	Total resistance	Value [mΩ]
I	M_1	$r_{pcb1} + r_{met1} + r_{on1}$	7.2
	M_3	$ESR + r_{pcb2} + r_{met3} + r_{on3}$	11
II	M_2	$ESR + r_{pcb2} + r_{on2} + r_{met2}$	12

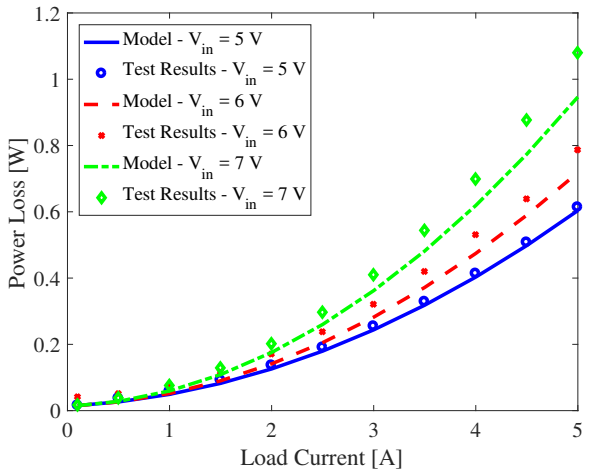

Fig. 13. Test Results for three different input voltages. Output voltage is 4 V and switching frequency is 1 MHz.

As can be seen, losses increase when the input voltage increases. As the conversion ratio reduces, interval II gets longer. This means that for the same inductor current, the flying capacitor is charged for a longer time increasing $V_1 - V_2$. Then, the loss associated with the charge sharing process in Equation (11), increases. This is equivalent to decreasing the switching frequency as described in Section II-C.

IV. DEVICE SIZING

The implemented converter in Section III uses a suboptimal size for each switch. Due to fabrication constraints, the half bridges used to implement the hybrid buck are repurposed from previous work [15]. Based on the analysis presented in Section II-B, it can be seen that each switch conducts a different current during the conduction time. The current through M_1 is comprised of the inductor current and the charge sharing current, M_2 conducts only the inductor current and M_3 conducts only the charge sharing current. Thus, optimal sizing of each transistor to minimize losses in a limited total silicon area would lead to different sizes for each device.

Fig. 14 uses the loss model of Section II-B to compute the optimal portion of the total silicon area for each FET, and computes the resulting optimized on-chip power loss. The left axis is the portion of the area that is allocated for each FET while the right axis is the total calculated power loss. The red dashed line represents the power loss of an even distributed

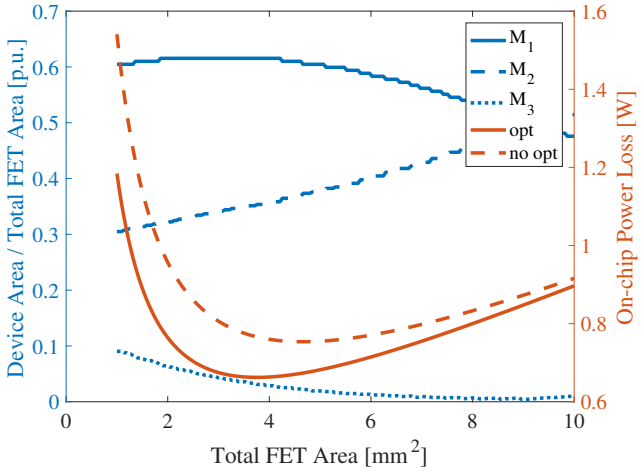

Fig. 14. FET area optimization to decrease the losses.

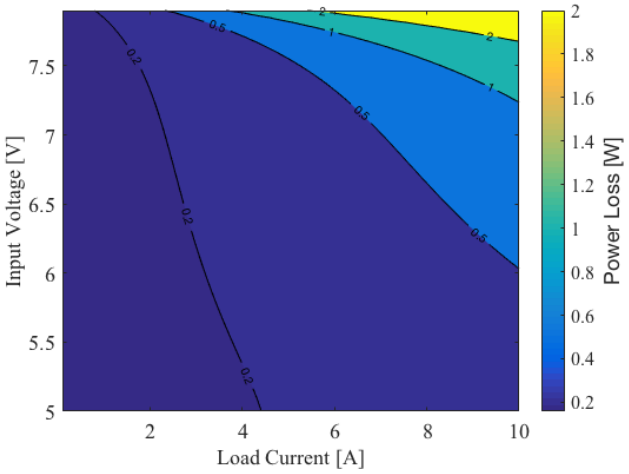

Fig. 15. Loss map for an optimized hybrid buck converter with a total FET area of 3.3 mm^2.

hybrid buck converter; that is, each switch uses one third of the total FET area. At small areas, power stage optimization has a large impact on the losses, while this effect reduces as switching losses become dominant at large areas.

Fig. 15 shows the loss map for a fixed total FET area over load current and input voltage at $V_{out} = 4$ V and $f_s = 1$ MHz. The switch area for this plot is 3.3 mm^2, which is equal to the prototype detailed in Section III. For each operating point (V_g, I_L), the transistor scaling in the power stage is optimized giving the optimal power loss.

Fig. 16 compares the hybrid buck converter with other step-down converters. It shows the minimum power loss contours between a buck, 3-Level buck and a hybrid buck converter, with only the lowest power loss topology selected at each operating point (V_g, I_L). The three converters have the same total FET area of 3.3 mm^2 and the size of each switch is optimized to find the lowest power loss for each operating

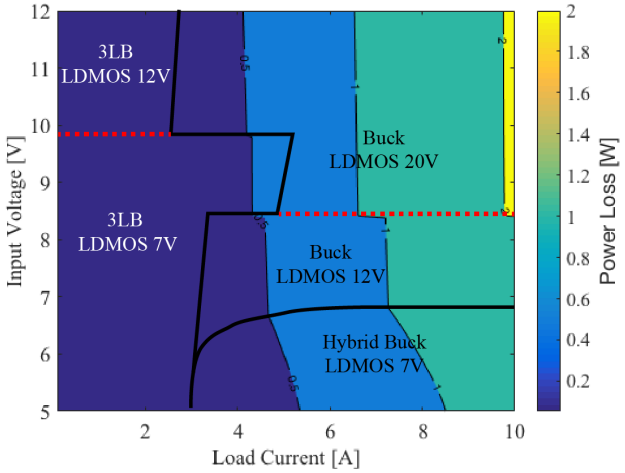

Fig. 16. Power loss map comparing a buck, 3-Level buck and a hybrid buck converter for a total FET area of 3.3 mm^2.

point [9]. Depending on the input voltage, device blocking voltage selection is selected using a safety margin of 1.2 in order to account for voltage breakdown of the FETs. In addition, due to the output voltage, the hybrid buck converter is only evaluated between 5 V and 8 V according to Equation (1). The hybrid buck and the buck converters are evaluated at $f_s = 1$ MHz. The 3-Level buck doubles the switching frequency of the inductor current, thus it is evaluated at 500 kHz. At light load, where switching losses dominate, the 3-Level buck performs with lower losses due to the lower switching frequency and the reduced blocking voltage of $V_g/2$ of the devices. As current increases, conduction losses begin to dominate the performance of the converters. The hybrid buck converter has lower losses than the other topologies. Inductor losses are reduced due to the fact that it is located at the input port. In addition, there is one less switch than the 3-Level buck and 7 V LDMOS are used due to the lower blocking voltage when compared with the buck converter that, at the same input voltage needs to use 12 V devices. As the input voltage increases, charge sharing losses in the hybrid buck converter increase and the buck outperforms the other converters.

V. Conclusion

The hybrid buck converter presents two major benefits when compared with other inductive step-down converters. First, the three transistors are stressed only to the output voltage, allowing the use of low blocking voltage devices with lower on-resistance. Second, the inductor is located at the input port where lower current flows, reducing conduction loss of the inductor. Then, a smaller inductor can be used while maintaining its losses when compared with an output port inductor converter. These two improvements, along with optimized FETs sizing, make the hybrid buck converter perform with lower losses at heavy load.

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