System Optimization of a High Power Density Non-Isolated Intermediate Bus Converter for 48 V Server Applications

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***Abstract*— With the power architecture transition from a 12 V to 48 V rack in modern data centers there is an increased interest in improving 48 V power conversion efficiency and power density. In this paper, we will analyze system optimization for a 48 V to 12 V non-isolated, fully regulated, intermediate bus converter (IBC) to maximize efficiency and power density. The final experimental prototype, a fully regulated, digitally controlled, 720 W, five phase, GaN transistor based 48 V to 12 V buck IBC demonstrates exceptional efficiency and power density, respectively exceeding 95% and 1000 W/in^3.**

I. Introduction

For higher performance in 48 V applications [1-3], there have been many different topological approaches ranging from hard-switching [4-6,8] to highly resonant [7,9-12], fully regulated to unregulated, and fully isolated to non-isolated. A plot of performance vs density for the different approaches with an output voltage of 12 V are shown in figure 1. In general, resonant and soft-switching converters provide the highest efficiency and power density, but have the least flexibility with regard to regulation and input voltage variation.

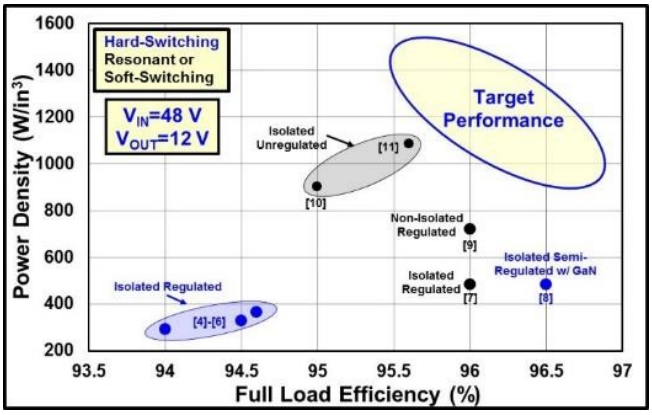


Figure 1: Comparison of full load efficiency and power density of state-of-the-art commercial products and previously published research

In this paper, we will focus on employing the simplest and most common topology, a non-isolated multi-phase 48 V buck converter (detailed schematic shown in figure 6), the topology of choice for the downstream 12 V point of load (POL) conversion, designed with superior GaN transistors for use as a high performance fully regulated intermediate bus converter (IBC). Beyond employing improved power devices, the paper will focus on magnetic optimization with final design full load efficiency targeted above 95% and power density targeted in the range of 1000-1500 W/in^3.

II. Impact of GaN Transistors on Performance

The introduction of high performance GaN transistors [13] has lessened the impact of semiconductor on power converter performance and offers the potential to revisit topologies that may not have been previously possible or practical with Si MOSFET technology. In table I, 100 V state-of-the-art GaN and Si MOSFETs are compared. The GaN transistor has lower on-resistance, universally lower charges, and occupies a fraction of the board space compared to the Si MOSFET.

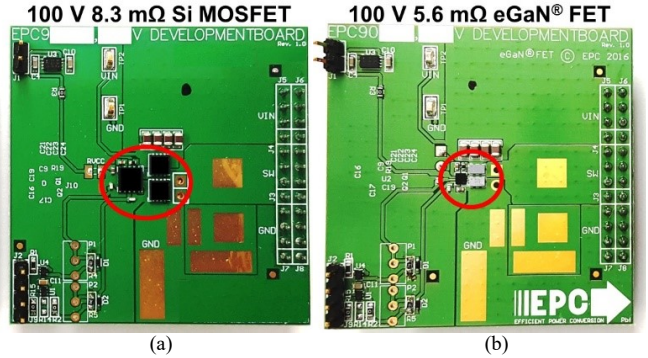
Table I: Characteristic comparison of 100 V GaN and Si Transistors

Device Technology	GaN	Si
Voltage Rating (V)	100	100
Part Number	EPC2045	BSZ097N10NS5
Typical On-Resistance $R_{DS(on)}$ (mΩ)	5.6 @ 5 V	8.3 @ 10 V
Total Gate Charge Q_G (nC)	5.2 @ 5 V	22 @ 10 V
Gate-to-Drain Charge Q_{GD} (nC)	1.1	5
Gate-to-Source Charge Q_{GS} (nC)	1.7	7
Output Charge Q_{OSS} (nC)	21	30
Reverse Recovery Charge Q_{RR} (nC)	0	60
Device Area (mm^2)	3.75	10.89

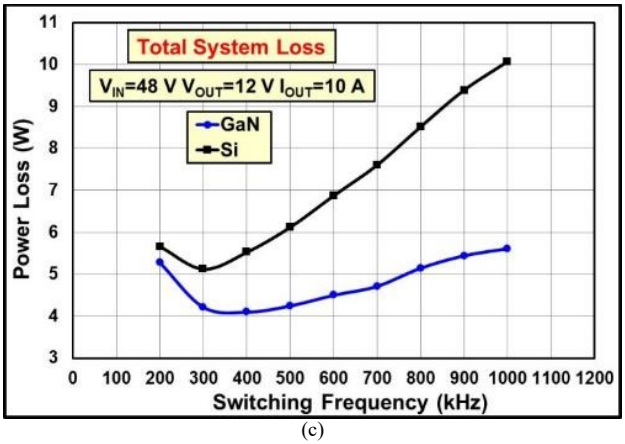
To evaluate the impact an improved semiconductor has on the system performance, two experimental evaluation boards were developed and are shown in figures 2 (a) and (b) for Si MOSFET and GaN transistor based prototypes, respectively. Each prototype is designed with a similar layout based on [13]: uses four-layer, two by two inch, two-ounce copper PCBs, the same output inductor (5.6 µH, IHLP-5050FD-01), and gate drivers designed for their respective technologies.

The switching frequency was swept for both designs from 200-1000 kHz and the measured total system power loss is shown in figure 2(c) for an output current of 10 A. As frequency increases from 200 kHz to 300 kHz, the total system power loss decreases for both technologies, indicating that the inductor core loss reduction is greater than the increase in device switching losses in this frequency range for the selected inductor. Beyond 300 kHz, the total system loss of the Si MOSFET based design increases significantly, indicating the device switching losses dominate power loss at higher frequencies. The GaN transistor based design demonstrates reduced system losses from a switching frequency of 200 kHz

to approximately 400 kHz, with the total losses increasing at a much lower rate up to 1 MHz. This indicates that the GaN transistor switching loss contributes a much lower percentage of the overall system power loss as result of the improved characteristics outlined in table I. For a given device and inductor, an optimal design point can be selected at the frequency with the minimal loss, which is around 300 kHz for the Si MOSFET and around 400 kHz for the GaN transistor in the case of figure 2. To better understand the optimization procedure, a more detailed loss breakdown is required and will be developed later in this paper. But, from figure 2(c) it is clear that a better semiconductor will provide the designer the ability to explore higher frequency without sacrificing significant performance to pursue higher power density.



(a) (b)



(c)

Figure 2: Experimental V_{IN}=48 V to V_{OUT}=12 V prototypes: (a) Si MOSFET based design with BSZ097N10NS5 Si MOSFETs and ISL2111 MOSFET 10 V gate driver and (b) GaN transistor based design with EPC2045 eGaN FETs and GaN FET LM5113 gate driver. (c) Comparison of frequency impact on performance for GaN and Si transistor based prototypes

III. Impact of Inductor Selection on Performance and Power Density

The first step towards optimizing converter performance is to narrow the optimization process to a suitable switching frequency range. For this application, a wide initial potential frequency range is set from 200 kHz to 1 MHz, based on the results obtained from figure 2(c). The second step is to choose potential series of commercially available inductors that are suitable for the frequency range considered in this paper for evaluation. The selection criteria is given in equations (1)-(3):

$$I_{LTEMP} > 1.25 \cdot I_{OUT} \quad (1)$$

$$I_{LSAT} > 1.25 \cdot I_{LPK} \quad (2)$$

$$0.2 \cdot I_{OUT} < \Delta I_{LPK\text{-}PK} < I_{OUT} \quad (3)$$

Where I_{LTEMP} is the heat rating current of the inductor, I_{OUT} is the full load output current of each phase of the converter, targeted between 10-15 A, I_{LSAT} is the saturation current of the inductor, and I_{LPK} is the peak inductor current, including peak to peak current ripple, given by $\Delta I_{LPK\text{-}PK}$. Using the initial selection criteria to narrow the suitable candidates, thirty-six inductors, from ten series (each series identifies a certain volume), and three manufacturers were selected for evaluation.

An automated test equipment (ATE) setup was used to test the inductors on the GaN transistor based test board. Figure 3 shows a plot of the experimentally measured system loss for frequencies ranging from 200 kHz to 1000 kHz for each inductor from a given inductor series #4 (refer table III) selected for evaluation that met the criteria outlined in equations (1)-(3). In this plot, each color represents a different inductor value, the data points are sized relative to their effective current ripple, and a minimum loss curve is generated, with the curve color representing the optimal inductance for the respective switching frequency range. Continuing this practice, a curve similar to figure 3 was generated for each inductor series.

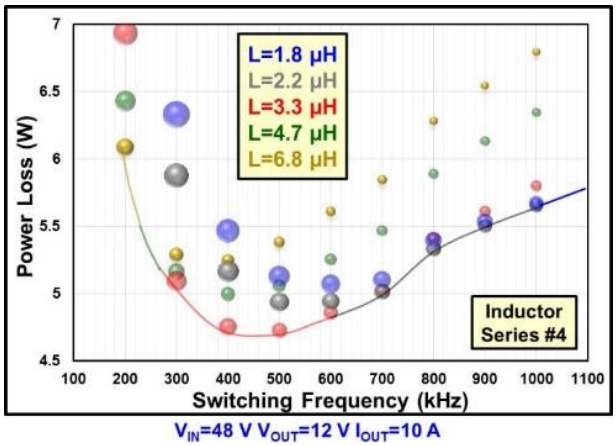


Figure 3: Experimentally measured impact of frequency and inductance on system power loss for GaN transistor based converter where dot size is proportional to inductor current ripple for inductor series #4

TABLE II: Summary of optimal inductance and corresponding current ripple for inductor series #4

fsw (kHz)	Optimal L (µH)	$\Delta I_{Lpk\text{-}pk}$ (%) I_{OUT}=10 A
200	6.8	66%
300	3.3	91%
400	3.3	68%
500	3.3	55%
600	3.3	45%
700	2.2	58%
800	2.2	51%
900	2.2	45%
1000	2.2	41%

The impact of frequency and inductance on system performance is evaluated and a clear optimization point is reached around 500 kHz with an inductance of 3.3 µH for this series of inductor (IHLP-5050EZ-01). Table II gives the optimal inductance value and effective switching ripple percentage for each switching frequency and the trend of lower optimal inductance for higher frequencies is verified in the experimental hardware, with the optimal switching ripple generally lying between 40% to 60% for the frequencies of interest for the GaN based prototype.

With the objective of higher power density, and a GaN transistor capable of high frequency, the next exercise was to assess the impact of frequency on inductor volume. From the initial inductor testing, three different series of inductors, with volumes ranging from 424 mm^3 to 1090 mm^3 were selected for the evaluation. The minimum loss curves for these three series are shown in figure 4. From figure 4, there are two clear findings: (1) smaller sized inductors require higher frequencies to reach their optimal system frequencies and (2) the inductor loss represents a significant portion of overall system loss, with the total system loss changing by over 30% when comparing the three series of inductors. In the following subsection, inductor loss will be evaluated in greater detail in an effort to get a better understanding of the loss breakdown of the system.

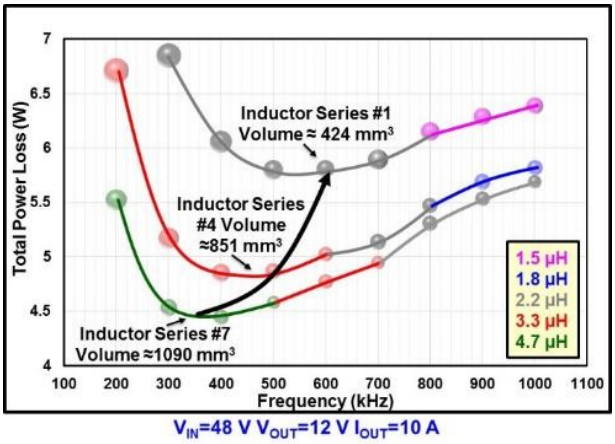
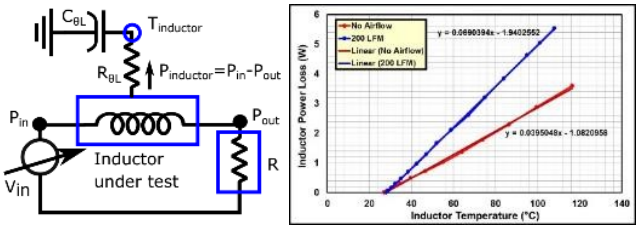


Figure 4: Experimentally measured impact of frequency and inductance on system power loss for GaN transistor based converter where dot size is proportional to inductor current ripple for three different inductor volumes

A. Estimating Inductor Losses

In figure 4, a large relative system loss introduced by the power inductor was encountered. To better understand the tradeoffs in the system, inductor loss characterization must be improved. While much information about core loss estimation methods and material properties for discrete core materials has been published [14-17], very little information is given about the core or winding properties of commercial inductors beyond vendor calculators, which will be compared to measured experimental data in table III, at the end of this subsection.

The method used to estimate the inductor loss for this work was calorimetric [18-19]. Taking the test board from figure 2(b), a loss versus temperature rise model for an inductor series was generated using the setup in figure 5 for no air flow (0 LFM) and minimal forced air cooling (200 LFM). It consists of a simple L-R circuit, with L representing the inductor under test, a variable DC source, and a load resistance R. The system was allowed to reach thermal steady state with the same ambient conditions, i.e. same $R_{\theta L}$ and $C_{\theta L}$ as the test converter, and the inductor temperature was measured with an infrared camera. This enables us to generate and directly measure inductor loss, $P_{inductor}$, while recording the inductor temperature, $T_{inductor}$, for a test case representative of the power converter setup, shown in figure 2(b). The inductor temperature data was also measured in the previous power converter testing and could be cross-referenced against these loss curves to estimate the magnetic loss component in the converter circuit, including the difficult to model AC winding and core losses.



(a) (b)

Fig. 5: (a) Calorimetric setup for estimating magnetic losses and (b) measured inductor power loss as a function of temperature

The resulting measurements for the final seven inductors under consideration, at a switching frequency of 500 kHz, are shown in table III and compared to their respective vendor calculators. The medium sized inductor series #4 was selected to be the inductor of choice for the initial multiphase prototype (discussed in the following section), as a result of its good tradeoff between size, performance, and temperature rise; and the inductor volumes in table III are normalized to it for comparison. From table III, the impact of the inductor on system performance becomes clearer, with the inductor loss representing 45-55% of the total system loss. It also demonstrates that the manufacturer's loss and temperature calculators were unable to choose the best inductor for the system, with some series underestimating loss and temperature and others overestimating loss and temperature.

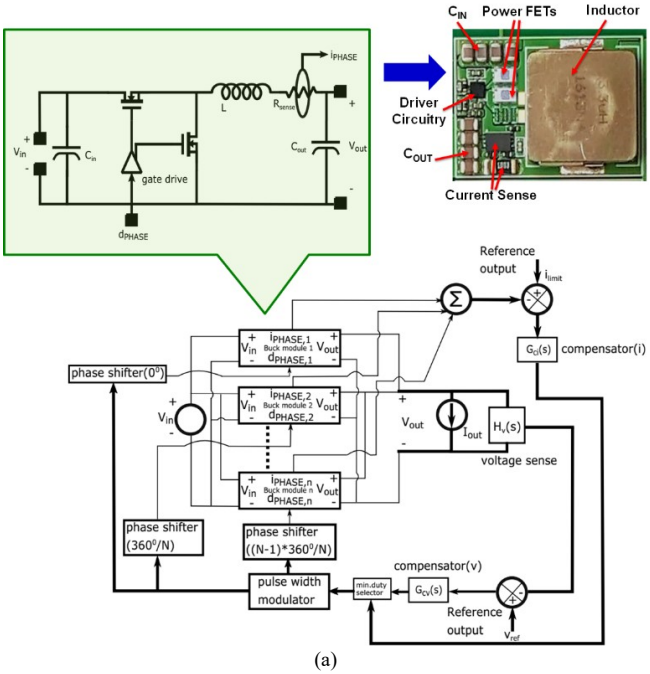
TABLE III: COMPARISON OF TESTED INDUCTOR SERIES FOR V_{IN}=48 V TO V_{OUT}=12 V, 500 KHZ, 10 A GAN BASED IBC

Small Size (Normalized Volume < 0.80)		
Parameter	Series #1	Series #2
Optimal Inductance (µH)	2.2	3.3
Tested Inductance Range (µH)	2.2-4.7	3.3-4.7
Normalized Volume (to Series #4)	0.56	0.79
$P_{inductor}$ Measured (W)	3.46	3.14
$P_{inductor}$ Vendor Calculator (W)	3.91	1.99
ΔTemperature Measured (200 LFM) (°C)	83.9	60.6
ΔTemperature Vendor Calculator (°C)	114.9	31.0

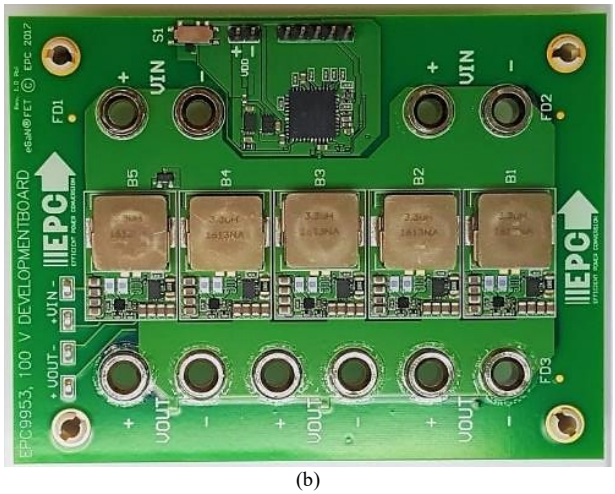
Medium Size (0.80 < Normalized Volume < 1.20)			
Parameter	Series #3	Series #4	Series #5
Optimal Inductance (µH)	3.3	3.3	3
Tested Inductance Range (µH)	1.8-4.7	1.8-6.8	2.2-3.0
Normalized Volume (to Series #4)	0.95	1.00	1.07
$P_{inductor}$ Measured (W)	3.00	2.48	3.27
$P_{inductor}$ Vendor Calculator (W)	3.43	3.42	2.32
ΔTemperature Measured (200 LFM) (˚C)	45	39	59.4
ΔTemperature Vendor Calculator (˚C)	85.7	68.5	46.0
Large Size (Normalized Volume > 1.20)			
Parameter	Series #6	Series #7	
Optimal Inductance (µH)	3.3	3.3	
Tested Inductance Range (µH)	3.3	1.8-4.7	
Normalized Volume (to Series #4)	1.22	1.28	
$P_{inductor}$ Measured (W)	2.40	2.20	
$P_{inductor}$ Vendor Calculator (W)	3.16	2.30	
ΔTemperature Measured (200 LFM) (˚C)	35.5	28.0	
ΔTemperature Vendor Calculator (˚C)	79.0	43.1	

IV. Multiphase Experimental Prototype

Implementing the optimization process of the previous sections to determine the switching frequency and inductor selection, an optimized experimental prototype was developed to target high efficiency and high power density. The block diagram is shown in figure 6(a) and the hardware is shown in figure 6(b). The experimental prototype contains five phase-shifted buck power stages described in Table IV.



(a)



(b)

Figure 6: Multiphase prototype (a) block diagram with buck IBC power stage cell schematic and phase hardware close-up (b) complete five phase hardware

TABLE IV: POWER STAGE COMPONENTS
(PER PHASE UNLESS SPECIFICALLY MENTIONED)

Component	Value
Power Devices	EPC2045 100 V, 7 mΩ eGaN®FET
Gate Driver	LM5113 Half-Bridge GaN FET Driver
Bootstrap Capacitor	100 nF Ceramic Capacitor 25 V, ±10%, X5R, 0402 SMD
Local Decoupling Capacitor	1 µF Ceramic Capacitor 25 V, ±10%, X5R, 0402 SMD
Input Capacitors (Qty=4)	1 µF Ceramic Capacitor 100 V, ±10%, X7S, 0805 SMD
Output Capacitors (decoupling) (Qty=4)	22 µF Ceramic Capacitor 25 V, ±20%, X5R, 0805 SMD
Output Capacitors (bulk) (Qty=3, for all phases combined)	180 µF OSCON (Organic Semiconductor) Capacitor 16 V, ±12%, 16SVPF180M
Inductor	3.3 µH, 7.7 mΩ, IHLP5050EZ-01

TABLE V: CONTROLLER AND SENSING CIRCUIT
(PER PHASE UNLESS SPECIFICALLY MENTIONED)

Component	Value
Microcontroller (Qty=1, for all phases combined)	Microchip dsPIC33E (16-bit)
Current Sense Amplifier	LT6105, 100 kHz BW
Current Sense Resistor	3 mΩ, 1%, 1W, 1206
Temperature Sensor (Qty=1, for all phases combined)	Microchip TC1047A, 3-pin SOT23-B

The phases are digitally controlled at a switching frequency of 500 kHz and full load current of 12 A per phase with an airflow of 200 LFM. The control scheme utilizes proportional-integral (PI) controllers to regulate the voltage as well as the upper limit on the total load current. The controller scheme is shown in figure 6(a). Each buck module in the figure consists of the power semiconductors, input capacitors, output capacitors (decoupling), driver circuitry and inductor. In addition to this, the controller incorporates current sharing among the phases, soft-start, temperature sense, and short

circuit protection. The control circuit parameters are listed in Table V. Typical waveforms for this closed-loop five-phase system, are shown in figure 7, which shows the output voltage feedback loop regulation during a load current transient of 12.5 A to 37.5 A to 12.5 A over a period of 2 ms.

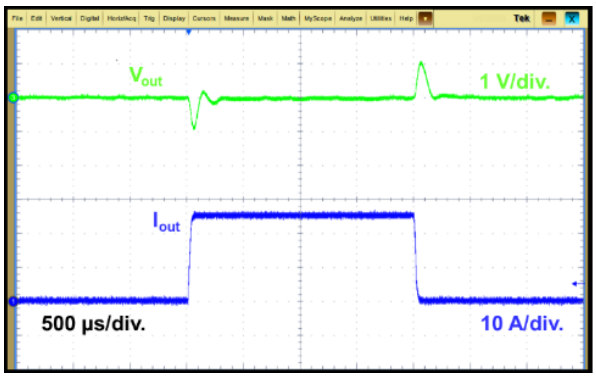
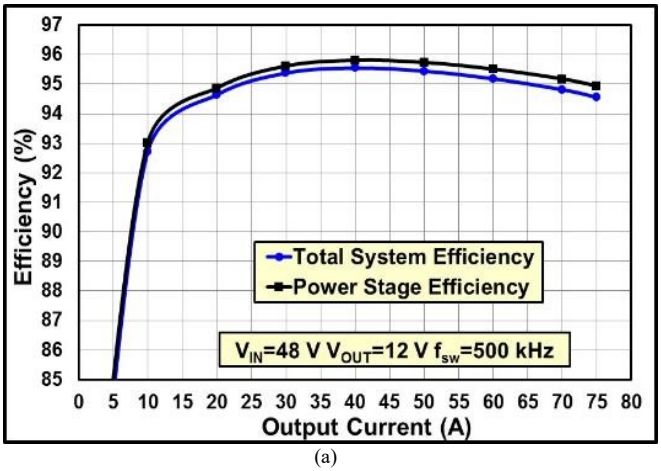


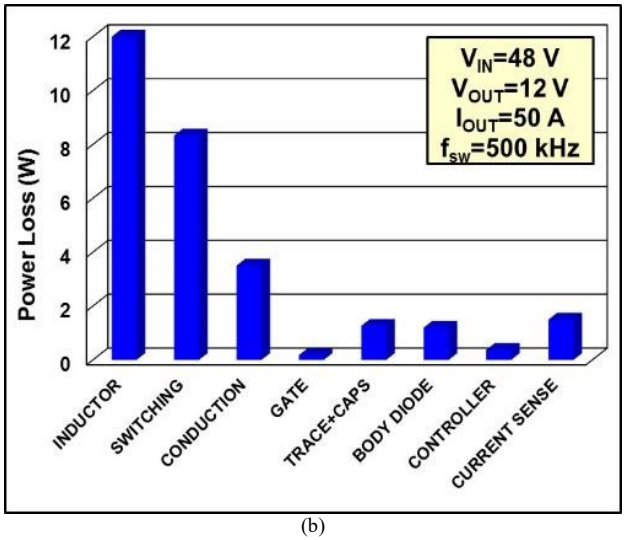
Figure 7: Typical Load Transient-12.5 A to 37.5 A to 12.5 A over a period of 2 ms

The measured efficiency of the prototype is shown in figure 8(a). The total efficiency, including power stage, controller, current sensing, temperature sensor, etc. reached a peak efficiency of 95.5% and a full load 60 A efficiency of 95.2%. When looking at the power stage efficiency of the buck module, efficiency at 60 A was measured to be over 95.5%.

A loss breakdown for the converter is shown in figure 8(b). From the loss breakdown, it can be seen that the inductor loss is significant, representing over 40% of the loss at 50 A of output current. The inductor also dominates design real estate, occupying 50% of the board area and 80% of the volume. The device loss, including conduction, switching loss, gate drive, and body diode conduction represents around 45% of the total loss. The remaining losses, from the controller, capacitors, PCB, and current sense making up the remaining 15%. The current sense in this prototype uses a discrete sense resistor in series with the output inductor and represents 5% of the total system loss at 50 A. In future designs, the current sensing could be more area-optimized by using the inductor DCR to sense phase current.



(a)



(b)

Figure 8: Electrical performance of IBC (V_{IN}=48 V, V_{OUT}=12 V, f_{sw}=500 kHz) (a) total system and power stage efficiencies (b) total system loss breakdown

The thermal performance of the prototype is shown in figure 9 with an air flow of approximately 200 LFM, with a picture of a zoomed-in power stage phase on the left and the corresponding thermal image on the right. At 60 A of output current and a measured ambient of 25°C, the hottest power device measured 97°C and the inductor measured approximately 73°C. There is no heatsinking applied in this case, which would improve the current handling capability of the prototype [20].

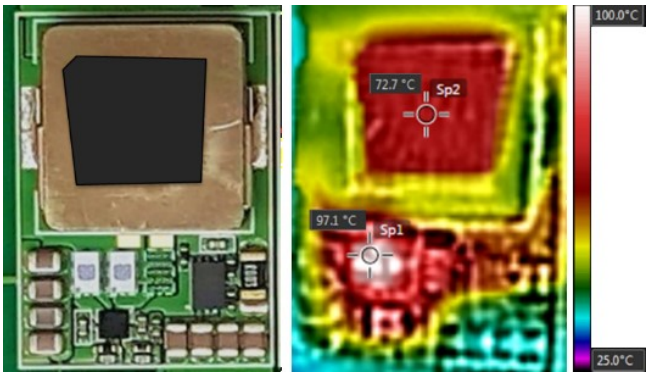


Figure 9: Thermal performance of a single phase in the IBC (V_{IN}=48 V, V_{OUT}=12 V, I_{out}=12 A, f_{sw}=500 kHz, air flow≈200 LFM)

V. Further Improving Performance

To further improve the performance of the prototype introduced in section IV, we will explore ways to improve both performance and power density in this section. First, we will focus on the power semiconductor device performance. The GaN optimized gate driver (table IV) used in the initial prototype has been available for over five years. The driver has a higher turn on resistance to slow turn on speed, required to minimize gate over-voltage for early eGaN FET designs. With improved chip-scale driver packages and significant improvements in over-voltage management techniques [21]

and circuit layout [22], newer GaN designs can be driven with faster, lower resistance gate drivers to further decrease loss for higher performance in higher frequency designs. A stronger prototype drive, with turn on and turn off gate resistances less than 1 **Ω**, was tested for comparison and the impact on power loss vs frequency for the system is shown in figure 10. The resulting power loss savings would translate to a 13% reduction in switching power loss or 0.2% efficiency improvement at 500 kHz. The power loss vs frequency curve becomes significantly flatter and at 1 MHz the efficiency improvement jumps to 0.5%.

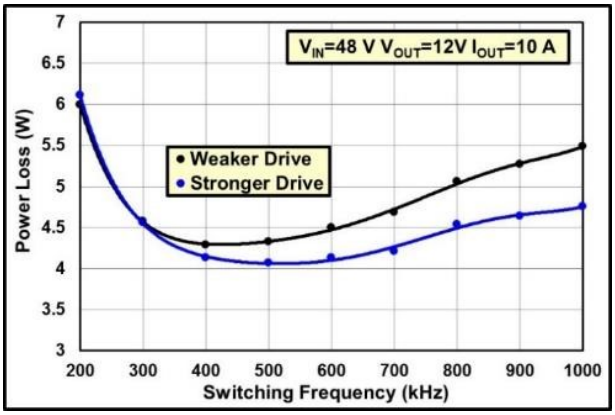
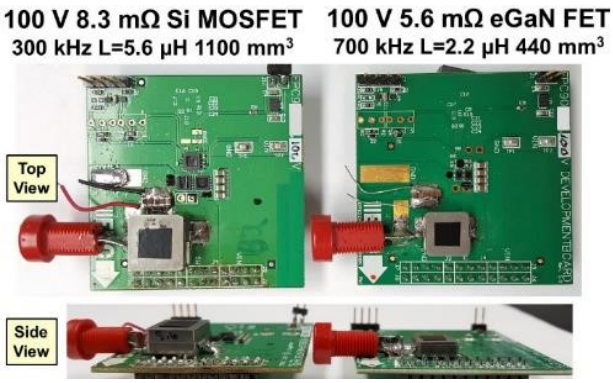


Figure 10: Experimentally measured impact of gate drive strength on system power loss for GaN transistor based converter for switching frequencies ranging from 200 kHz to 1000 kHz

We next will look at using the stronger gate drive to increase the frequency and reduce the inductor size, which dominated volume in the prototype in section IV. Using the inductor optimization data from section III, a switching frequency of 700 kHz and the smallest volume 2.2 µH inductor from series #1 (table III) were selected for the GaN prototype. For benchmarking purposes, a Si MOSFET based design was also compared. The Si MOSFET design used the same optimization procedure outlined earlier and a switching frequency of 300 kHz and the largest volume 5.6 µH inductor from series #7 (table III) were selected for the Si prototype.



(a) (b)

Figure 11: Experimental V_{IN}=48 V to V_{OUT}=12 V prototypes: (a) Si MOSFET based design with BSZ097N10NS5 Si MOSFETs, ISL2111 MOSFET 10 V gate drive, and 5.6 µH IHLP-5050FD-01 inductor (b) GaN transistor based design with EPC2045 eGaN FETs, stronger experimental prototype gate drive, and 2.2 µH IHLP-4040DZ-01 inductor

Figure 12 compares the electrical performance of the two prototypes from figure 11 and the advantage of GaN in power switching applications is clear. Using the improved electrical performance of GaN, the frequency is increased by over a factor of two over Si MOSFETs and the inductor, the component with the largest physical size and loss, is shrunk in volume by a factor of two and a half. With higher frequency and smaller size, the performance of the GaN based prototype still exceeds that of the Si benchmark for all load currents.

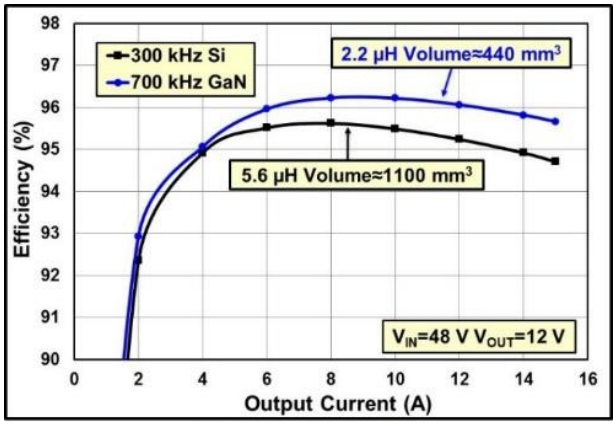


Figure 12: Experimental V_{IN}=48 Vto V_{OUT}=12 V electrical performance comparison based on prototypes in figure 11

Comparing the no air flow or natural convection thermal performance of the two prototypes in figure 13, the GaN based prototype performs slightly better, being able to conduct an additional 0.5 A of output current before reaching a 100°C thermal limit, which is purposely set well below the 150°C rating of both devices to account for higher potential ambient conditions. It should be noted that the GaN device is about a third of the size of the Si MOSFET and to achieve improved thermal performance in a such a small size, the device must first have significantly lower losses, and second, better thermal performance in the device package. The electrical performance advantage has been demonstrated throughout this paper and the chip-scale GaN package performs excellent thermally [20]. When previously comparing inductor performance, it could be seen that at higher frequencies, the core loss could be driven down. In this case, it allows the GaN based prototype to reduce the inductor volume by a factor of two and a half over the lower f_{sw} Si design, while maintaining similar thermal performance.

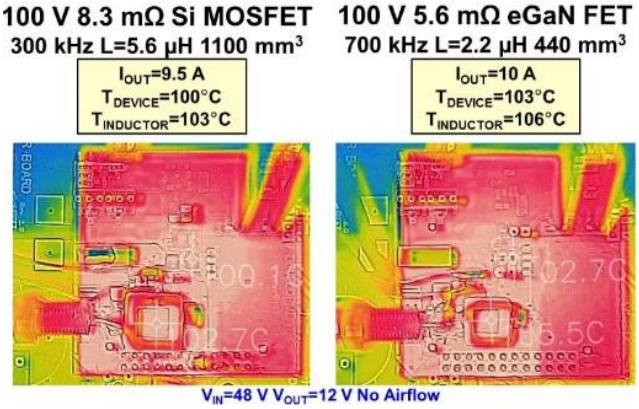


Figure 13: Experimental V_{IN}=48 Vto V_{OUT}=12 V thermal performance comparison based on prototypes in figure 11

VI. CONCLUSIONS

This paper has provided an optimization process for a fully regulated non-isolated 48 V_{IN} to 12 V_{OUT} intermediate bus converter. In section II, the latest power semiconductor technologies were evaluated, establishing that the GaN transistor provides smaller size and lower loss, and is a clear choice for higher switching frequency high density applications. In section III, the impact of frequency, inductance, and inductor size on system performance was examined; identifying the capability of higher frequencies to reduce inductor size and loss. Vendor inductor loss calculators were also compared against direct calorimetric hardware measurements of the switching converter to find the best performing inductor. In section IV, a fully regulated, digitally controlled, 720 W, 48 V to 12 V, 500 kHz IBC was demonstrated, achieving a full load efficiency of 95.2% and power density over 1000 W/in^3 and the relative performance is shown in figure 14. Section V assessed improvements that could be made to the prototype from section IV through the use of stronger gate drivers to increase the switching frequency and further reduce magnetic size. Also in section V, comparisons were made between independently optimized Si and GaN based designs, using the process developed in the previous sections. The projected/estimated performance of the designs from section V, implemented as systems similar to section IV, are plotted in figure 14.

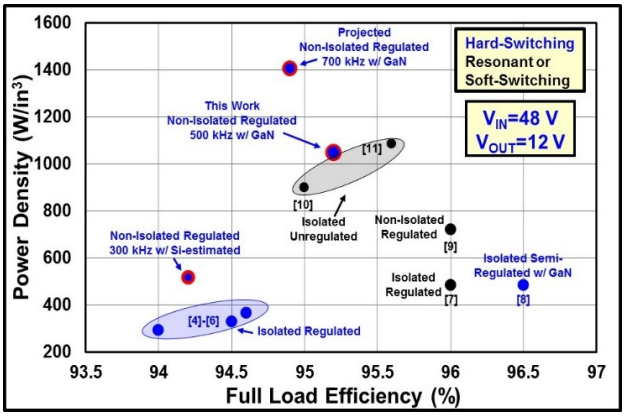


Figure 14: Comparison of full load efficiency and power density of state-of-the-art commercial products and previously published research and the fully regulated non-isolated buck IBCs presented in this work

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