A Current-fed DC-DC Converter Using Two Transformers With Reducing Current Ripple And Wide Input Range

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***Abstract*—A current-fed DC-DC converter is proposed for the fuel cells, which is suitable for the wide voltage conversion gain application. With the proposed control strategy, wide ZVS range can be achieved. Furthermore, there is no input current ripple in this way, which is beneficial for the fuel cells. The typical working mode of the proposed converter is given. The ZVS conditions for every switch are discussed in detail in this paper. The parameters design basing on the ZVS condition is also demonstrated. The effectiveness of the proposed method is verified by the simulation and experimental results of an 800W prototype.**

I. INTRODUCTION

Fuel cells are widely used in vehicles [1], mobile devices [2], distributed generation system [3], and so on. In these applications, the converters which connected with the fuel cells are required to suit wide input range with low current ripple.

As we know, the voltage-fed dual active bridge (VF-DAB) is a good choice as an interface between the high voltage DC bus and the fuel cells [4], under Single Phase Shift (SPS) control it can achieve all switches zero voltage switch (ZVS) [5,6]. But the input current ripple of VF-DAB is significant, which will reduce the working life of fuel cells [7,8]. Besides, the VF-DAB is not suitable for wide input voltage range.

To decrease the input current ripple, the current-fed full bridge DC-DC converter is a suitable solution [9], because of the staggered work of the half bridge's two legs. Besides, current-fed DC-DC converters have high voltage gain [10], and are easy to achieve ZVS [11].

This paper proposed a current-fed DC-DC converter with dual transformers. It adapt to the wide output voltage range of the fuel cell excellently. With the proposed control strategy, the input current ripple of the proposed converter can be reduced as much as possible.

In this paper, the operation principle is given in the first section including the topology and the main waveforms of the proposed converter. The ZVS conditions of every switch are analyzed in the second section. Section III illustrates the design process of transformers turns ratios. The experiment results are shown in section IV, which are used to verify the method proposed in this paper. The last section is the conclusion.

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II. OPERATION PRINCIPLE

Fig.1 illustrates the topology of the current-fed DC-DC converter with two transformers. In the fuel cell side, there are two boost-half bridges consisting of four MOSFETs (Q_1, Q_{1a}, Q_2, and Q_{2a}) and two DC inductors (L_1 and L_2). Besides, a clamping capacitor C_1 is connected with the two boost-half bridges in parallel. L_k is the leakage inductor at the input side. The output side comprises a full-bridge and an auxiliary half bridge, which share the same leg consisting of S_1 and S_2.Two high frequency transformers are used to link the two sides, which are connected in series at primary side, but in parallel at secondary side. The turn ratio of T_1 is 1:N_1, and 1:N_2 for T_2. v_{ab} denotes the voltage across the points 'a' and 'b' shown in Fig.1, and v_{cd} is the voltage across 'c' and 'd'. The current flowing through the leakage inductor L_k is denoted as i_{Lk}.

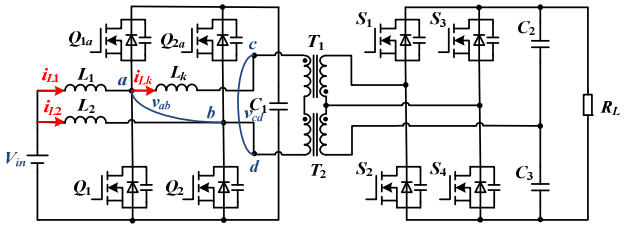
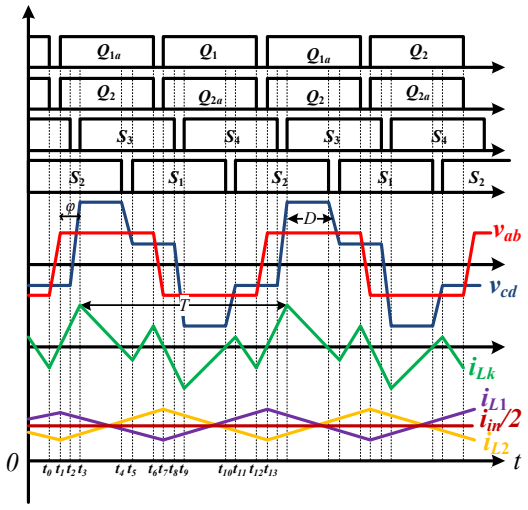


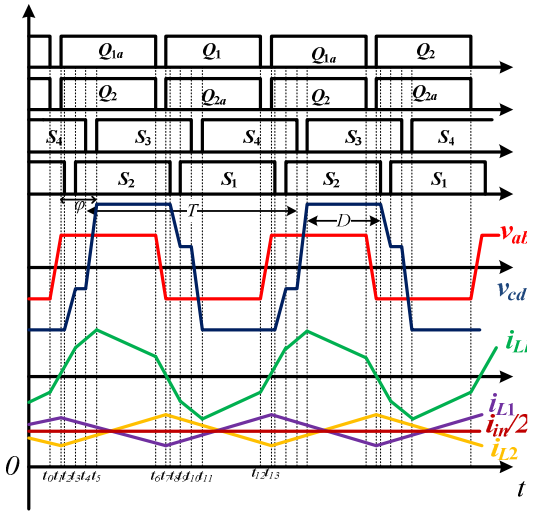
Fig. 1. Circuit of the current-fed DC-DC converter.

The steady-state waveforms when $0<\varphi<0.5-D$ and $\varphi>0.5-D$ of the proposed converter are shown in Fig.2. It should be noted that φ is the phase shift ratio between v_{ab} and v_{cd}, D is the duty cycle of secondary side. All of the MOSFETs are

driven by 50% duty cycle PWM waves. Q_1 and Q_2 are phase shifted by $T/2$, where T is the switching period. Q_{1a} and S_3 are phase shifted by φT. And the phase shift ratio between S_3 and



(a)



(b)

Fig.2. Steady state waveforms (a) $0<\varphi<0.5-D$, (b) $\varphi>0.5-D$.

S_1 is DT. Besides, Q_1 and Q_{1a}, Q_2 and Q_{2a}, S_1 and S_3, S_2 and S_4 operate complementarily.

In the case when $0<\varphi<0.5-D$, The leakage inductor current can be expressed as,

$$\begin{cases} i_{Lk}(t)=i_{Lk}(t_1)+(2V_{in}+V_o/2N_2)(t-t_1)/Lk, t\in(t_1,t_2] \\ i_{Lk}(t)=i_{Lk}(t_3)+(V_o/N_1+V_o/2N_2-2V_{in})(t-t3)/Lk, t\in(t_3,t_4] \\ i_{Lk}(t)=i_{Lk}(t_5)+(2V_{in}-V_o/2N_2)(t-t_1)/Lk, t\in(t_5,t_6] \end{cases} \quad (1)$$

In the case when $\varphi>0.5-D$, The leakage inductor current can be expressed as,

$$\begin{cases} i_{Lk}(t)=i_{Lk}(t_1)+(2V_{in}+V_o/(2N_2)+V_o/N_1)(t-t1)/Lk, t\in(t_1,t_2] \\ i_{Lk}(t)=i_{Lk}(t_3)+(V_o/N_1+V_o/(2N_2))(t-t_3)/Lk, t\in(t_3,t_4] \\ i_{Lk}(t)=i_{Lk}(t_5)+(V_o/N_1+V_o/(2N_2)-2V_{in})(t-t_1)/Lk, t\in(t_5,t_6] \end{cases} \quad (2)$$

Ignoring the dead band, it can be obtained,

$$\begin{cases} i_{Lk}(t_0)=i_{Lk}(t_1) \\ i_{Lk}(t_2)=i_{Lk}(t_3) \\ i_{Lk}(t_4)=i_{Lk}(t_5) \end{cases} \quad (3)$$

The current through L_1 can be expressed,

$$\begin{cases} i_{L1}=P_o/(2V_{in})+(V_{in}T)/(4L_1)-(t-t0)V_{in}/L_1, t\in(t0,t6] \\ i_{L2}=P_o/(2V_{in})-(V_{in}T)/(4L_1)+(t-t0)V_{in}/L_1, t\in(t6,t13] \end{cases} \quad (4)$$

Because the DC bias of leakage current is 0, and the two half cycle waveform are symmetric, it can be gotten,

$$\begin{cases} i_{Lk}(t_0)+i_{Lk}(t_6)=i_{Lk}(t_2)+i_{Lk}(t_{10})=i_{Lk}(t_4)+i_{Lk}(t_{13}) \\ \frac{1}{T}\int_{t0}^{t13} i_{Lk}(t)dt=0 \end{cases} \quad (5)$$

So, when $0<\varphi<0.5-D$,

$$\begin{cases} i_{Lk}(t_0)=\frac{T(N_1V_o-4N_1N_2V_{in}+4N_2DV_o-4N_1\varphi V_o)}{8L_kN_1N_2} \\ i_{Lk}(t_2)=\frac{T(N_1V_o-4N_1N_2V_{in}+4N_2TDV_{in}+16N_1N_2T\varphi V_{in})}{8L_kN_1N_2} \\ i_{Lk}(t_4)=\frac{T(N_1V_o-4N_1N_2V_{in}-4N_1DV_o+16N_1N_2DV_{in}+16N_1N_2\varphi V_{in})}{8L_kN_1N_2} \end{cases} \quad (6)$$

When $\varphi>0.5-D$,

$$\begin{cases} i_{Lk}(t_0)=-\frac{4N_1N_2TV_{in}-4N_2TV_o-3N_1TV_o+4N_1TDV_o+4N_2TDV_o+4N_1T\varphi V_o+8N_2T\varphi V_o)}{8L_kN_1N_2} \\ i_{Lk}(t_2)=\frac{T(N_1V_o-12N_1N_2V_{in}+4N_2TDV_o+16N_1N_2TDV_{in}+16N_1N_2\varphi V_{in})}{8L_kN_1N_2} \\ i_{Lk}(t_4)=\frac{T(4N_1TDV_o-4N_1N_2V_{in}-N_1TV_o+4N_2DV_o+16N_1N_2\varphi V_{in})}{8L_kN_1N_2} \end{cases} \quad (7)$$

III. Soft Switching Condition

The mode when $0<\varphi<0.5-D$ is defined as mode (a), and the mode when $\varphi>0.5-D$ is mode (b). The ZVS conditions are different in these two modes. According to Fig.2, assuming that ZVS is only determined by the polarity of leakage current i_{Lk} at the instant when the switches turn on, the ZVS conditions of the two modes are listed in Table. I.

TABLE I. ZVS Condition

	Q_1&Q_{2a}&Q_{1a}&Q_2	S_1&S_2	S_3&S_4
(a) $0<\varphi<0.5-D$	$i_{Lk}(t_0)<i_{L1}(t_0)$	$i_{Lk}(t_4)<0$	$i_{Lk}(t_2)>0$
(b) $\varphi>0.5-D$	$i_{Lk}(t_0)<i_{L1}(t_0)$	$i_{Lk}(t_2)>0$	$i_{Lk}(t_4)>0$

Assume the design demand is P_o=800W, V_{in}=18V~28V, V_o=400V, where P_o is the output power, V_{in} is the input voltage and V_o is the output voltage. To keep the voltage-second balance between the two ports of L_k, it is obtained,

$$D=N_1V_{in}/V_o-N_1/(4N_2) \quad (8)$$

Substituting (6), (7) and (8) into the expressions in Table I, The ZVS detail conditions are listed in Table. II (AS means always satisfied ZVS), where,

$$\begin{cases} N_1\varphi - 2N_2D + 4N_2D^2 + 4N_2D\varphi < 0 & (9) \\ 2N_1D - N_1 - 4N_2D + 2N_1\varphi + 8N_2D\varphi > 0 & (10) \\ 2N_1d - N_1 + 2N_1\varphi + 8N_2D\varphi > 0 & (11) \end{cases}$$

TABLE II. DETAIL ZVS CONDITION

	Q_1&Q_{2a}&Q_{1a}&Q_2	S_1&S_2	S_3&S_4
(a) 0<φ<0.5-D	AS	(9)	AS
(b) φ>0.5-D	AS	(10)	(11)

Taking N_1, N_2, D and φ into the consideration, it is easy to find that ZVS is difficult to be achieved in mode (b), so mode (b) should be avoided when the converter is designed. As for the S_1&S_2 in mode (a), ZVS can be achieved if the turn ratios N_1 and N_2 are designed properly.

IV. PARAMETERS DESIGN

The turn ratios of the two transformers should be designed to ensure the converter working in mode (a).

According to Fig.3, two restrictions can be obtained to make the converter always work in mode (a),

$$\begin{cases} \dfrac{V_o}{N_1} + \dfrac{V_o}{2N_2} > 2V_{in} \\ \dfrac{V_o}{2N_2} < 2V_{in} \end{cases} \quad (12)$$

When P_o=800W, V_{in}=18V~28V, V_o=400V, it can be gotten that

$$\begin{cases} N_2 > 5.5 \\ N_1 < \dfrac{1}{2V_{in}/V_o - 1/(2N_2)} \end{cases} \quad (13)$$

So,

$$N_1 < \left(\frac{1}{2V_{in}/V_o - 1/(2N_2)}\right)_{\min} = \left(\frac{1}{2V_{in}/V_o}\right)_{\min} = 7.1 \quad (14)$$

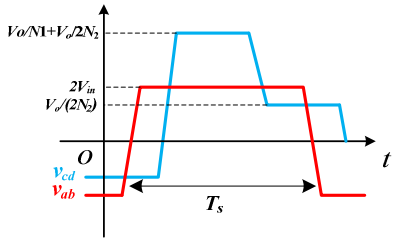


Fig. 3. The voltage between two ports of L_k.

According to the expression of i_{Lk_max}=i_{Lk}(t_2), if N_2 is too small, the current spikes of L_k will be very high. So let N_1=7.

The output power P_o can be expressed as,

$$P_o = \frac{TV_o^2}{4L_kN_1^2N_2^2}[A\varphi^2 + B\varphi + C] \quad (15)$$

Where,

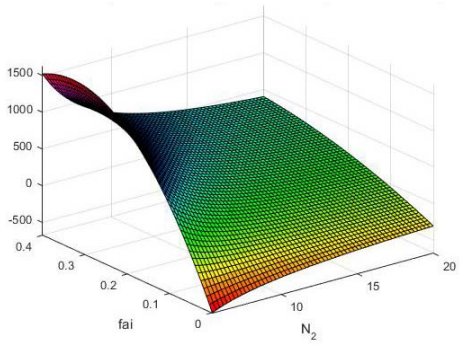


Fig.4. $P_o(\varphi,N_2)$ surface when D=0.1.

$$\begin{cases} A = -2N_1^2 - 8N_1N_2D \\ B = N_1^2 + 8N_1N_2D + 16N_2^2D^2 \\ C = 2N_1N_2D^2 - N_1N_2D + 8N_2^2D^3 - 4N_2^2D^2 \end{cases} \quad (16)$$

Fig.4 illustrates the $P_o(\varphi,N_2)$ surface when T=20μs, N_1=7, L_k=3.26μF, V_o=400V, D=0.1. In the same way, surfaces when D varies from 0 to 0.5 can be drawn. In the light of these surfaces in Fig.4, it can be obtained that the value of max P_o is reduced when N_2 is mounting. φ should be in the range of 0<φ<0.2 to ensure the output power is monotonically increasing with φ. When φ=φ_{max}=0.2, V_{in}=V_{in_max}=28V, it is most difficult to work in mode(a). So the value of D should be limited at this point,

$$D = \frac{\max(V_{in})N_1}{V_o} - \frac{N_1}{4N_2} < 0.5 - \max(\varphi) = 0.3 \quad (17)$$

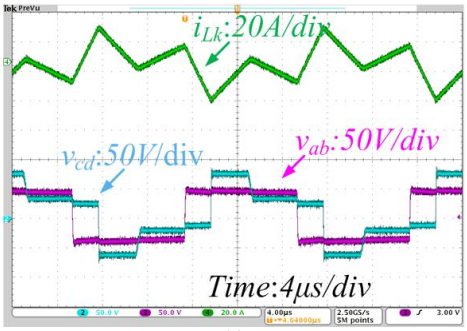
So it can be obtained that 5.5<N_2<9.2 according to (13) and (17). When the value of N_1 is determined to be 7, it can be proved that the maximum output power P_{o_max} is always larger than 800W, and the output power is monotonically increasing with φ when input voltage V_{in} varies from 18V to 28V.

V. EXPERIMENTAL RESULTS

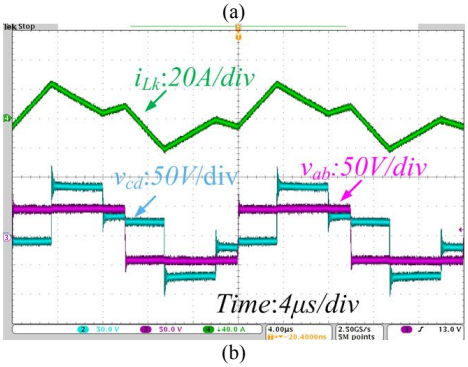
An 800W experimental prototype has been built in order to verify the effectiveness of the design and control of the current-fed DAB with dual transformers. The parameter specifications are shown in Table III.

TABLE III. SYSTEM SPECIFICATIONS

LVS voltage V_1	18V~28V	HVS voltage V_2	400V
Switching frequency f	50kHz	Rated power P_o	800W
DC inductance L_1, L_2	11μH	Clamp capacitance C_1	60μF
Turns ratio of $T1$(1:N_1)	5:35	Turns ratio of $T2$(1:N_2)	5:40
Leakage inductance L_r	3.26μH	Output capacitance C_2, C_3	10μF
junction capacitance	342pF	Dead time t_{dz}	250ns

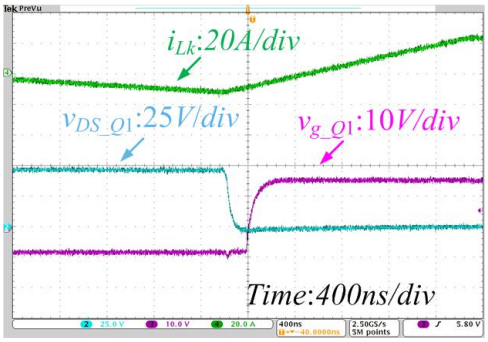


(a)



(b)

Fig.5. Steady waveforms when (a) P_o=285W, V_{in}=20.8V, V_o=400V,(b) P_o=800W, V_{in}=23V, V_o=400V.



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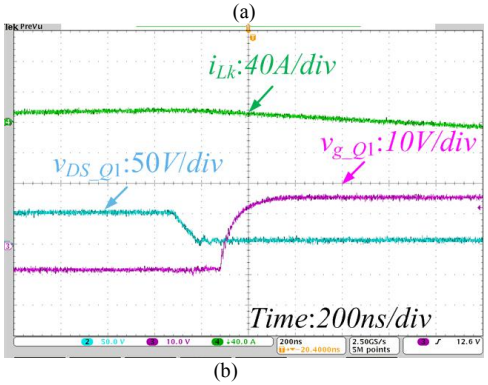
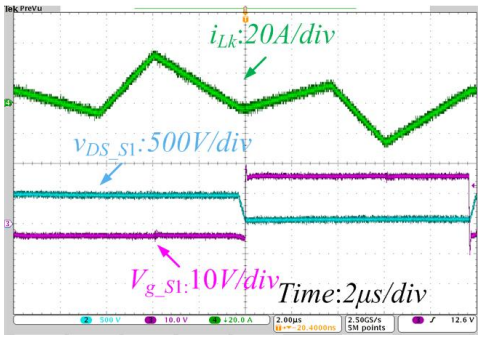


(b)

Fig.6. ZVS of Q_1 when (a) P_o=285W, V_{in}=26V, V_o=400V,(b) P_o=800W, V_{in}=24V, V_o=400V.



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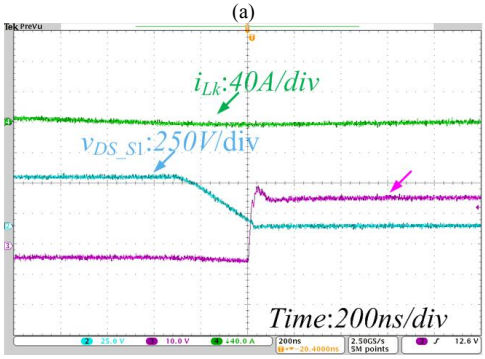


(b)

Fig.7. ZVS of S_1 (a) P_o=285W, V_{in}=22V, V_o=400V, (b) P_o=800W, V_{in}=23V, V_o=400V.

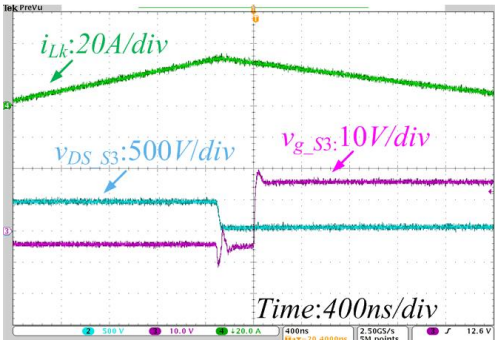


Fig.8. ZVS of S_3 when P_o=285W, V_{in}=22V, V_o=400V.

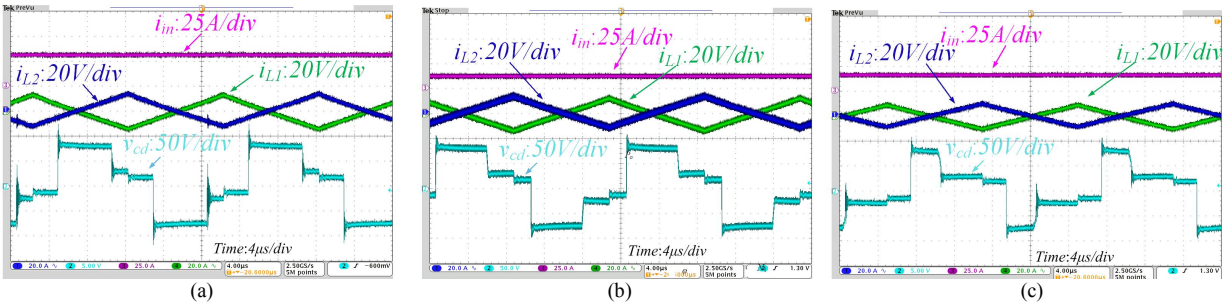
A. *Steady State Waveforms*

Fig.5 gives the steady state waveforms when P_o=800W. The voltage mutation in the voltage level of v_{cd}=V_o/N_2 is a result of the non-ideal transformers which have leakages. As the pictures show, the duty cycles are different when the input voltages are different, besides, the phase shift angle when the power is 800W is larger than the one when the power is 285W.

B. *Soft Switching Waveforms*

Fig.6. shows the ZVS waveforms of Q_1, demonstrating that the ZVS of the switches in the primary side can be achieved when the input voltages and output powers are not the same, because the ZVS conditions of Q_1, Q_2, Q_3 and Q_4 are the same.

The soft switching waveforms of S_1 with V_{in}=22V, P_o=285W and V_{in}=23V, P_o=800W are illustrated in Fig.7. S_1



(a) (b) (c)

Fig.9. Input current waveforms (a) P_o=800W, V_{in}=28V, V_o=400V, (b) P_o=285W, V_{in}=28V, V_o=400V, (c) P_o=285W, V_{in}=20V, V_o=400V

and S_2 are the two most difficult to achieve soft-switching for MOSFETs.

Fig.8 illustrates the ZVS situations of S_3 with V_{in}=22V, P_o=285W. For S_3 and S_4, ZVS always can be achieved.

C. Input Current Waveforms

Fig.9 illustrates the input current waveforms with different power and different input voltage. The three pictures demonstrate the current ripple-free is achieved obviously under the proposed control. And the proposed converter can work in wide input range.

VI. Conclusion

This paper proposed a current-fed DC-DC converter for fuel cells applications. The proposed converter can work when the input voltage varies in a wide range, and the input current ripple is reduced effectively. The ZVS conditions of every switch in different work modes are analyzed. Turns ratios are designed to achieve ZVS in wide voltage range, and the design process is given in detail. The closed loop control of proposed control is easy to be implemented since there is just one variable which is the phase shifted angle. All the methods proposed in this paper are verified by the experiment results.

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