Duty Phase Shift Technique for Extended-Duty-Ratio Boost Converter for Reducing Device Voltage Stress Over Wider Operating Range

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***Abstract*—This paper proposes a modified duty phase shift technique for an M-phase extended-duty-ratio (EDR) boost converter to facilitate the inherent current sharing property and reduced voltage stress on the switching devices of the EDR converter over wider operating region. With conventional phase shift of $(360/M)^\circ$ among the operating phases, a reduced voltage stress and inherent current share between the interleaved boost phases is only possible for the operating region of duty ratio given by $(M-1)/M \leq D \leq 1$, with a minimum gain of M^2. However, for a wide range of input-output application with the need of extended range of voltage conversion gain, the converter will operate over broader duty ratio range. With the proposed duty phase shift technique, the advantages of EDR converter of inherent current sharing and reduced voltage stress on the active devices can be restored over wider operating range allowing a minimum gain of $2M$. The method is validated with extensive simulation results from multi-phase EDR boost and experimental results from a 250 W 3-phase EDR boost with GaN-based hardware prototype operating at 200 kHz switching frequency.**

***Index Terms*—Extended duty ratio converter, high voltage step up, interleaved boost, multi-phase converter, reduced voltage stress, switched capacitor.**

I. Introduction

An extended-duty-ratio (EDR) boost is a high gain non-isolated dc-dc converter which inherits the merits of switched capacitors and interleaved inductor technique and offers lower converter losses as most of the switches encounter lower voltage stress. Further the inductor current being interleaved, the corresponding core and copper losses are reduced. [1]–[6] are the other popular high gain non-isolated dc-dc converters available in literature based on interleaved/coupled inductor boost, switched capacitor, voltage multiplier cell, or a combination of them. Authors of [7] have presented a review of the high gain boost converters.

For an M-phase EDR boost converter, the current is inherently shared among all the boost phases and voltage stress on the active switches is $1/M$ of the output voltage for duty ratio in the operating region of $(M-1)/M \leq D \leq 1$ [8]–[11]. But for applications with wider operating region with the need of lower duty ratio, the inherent current sharing property is lost. More importantly, the voltage stress on the bottom switches are not limited to $1/M$ of the output voltage, necessitating the use of higher voltage rating switches with higher R_{DS_ON} (which almost varies proportionally with the square of the blocking-voltage). Thus it impacts the overall efficiency of the converter.

A sensor-less current sharing technique for 3-phase EDR boost converter is provided in [12] for wide operating range, however, a generalized approach is difficult to achieve for higher number of phases. Further, even this technique does not ensure the voltage stress on the bottom switches to be limited to $1/M$ of the output voltage. In this paper, a duty phase shift technique is proposed to expand the current sharing property over a wider range of duty ratio, $0.5 \leq D \leq 1$, instead of only $(M-1)/M \leq D \leq 1$ for an M-phase EDR boost converter. Also, the voltage stress on the bottom switches can be limited to $1/M$ of the output voltage. This technique does not impact the voltage boost attainable with the conventional phase shift approach, but affects the input current ripple. Further, the input current ripple reduction is different for odd and even number of phase implementation of EDR boost which is thoroughly analyzed in this paper. The proposed concept is validated with simulation results for a generalized M-phase EDR boost converter and with experimental results from a 250 W, 3-phase EDR boost, GaN-based hardware prototype.

The rest of the paper is organized as follows. Section II gives a detail of the basic M-phase converter topology and its operating principles. The duty phase shift technique to ensure current sharing between phases and limiting the voltage stress on the bottom switches is given in the following Section III along with the

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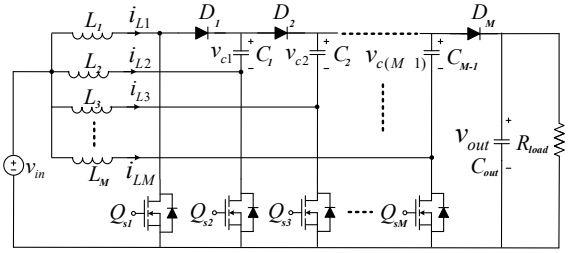


Fig. 1. Topology for M-phase EDR boost converter.

simulation results. An input current ripple is analysed for even and odd number of phase implementation. The experimental results for the GaN-based 3-phase EDR boost converter are provided in Section IV for validation of the analytical and simulation results. Finally a conclusion of the presented work is drawn in Section V.

II. M-PHASE EXTENDED DUTY RATIO BOOST

Fig. 1 shows the non-synchronous M-phase EDR boost topology whose equivalent buck structure has been exploited in voltage regulator (VR) and point of load (POL) applications in [13]–[15]. EDR converter variations are reported in some of the recent works [16], [17] for voltage step-down applications.

The upper switches (implemented with SiC diodes) of each phase are complementary to the corresponding lower switches (implemented with GaN MOSFETs in the present work). The high frequency energy storage capacitor C_M is placed in between the upper and lower switch of each phase which gets charged to a factor of the output voltage. For conventional implementation, the phases are interleaved with a phase difference of $(360/M)^\circ$.

A. Operating principles

The operation of EDR boost converter can be divided into M different number of zones depending on the duty ratio D of operation, with independent combination of the operating modes. For $(M-1)/M \leq D \leq 1$ corresponding to Zone I operation, the operating modes comprise of either all the phases being simultaneously ON, or only one of the phases being OFF in a particular pattern depending on the phase sequence. The converter gain for corresponding operation is given in (1).

$$k = \frac{v_{out}}{v_{in}} = \frac{i_{L1} + i_{L2} + ... + i_{LM}}{i_o} = \frac{M}{(1-D)} \quad (1)$$

Zone I operation is of interest as it is the only operating region of inherent equal current sharing and reduced switch voltage stress. The operation in other zones can be referred from [12] for 3-phase EDR boost.

B. Voltage stress and current sharing

For the duty ratio in the range of $(M-1)/M \leq D \leq 1$ corresponding to a minimum voltage gain of M^2, the voltage stress on the bottom devices is $1/M$ of v_{out}. The stress on the top switches for the first $(M-1)$ phases is $2/M$ of v_{out}, while for the M^{th} phase it is $1/M$ of v_{out}. Also, the input current is inherently equally shared among all the boost phases. But for wider operating range with varying voltage gain requirement, the voltage stress on most of the switches is increased requiring switches with higher voltage rating and higher R_{DS_ON}, increasing the conduction loss of the converter. Also, the current sharing property is lost once the required voltage gain is reduced than M^2 and additional duty ratio modification is required to ensure current sharing.

III. DUTY PHASE SHIFT TECHNIQUE

The duty of each phase is shifted by 180° instead of the conventional $(360/M)^\circ$, thus duty of each alternate phases are in-phase, while duty of any two adjacent phases are out-of-phase. With duty ratio in range of $0.5 \leq D \leq 1$ (corresponding to a minimum voltage gain of $2M$), this technique implies that the next phase is turned-on at least before the turn-off of the previous phase, ensuring the inherent current sharing between all the input phases and limiting the voltage stress of all the bottom switches to $1/M$ of the output voltage. For 2-phase implementation, both the conventional and modified phase shift techniques result the same. The modified technique is particularly beneficial as the number of phases increases, by extending the duty ratio range from $(M-1)/M$ to a minimum of 0.5. It is to be noted that for $0.5 \leq D \leq 1$ with modified phase shift technique, the converter gain remains the same as given in (1), but the input current ripple is increased than the conventional approach.

A. Input current ripple

For an M-phase EDR boost converter with duty ratio in the range $(M-1)/M \leq D \leq 1$, for a given v_{out} the input current ripple Δi_{L_con} is reduced by $1/M$ for a fixed D as given in (2). In fact, as can be seen it is a complex function of the number of phase and duty ratio. Also, its effective switching frequency is increased by M times as is illustrated in Fig. 3.

$$\Delta i_{L\_con} = \frac{v_{in}(MD-(M-1))}{Lf_s} = \frac{v_{out}}{Lf_s}(1-D)(MD-(M-1))\frac{1}{M} \quad (2)$$

In contrast, the equivalent input current ripple with modified phase shift technique is not much reduced, in fact, for odd number of phase implementation, the ripple is higher than the individual phase current ripple (though

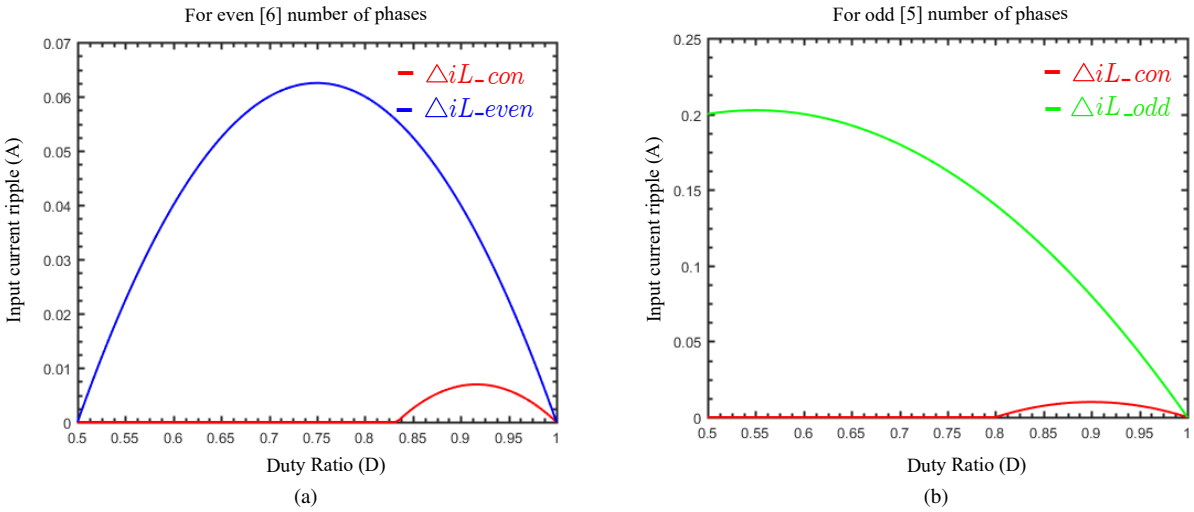


Fig. 2. Comparison of the input current ripple for odd and even number of phase implementation of EDR boost with modified duty phase shift technique and with conventional approach (shown only in the range $(M-1)/M \leq D \leq 1$) for a fixed output voltage.

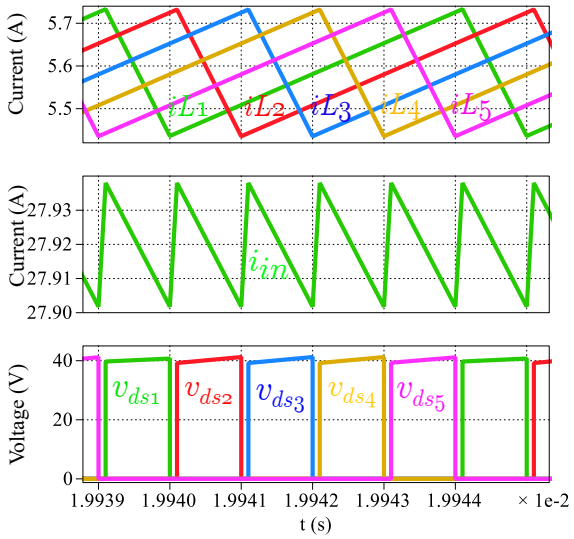


Fig. 3. Simulation waveforms for 200 W, 200 V output, 200 kHz switching frequency, 0.82 duty ratio with conventional approach for 5-phase EDR boost converter with 7.5 V input showing the converter phase and input currents and device voltage stress.

it does not affect the converter's efficiency as the ripple current on individual phase inductor remains the same). This is a disadvantage for the proposed method, but can be addressed in the design stage with higher inductance value to limit the total input ripple within a specified percentage. Further, it is interesting to note that the ripple component in the input current is not the same for even and odd number of EDR boost implementation.

1) Even number of phases: For even number of phases, the input current ripple Δi_{L_even} is smaller than the individual boost phases as given by (3), which is a function of the phase duty ratio D. The ripple decreases with smaller D and is ideally 0 for $D = 0.5$. Further, its equivalent frequency is only twice of the switching frequency unlike with the conventional approach (illustrated in Fig. 4a).

$$\Delta i_{L\_even} = \frac{v_{in}}{Lf_s}(2D-1)\frac{M}{2}$$
$$= \frac{v_{out}}{2Lf_s}(1-D)(2D-1) \quad (3)$$

2) Odd number of phases: For odd number of phase, the input current ripple Δi_{L_odd} is higher than the even number of phases as given in (4) by a term which is again a function of D for a fixed output voltage and given circuit parameters. The ripple decreases with smaller D and reaches a minimum for $D = 0.5$, but unlike for even number of phases, it is not 0. Also its equivalent frequency is same as the switching frequency (illustrated in Fig. 4b).

$$\Delta i_{L\_odd} = \Delta i_{L\_even} + \frac{v_{in}}{2Lf_s}$$
$$= \Delta i_{L\_even} + \frac{v_{out}}{2Lf_s}(1-D)\frac{1}{M} \quad (4)$$

Fig. 2 shows a comparison of the input current ripple for odd and even number of phase implementation of EDR boost with modified duty phase shift technique and with conventional approach. The plots illustrate input ripple (normalized by $v_{out}/(Lf_s)$) vs the duty ratio for a fixed output voltage for $M = 6$ (even M shown in Fig. 2a) and $M = 5$ (odd M shown in Fig. 2b).

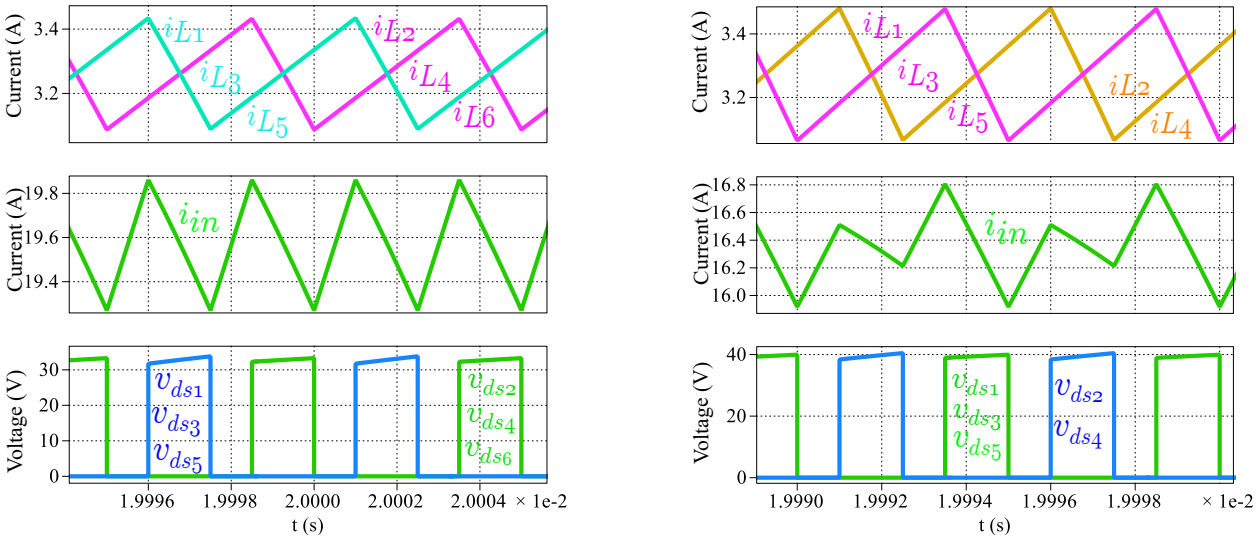


Fig. 4. Simulation waveforms for 200 W, 200 V output, 200 kHz switching frequency, 0.7 duty ratio with modified phase shifted technique showing the converter phase and input currents and device voltage stress for (a) even [6] number of phases with 10 V input, (b) odd [5] number of phases with 12 V input.

B. Device voltage stress

The voltage stress on the bottom devices is always $1/M$ of v_{out} for the duty ratio in the range $0.5 \leq D \leq 1$. The stress on the top switches are different for different phases. For first $(M-1)$ phase, it is $2/M$ of v_{out}, while for the M^{th} phase it is $1/M$ of v_{out}. Also the alternate device voltages are in-phase as expected.

C. Simulation waveforms

Fig. 4 shows the simulated waveforms for the even and odd number of phases with EDR boost implementation for 200 W, 200 V output, 200 kHz switching frequency, 100 μH inductor, and 0.7 duty ratio ($0.5 \leq D \leq 1$ for inherent equal current sharing) with modified phase shifted technique. Fig. 3 gives the corresponding waveforms for 5-phase EDR boost converter with 7.5 V input, 0.82 duty ratio ($0.8 \leq D \leq 1$ for inherent equal current sharing), and conventional duty approach, i.e., with 72° phase-shift. The phase currents as well as the device voltages are also phase-shifted by 72°. Also it is observed that the current is inherently equally shared among all the boost phases and the voltage stress is 40 V ($1/M$ of v_{out}) only in this operating range.

The converter phase and input currents and device voltage stresses are illustrated for 6-phase EDR boost with 10 V input in Fig. 4a where i_{L3} and i_{L5} are in-phase with i_{L1}, and i_{L4} and i_{L6} are in-phase with i_{L2}. Similar is true with voltage stress. The input current ripple is smaller with equivalent frequency half of the actual switching frequency as discussed. Similarly, from Fig. 4b with 5-phase EDR boost with 12 V input, it can be observed that the alternate phases are in-phase, with the input current ripple higher than the individual boost phase ripple current, and the equivalent frequency same as the switching frequency. Also in both the cases it can be seen that the current is inherently equally shared among all the boost phases and the voltage stress is $1/M$ of v_{out} (33.5 V and 40 V for 6-phase and 5-phase EDR boost converters respectively).

TABLE I
COMPONENT DETAILS

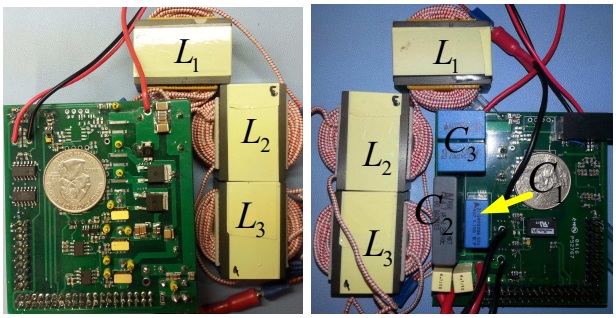
Component	Parameters
C_1 , C_2 , C_3	4.7 μF/ 100 V, 4.7 μF/ 200 V, 4.7 μF/ 300 V
L_1 , L_2 , L_3	180 μH
Q_{s1} , Q_{s2} , Q_{s3}	GS66508T
D_1 , D_2 , D_3	C3D04060E (2), SBR10U200

IV. HARDWARE PROTOTYPE AND EXPERIMENTAL RESULTS

A. Hardware prototype

A 250 W GaN based hardware prototype for 3-phase EDR boost as shown in Fig. 5, has been built to implement the proposed duty phase shift technique. Table I gives the passive and active component details for the hardware set-up. Planar E38/8/25-3F3 with Litz wire has been used as the inductor core to obtain a low profile design and lower conduction loss.

UCC27511 from Texas Instruments has been used as gate driver and digital isolator Si8610BB from Silicon Labs is used for isolating the PWM signals from the



(a) (b)

Fig. 5. Experimental prototype for 3-phase EDR boost showing (a) top view, (b) bottom view.

control and power sections. The auxiliary power supply for the control section is derived externally. EZDSP TMSF28335 has been used to generate the 200 kHz interleaved PWM signals. LeCroy 6200A oscilloscope is used to capture the relevant waveforms. A load resistor of 200 Ω is used for the experiment.

B. Experimental results

Figs. 6 and 7 shows the boost inductor currents, input current, and input, output, and device voltages for 3-phase EDR boost converter for each of duty ratio 0.7 and 0.5 for all the phases. Fig. 6 illustrates the results with 120° phase-shift whereas, Fig. 7 illustrates the results with 180° phase-shift. With 120° phase-shift, the current is shown to be shared among all the inductors for only Fig. 6a with duty ratio 0.7 (where $(M-1)/M \leq D \leq 1$). But for Fig. 6b with duty ratio 0.5, it is not shared. Also the voltage stress on the switches is no more $v_{out}/3$, but $2v_{out}/3$.

On the contrary, with 180° phase-shift, the current is shown to be shared among all the inductors for both Figs. 7a and 7b with duty ratio 0.7 and 0.5 respectively, as expected. Also the voltage stress on the switches is always $v_{out}/3$. Further with odd number of phase implementation, the input current ripple can be seen to be higher in Fig. 7 (equivalent frequency as 600 kHz) than in Fig. 6a, (equivalent frequency as 200 kHz, same as the switching frequency) as already discussed earlier.

V. Conclusion

In this paper a modified duty phase shift technique for an M-phase extended-duty-ratio (EDR) boost converter to facilitate the inherent current sharing property and reduced voltage stress on the switching devices of the EDR converter over wider operating region has been discussed. Thus switches with lower voltage rating and thus lower R_{DS_ON} and conduction loss can be used. The input current ripple reduction is different for odd and even number of phase implementation which is thoroughly analyzed. The proposed concept is validated with simulation results from a generalized M-phase EDR boost converter and experimental results from a 250 W, 3-phase EDR boost, GaN-based hardware prototype operating at 200 kHz switching frequency.

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Disclaimer

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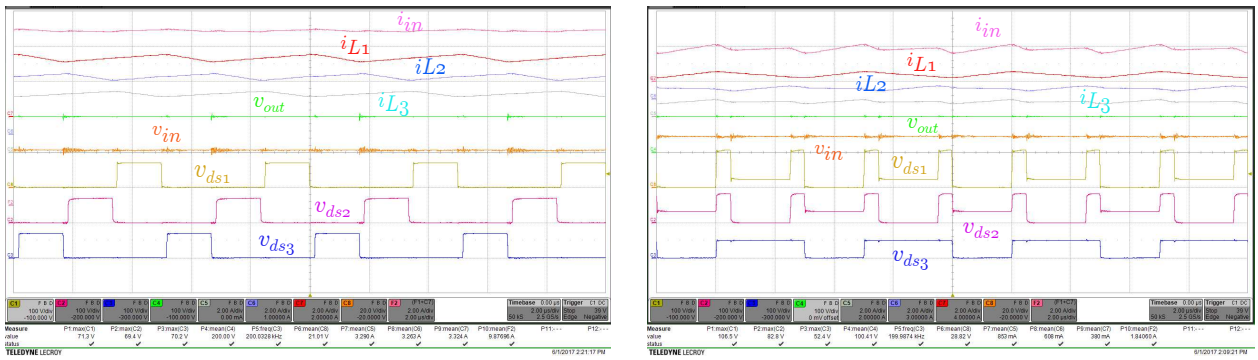
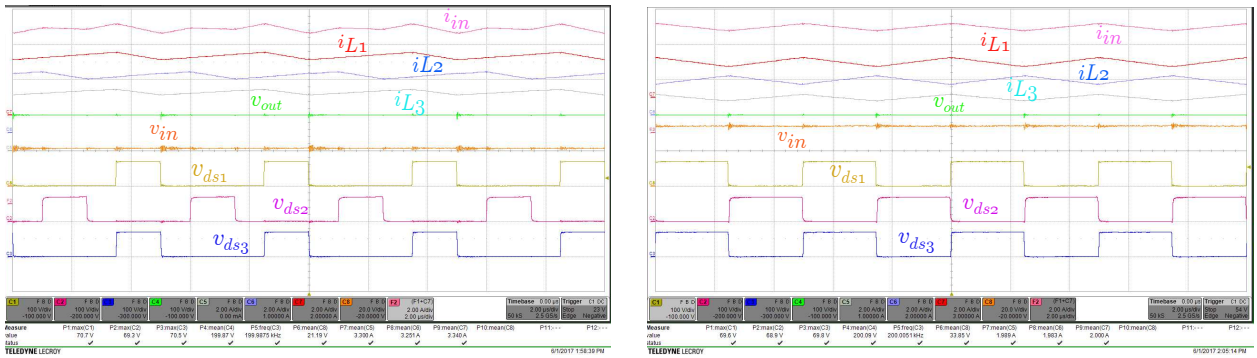


(a) (b)

Fig. 6. Experimental waveforms illustrating each boost inductor currents, input current, and input, output, and device voltages with conventional approach of 120° phase-shift for 3-phase EDR boost (currents: 2 A/div, v_{in} : 20 V/div, other voltages: 100 V/div, time : 2 μs/div) for (a) D = 0.7, (b) D = 0.5.



(a) (b)

Fig. 7. Experimental waveforms illustrating each boost inductor currents, input current, and input, output, and device voltages with modified duty phase shift technique of 180° for 3-phase EDR boost (currents: 2 A/div, v_{in} : 20 V/div, other voltages: 100 V/div, time : 2 μs/div) for (a) D = 0.7, (b) D = 0.5.

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