Modeling and Dynamics Investigation of an Active-Clamp Buck Converter

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***Abstract*—In this paper, an accurate averaged model of an active-clamp buck converter is presented. An insightful and straightforward derivation method is developed for dealing with signals with large ripple. The large and small signal models are derived and verified through detailed simulations. For the control-to-output bode diagrams, the Simplis simulation result shows a good match with the derived model. Then, an investigation of the active-clamp buck dynamics and the guideline for choosing the clamp capacitor values are provided.**

Keywords—active-clamp buck converter; dc-dc converter; soft-switching; zero-voltage-switching; converter modeling; large signal model

I. INTRODUCTION

Active-clamping has been widely used for achieving zero-voltage-switching (ZVS) for isolated dc-dc converters since it was introduced for actively resetting of the transformer in a forward converter [1], [2]. This technique could also be applied for non-isolated dc-dc converters [4], [4]. Active-clamp buck converter is a suitable topology for many non-isolated low power step down applications [5]. Fig. 1 shows the circuit diagram of an active-clamp buck converter. It features high conversion efficiency and low EMI noise simultaneously by realizing ZVS for all three active-switches and soft turn-off of body diode of the synchronous rectifier (SR).

The analytical model is important for studying the dynamics and designing the proper compensator of the active-clamp buck converter shown in Fig. 1. Reference [6] provides a large-signal transient model for active-clamp forward converter by using average-stage-trajectory approach, but the effect of resonant current is not included in the model. A full-order averaged model for active-clamp SEPIC converter is derived in [7] with better accuracy but also with much more complexity. References [8] and [9] present two reduced-order models for active-clamp SEPIC and active-clamp flyback converters, respectively, based on symbolic analysis methods. In this paper, a more straightforward and insightful averaged large-signal model for active-clamp buck converter is firstly derived, with reduced-order but high accuracy. Then, the small-signal performance is characterized and verified by Simplis simulation. Following the model derivation, the converter dynamics is investigated. Last is the conclusion and future work.

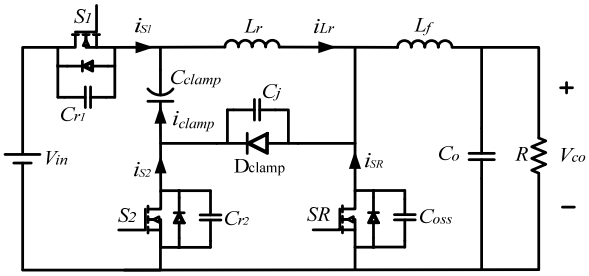

Fig. 1. Circuit diagram of the active-clamp buck converter.

II. CIRCUIT OPERATING PRINCIPLE AND MODEL SIMPLIFICATION

A. Operating principle of the active-clamp buck converter

In the circuit shown in Fig. 1, L_f and C_o are the output filter; C_{clamp}, L_r and D_{clamp} are the soft-switching branch components. Compared with the output filter L_f, the inductance of L_r is much smaller in order to achieve zero-voltage-switching of S_1 for a very high switching frequency. The clamp capacitor C_{clamp} creates a small negative voltage in the circuit which is needed to flip the direction of i_{Lr} during operation. The key operating switching waveform of the active-clamp buck converter in a switching cycle is illustrated in Fig. 2. The circuit has five operating modes corresponding to different time intervals in the switching cycle. The description of each operating mode is as follows:

1) Mode 0 ($-t_0$): Before switch S_1 is turned off, the load current flows through S_1, L_r and L_f. SR is off and blocking the input voltage V_{in}. S_2 is off and blocking the input voltage plus the clamping voltage of C_{clamp}, namly $V_{in} + v_{clamp}$. D_{clamp} is blocking clamping voltage v_{clamp}.

2) Mode 1 ($t_0 - t_1$): This time interval is the deadtime after switch S_1 is turned off and before S_2 and SR are turned on. The load current is charging C_{r1} and discharging C_{r2} and C_{oss}. C_j is also discharged and D_{clamp} becomes forward biased in the middle of this time interval. C_{clamp} starts to discharge L_r after D_{clamp} becomes forward biased. By the end of this operating mode, C_{r2} and C_{oss} are fully discharged and the body diodes are forward biased.

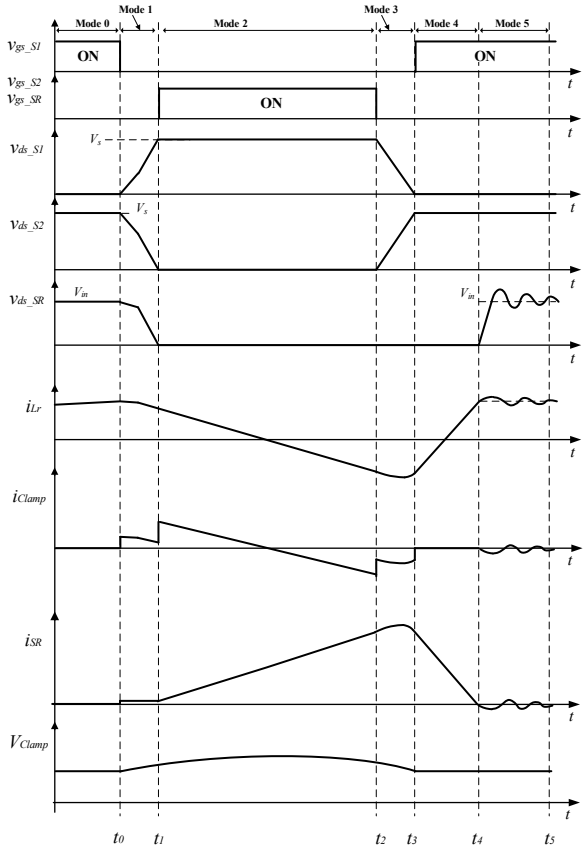

Fig. 2. Key operating waveforms.

3) Mode 2 ($t_1 - t_2$): At the beginning of mode 2, SR and S_2 are soft turned on as body diodes are forward biased. L_r continues to get discharged by C_{clamp} and its current becomes negative by the end of this time interval. As i_{Lr} decreases in this mode, i_{SR} increases accordingly to provide the load current.

4) Mode 3 ($t_2 - t_3$): After SR and S_2 are turned off, L_r starts to resonate with C_{r1}, C_{r2} and C_j. The body diode of SR is still forward biased which keeps its voltage as zero. By the end of this mode, voltage of C_{r1} is discharge to zero. At the same time, voltages of C_{r2} and C_j are both charged to $V_{in} + v_{clamp}$.

5) Mode 4 ($t_3 - t_4$): S_1 is turned on with ZVS since its body diode is conducting current. i_{Lf} starts to rise until it reaches the amount of load current. At the same time, i_{SR} starts to decrease until it reaches zero.

6) Mode 5 ($t_4 - t_5$): Since the voltage across SR is still zero by the end of mode 4, SR will start resonate with L_r and C_j after i_{Lr} decreases to zero. It can be shown that the final steady state voltages of SR and C_j are V_{in} and v_{clamp} respectively. If the circuit impedance is small, the oscillation might not be fully damped out before t_0 of the next switching cycle, however, the resonance peak of voltage across swithc SR is limited by $V_{in} + v_{clamp}$ and part of the energy is saved in the clamp capacitor.

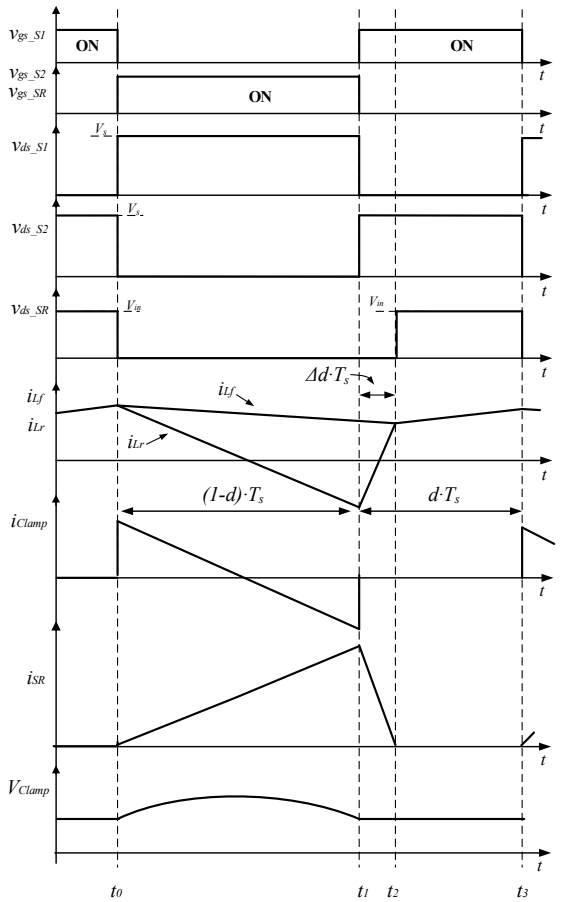

Fig. 3. Key operating waveforms after modeling assumptions.

B. Model assumptions and approximations

The modeling and dynamic study of the converter are of interest in the frequency range of below half switching frequency since the system gain at high frequency range is normally well damped by the filters. Therefore, some high frequency attributions of the converter are removed from the waveforms shown in Fig. 2 to simplify the modeling process. The assumptions made in this paper includes:

1) Resonant transition modes (mode 1 and mode 3) are ignored, since the intervals of these two modes are very small compared with the entire switching period.

2) Reonance after SR body diode turn-off in mode 5 is ignored.

3) The circuit parasitics (C_{r1}, C_{r2}, C_{oss} and C_j) are not considered during the modeling process.

With the above assumptions, the operating waveforms are modified and shown in Fig. 3. The converter model equations are derived based the modified waveforms.

III. LARGE-SIGNAL MODEL DERIVATION

As shown in Fig. 3, it is reasonable to assume v_{clamp}, i_{Lf} and v_{Co} have small ripple. Thus, the average values in one switching cycle V_{clamp}, I_{Lf} and V_{Co} are picked as the state variables of the

system state-space model. The input voltage V_{in} and duty cycle d are considered as model inputs. Firstly, the state-space equations for three different intervals [t_0, t_1], [t_1, t_2] and [t_2, t_3] will be derived separately. Then, the combined model equations for the entire switching cycle can be derived based on state-space averaging method.

As seen in Fig. 3, there is a $\Delta d \cdot T_s$ interval indicating the duty cycle loss of the active-clamp buck converter. Therefore, the averaged voltage at the point before the output L_f - C_o filter (drain node of SR) is determined by Δd, which is an intermediate variable between state variables and output. It is hence important to derive the expression for Δd with state variables, model inputs and circuit parameters. According to Fig. 3, Δd can be calculated based on the incremental value of i_{Lr} during this interval:

$$\frac{\Delta d V_{in}}{L_r} = \frac{(1-d)V_{clamp}}{L_r} - \frac{(1-d)V_{C_o}}{L_f} - \frac{\Delta d V_{C_o}}{L_f} \quad (1)$$

The following equation can be written by rearranging (1):

$$\Delta d = \frac{(1-d)L_f V_{clamp} - (1-d)L_r V_{C_o}}{L_f V_{in} + L_r V_{C_o}} \quad (2)$$

The value of another important variable which needs to be determined is the resonant inductor current i_{Lr}. It can be shown that i_{Lr} is an intermediate variable rather than an independent state variable. Based on Fig. 3, the expressions of the piece-wise linear waveform of i_{Lr} from t_0 to t_3 can be written as:

$$i_{L_r} = \begin{cases} I_{L_f} + \frac{V_{in}-V_{C_o}}{2(L_r+L_f)}(d-\Delta d)T_s - \frac{V_{clamp}}{L_r}t, & t \in [t_0, t_1] \\ I_{L_f} - \frac{V_{in}-V_{C_o}}{2(L_r+L_f)}(d-\Delta d)T_s + \frac{V_{in}}{L_r}(t-(1-d+\Delta d)T_s), & t \in [t_1, t_2] \\ i_{L_f}, & t \in [t_2, t_3] \end{cases} \quad (3)$$

Consequently, there are only three independent states: V_{clamp}, I_{Lf} and V_{Co} in the model. The next step is to write the state-space equations in terms of the state variables in different time intervals.

It can be seen from Fig. 3 that V_{clamp} only interacts with i_{Lr} during interval [t_0, t_1], while is kept unchanged for the other two intervals. The state-space equations of V_{clamp} can be written as:

$$\frac{dV_{clamp}}{dt} = \begin{cases} \frac{1}{C_{clamp}} I_{L_r[t_0,t_1]}, & t \in [t_0, t_1] \\ 0, & t \in [t_1, t_2] \\ 0, & t \in [t_2, t_3] \end{cases} \quad (4)$$

where $I_{Lr[t0,t1]}$ is the average value of the resonant inductor current in interval [t_0, t_1]. This value can be calculated as:

$$I_{L_r[t_0,t_1]} = I_{L_f} + \frac{V_{in}-V_{C_o}}{2(L_r+L_f)}(d-\Delta d)T_s - \frac{V_{clamp}}{2L_r}(1-d)T_s \quad (5)$$

In intervals [t_0, t_1] and [t_1, t_2] L_f is being discharged by V_{Co}. In interval [t_2, t_3] L_f together with L_r are charged by V_{in} - V_{Co}. Thus the state-space equations for I_{Lf} can be written as following:

$$\frac{dI_{L_f}}{dt} = \begin{cases} -\frac{V_{C_o}}{L_f}, & t \in [t_0, t_1] \\ -\frac{V_{C_o}}{L_f}, & t \in [t_1, t_2] \\ \frac{V_{in}-V_{C_o}}{L_f+L_r}, & t \in [t_2, t_3] \end{cases} \quad (6)$$

Since the output filter capacitor C_o can be always considered as being charged by I_{Lf} and discharged by the load resistor, its state-space equation can be written for all of the three intervals:

$$\frac{dV_{C_o}}{dt} = \frac{1}{C_o}\left(I_{L_f} - \frac{V_{C_o}}{R}\right), \ t \in [t_0, t_3] \quad (7)$$

The final step is to apply the state-space averaging on the derivation equations (3) – (7) to get the combined state-space equations for the entire switching cycle. The final equations are:

$$\frac{dV_{clamp}}{dt} = \frac{1}{C_{clamp}}\left[I_{L_f} + \frac{V_{in}-V_{C_o}}{2(L_r+L_f)}(d-\Delta d)T_s - \frac{V_{clamp}}{2L_r}(1-d)T_s\right](1-d) \quad (8)$$

$$\frac{dI_{L_f}}{dt} = -\frac{V_{C_o}}{L_f}(1-d+\Delta d) + \frac{V_{in}-V_{C_o}}{L_r+L_f}(d-\Delta d) \quad (9)$$

$$\frac{dV_{C_o}}{dt} = \frac{1}{C_o}\left(I_{L_f} - \frac{V_{C_o}}{R}\right) \quad (10)$$

where Δd can be expressed as (2). The equations (8) – (9) are the large signal average model of the active clamp buck converter.

IV. Model Validation through Simulation

A. Large-signal model simulation and verification

In order to verify the accuracy of the derived analytical model, simulations are conducted in PLECS based on the model equations as well as the detailed switching model of the converter. Fig. 4 shows the comparison of the simulation results where a step change from 0.7 to 0.8 is applied to the duty cycle. It could be seen the results generated by the derived model equations match very well with the switching model results.

B. Small-signal modeling and verification

Based on the large-signal average model of the converter, the small-signal transfer function from control-to-output (d to V_{Co}) can be obtained. Fig. 5 shows the bode diagrams of the control-to-output transfer function from Simplis simulation and the derived small-signal model. The simulation and model parameters are given in Table I. It could be seen that the magnitude plot from the model matches Simplis simulation result very well up to half of the switching frequency. The phase plot also matches well with Simplis simulation result with a maximum phase error less than 15° which happens at half of the switching frequency.

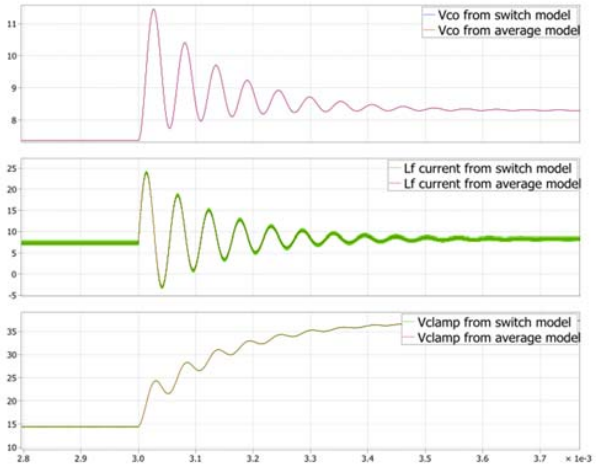

Fig. 4. Simulation Results with Average Model and Switch Model.

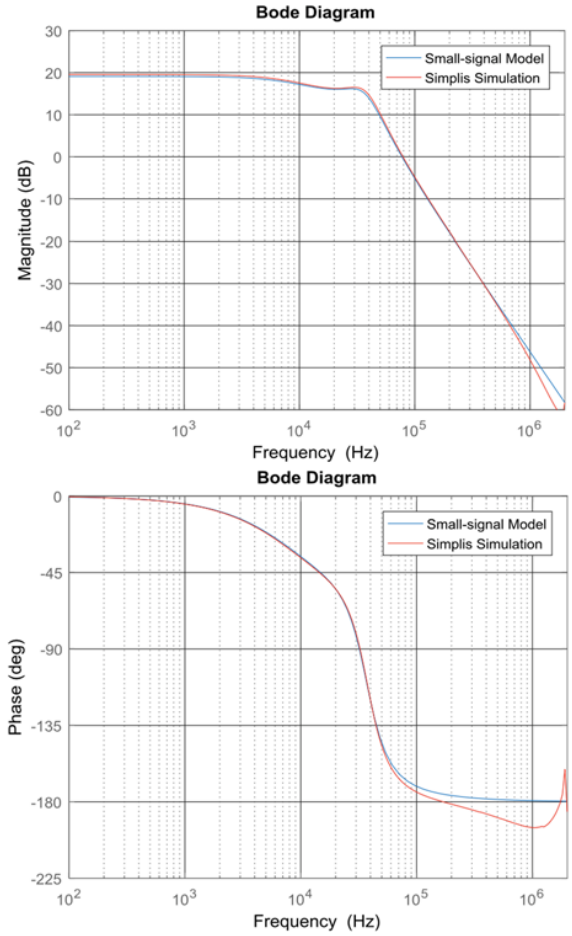

Fig. 5. Bode diagrams of control-to-output transfer function from Simplis simulation and the derived small-signal model.

TABLE I. SIMULATION AND MODEL PARAMETERS

V_{in}	12 V	Lf	1.3 uH	I_o	5 A	C_o	60 uF
V_{out}	5 V	C_{clamp}	3 uF	L_r	80 nH	f_s	2.2 MHz

The bode plot shows that the control-to-output transfer function of the active-clamp buck converter has a damped resonant peak in the frequency spectrum. Compared with the traditional buck converter, an additional pair of pole and zero is included in the transfer function. The phase change around resonant peak is not as steep as that in the conventional buck converter. In addition, the value of the clamp capacitor significantly affects the damping effect.

V. DYNAMICS INVESTIGATOIN OF THE ACTIVE CLAMP BUCK CONVERTER

From the converter operating principle, it is required that C_{clamp} to be an adequate large value, so that the voltage across the C_{clamp} is pretty stable during the operation. Based on the previous modeling analysis, it is clear that the value of C_{clamp} affect the dynamic characteristics of the active clamp-buck converter. It is required to investigate if we can use very large C_{clamp} value from the dynamic performance perspective. Fig. 6 shows the body diagram of the active-clamp buck converter with three different C_{clamp} values: 0.5 uF, 3 uF and 10 uF. The other parameters for generating Fig. 6 are shown in Table I. Fig. 6 indicates that large C_{clamp} will result in a resonant peak in the bode diagram, while smaller value of C_{clamp} will have a damping effect and eliminate the resonant peak. This damping effect is significant when C_{clamp} is small enough, such as 0.5 uF in Fig. 6.

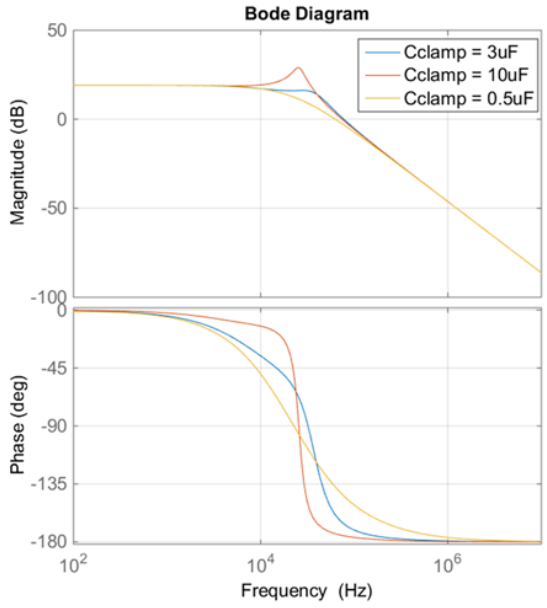

Fig. 6. Bode diagrams of control-to-output transfer function with three difference clamp capacitor values.

The existence of the resonant peak will complicate the compensator design of the converter and eventually affect the transient performance. For the scenario where a relatively small C_{clamp} value is used, a simple PI controller could be used to compensate the converter. While for the scenario where the C_{clamp} is large, with a simple PI controller, large ringing or unstable response could be observed due to small phase margin or negative gain margin. A comparison of the output voltage transient response is shown in Fig. 7 and it is clear that very large C_{clamp} is not helpful for the transient performance.

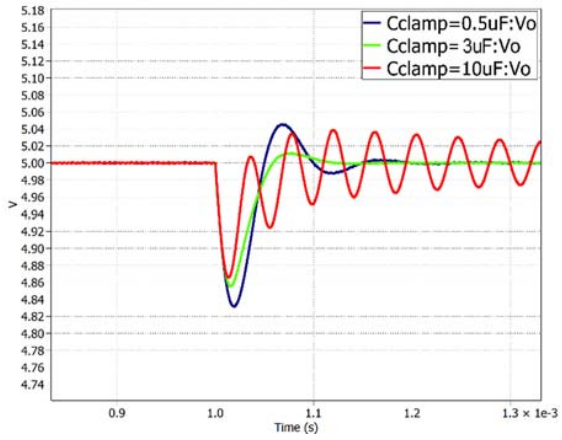

Fig. 7. A comparison of output voltage transient response with three different clamp capacitor values.

Therefore, the guideline when selecting the value of the clamp capacitor is to choose large enough capacitance for steady state operation while small enough capacitance for better dynamics performance. The model derived in this paper could be used to determine how small the clamp capacitance should be, and be used to assist the compensator design of the converter.

VI. Conclusion

In this paper, an accurate averaged model of an active-clamp buck converter is derived. The operating principle of the active-clamp buck converter is briefly reviewed. For the modeling, the large ripple of the resonant inductor current is dealt with the averaging over a specific time interval. Then, the large and small signal models are derived and verified with PLECS and Simplis simulations, respectively. It shows excellent match between the analytical model and simulation results. Last, the study of the active-clamp buck converter dynamics shows the impact of the dynamics by the clamp capacitor value. The guideline for choosing the proper clamp capacitor values is provided.

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