60 V-to-35 kV Input-Parallel Output-Series DC-DC Converter Using Multi-Level Class-DE Rectifiers

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***Abstract*—This paper presents a high-voltage dc-dc converter that includes inductively-isolated rectifiers. Previous work on multi-stage class-DE rectifiers only included capacitive dc isolation, limiting the output voltage to twice of the capacitor voltage rating. By adding an air-core transformer before the rectifier for inductive isolation, the maximum output voltage can be twice the breakdown voltage of the insulation between the transformer's primary and secondary windings, thus allowing the implementation of a small, lightweight, and fast transient high-voltage dc-dc converter. We experimentally demonstrate a multi-modular converter design with 60 V input voltage and 35 kV output voltage with 73 % efficiency.**

I. Introduction

High dc voltage in the range of tens of kV or higher plays an important role in X-ray sources and neutron generators [1] for airport security, ordinance and explosive detection, and medical applications such as dental X-rays or CT scanners. In order to enhance the portability of these devices without compromising their performance, a small, lightweight, and high-wattage power supply is often required.

The Cockroft-Walton multiplier is a well-known topology for high voltage generation that contains many voltage multiplication stages connected in series. Despite the advantage that voltage stresses on each diodes and capacitors are kept relatively low, the output voltage ripple as well as the output impedance increases rapidly with the number of stages [2]. For that reason, when the size and weight of the system should be kept low, Cockroft-Walton multipliers are restricted to low power applications.

A multi-stage class-DE rectifier [3] can address some of the aforementioned problems because it allows connecting all the input ports of rectifiers in parallel and output ports in series, thereby delivering current from the input to every node simultaneously. However, the maximum number of rectifier stages that can be cascaded is limited by the voltage rating of the dc-blocking capacitor at the top and bottom stages, and therefore the output voltage of the converter cannot exceed twice the voltage rating of the capacitor.

This paper presents a multi-stage class-DE rectifier with inductive isolation that breaks the limit set by the capacitor voltage rating. The insertion of an air-core transformer enhances the dc voltage blocking capability to the breakdown voltage of the material between transformer windings. Moreover, parallel connection of the stages enable fast rise time, making the circuit particularly suitable for systems that require pulsed dc voltage [4], [5]. In this paper, we demonstrate a proof-of-concept 1.25 MHz 6.08 kV 36 W rectifier with inductive isolation, and an input-parallel and output-series multi-level dc-dc converter with 60 V input voltage, 35 kV output voltage, and 204 W output power with the efficiency of 73 %.

∗ Sanghyeon Park and Lei Gu made an equal contribution to this work.

II. Circuit Description

The 300 V class-DE resonant rectifier [6]–[11] with capacitive dc isolation in Fig. 1a [3] is the basic building block for the high voltage generator. Since the rectifier diodes and output terminals are dc-isolated from the input, we can stack 20 units of a 300 V rectifier in series, as shown in Fig. 1b, to create a 6 kV voltage output.

In this configuration, the output voltage V_{out} can be up to twice the voltage rating of dc-isolation capacitors C_{Bt} and C_{Bb}. The reason is that the voltage stress on capacitors of top and bottom rectifiers is half of the total output voltage, provided that the isolated total output voltage diverges symmetrically toward positive and negative directions. In general, when the number of cascaded class-DE rectifiers is N and dc blocking capacitances are much larger than the diode junction capacitances, the voltage stress on n-th stage capacitors are expressed as follows:

$$\text{Voltage stress on } C_{Bt,n} = \left|\frac{n-1}{N} - \frac{1}{2} + \frac{1}{2N}\right| V_{out} \quad \text{where } n = 1, 2, \ldots, N$$

$$\text{Voltage stress on } C_{Bb,n} = \left|\frac{n-1}{N} - \frac{1}{2}\right| V_{out} \quad \text{where } n = 1, 2, \ldots, N+1.$$

In Fig. 1b, dc blocking capacitors of the top and bottom stages are withstanding $+3$ kV and -3 kV, respectively. If

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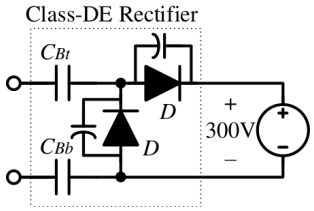

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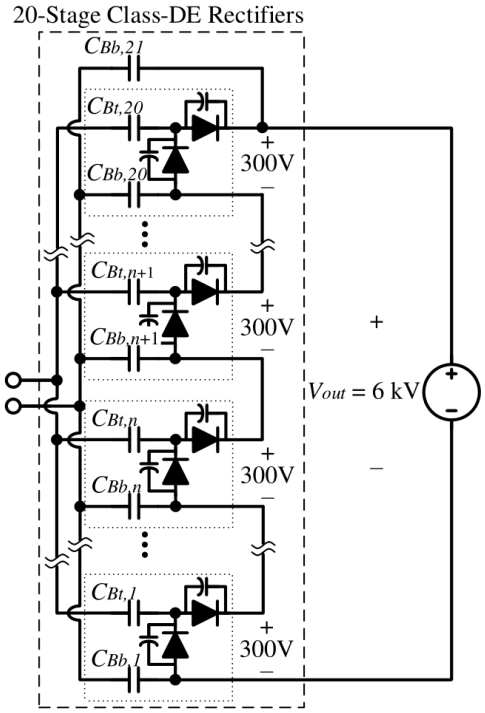

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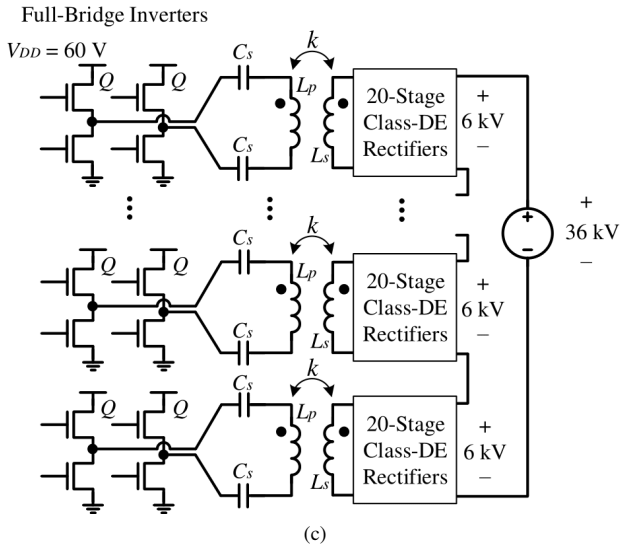
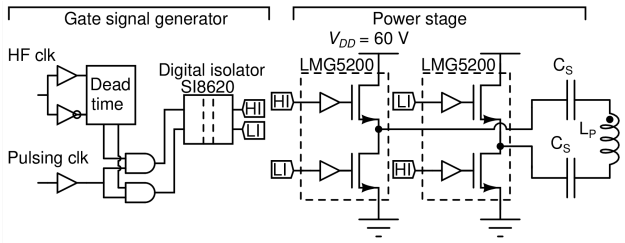


(c)

Fig. 1. The structure of the 60 V-to-36 kV dc-dc converter. (a) A 300 V single-stage class-DE resonant rectifier with capacitive isolation. (b) A 20-stage class-DE rectifiers with 6 kV output. (c) A 6-level dc-dc converter with 36 kV output driven by parallel-connected full-bridge inverters.



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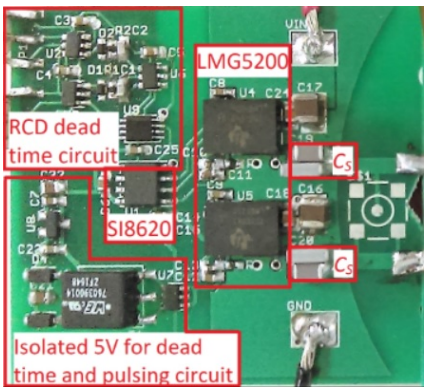


(b)

Fig. 2. Full bridge inverter circuit implemented. (a) The schematic of the full bridge inverter with timing circuit. (b) Photograph of the inverter circuit.

we assume that all capacitors are rated at 5 kV, no matter how many rectifier stages we connect, the total output voltage of this multi-stage rectifier cannot exceed 10 kV without operating capacitors of top and bottom rectifiers under a voltage stress of 5 kV or larger.

In order to achieve a higher output voltage, we introduce an air-core transformer which acts as an additional dc isolation barrier. As shown in Fig. 1c, we can cascade multiple units of the multi-stage class-DE rectifiers in series. Using this configuration, we can generate a high output voltage because the limit of the achievable voltage is now the breakdown voltage of the inductive isolation barrier between the transformer's primary and secondary windings.

III. Implementation

A. Inverter

Fig. 2 shows the inverter circuit which converts the dc input to a high frequency ac voltage. Fig. 2a and Fig. 2b show the schematic and photograph of the inverter, respectively. A full bridge resonant inverter is implemented here for the dc-ac stage. As the dc input V_{DD} is 60 V, we used two 80 V half-bridge circuits to form the full bridge. Each half bridge is implemented using a GaN power stage with an integrated gate driver. To maintain symmetry, the resonant capacitance are implemented with two capacitance in series as shown in Fig. 2a. Based on the PCB planner transformer parameters shown in Fig 3f, the series leakage inductance on the primary side is 1.7 μH. To design the series resonant frequency to

TABLE I. PART NUMBERS OF THE COMPONENTS USED FOR THE INVERTER IMPLEMENTATION. COMPONENT NAMES ARE IN REFERENCE TO FIG. 2A.

Name	Description	Part Number
Half bridge	80 V 10 A GaN	LMG5200
C_s	22 nF C0G cap	C3225NP02W223J230AA
	8.2 nF C0G cap	C4532C0G2J822J160KA
Digital isolator	2-CH 3.75kV 150Mbps	SI8620BC-B-IS
Isolated 5V	Push-pull transformer driver	SN6505B
Logic gates	Texas Inst. LVC series	SN74LVCxxx

TABLE II. GEOMETRICAL PARAMETERS OF THE PLANAR PCB TRANSFORMER LAYOUT.

	Parameter	Value
Primary winding L_p	Outer diameter	37 mm
	Inner diameter	30 mm
	Spacing between traces	18 mil (457 μm)
	Trace width	6 mil (152 μm)
	Turn number	12 turns
Secondary winding L_s	Outer diameter	37 mm
	Inner diameter	30 mm
	Spacing between traces	6 mil (152 μm)
	Trace width	6 mil (152 μm)
	Turn number	48 turns (24 turns on both top and bottom layers)

be 1 MHz, the series resonance capacitance needed is 15 nF. Therefore, each of C_s should be 30 nF. For each C_s, a 22 nF ceramic capacitor and a 8.2 nF ceramic capacitor are put in parallel and used here as shown in Fig. 2b. The low voltage input signals from the timing circuit are isolated from the GaN half-bridge modules using a digital isolator. An isolated 5 V is provided to the dead time and pulsing circuits using a push-pull transformer driver. The detail design of the isolated 5 V supply can be found in the manufacturer's datasheet of this part. Table I lists the part numbers of the components.

B. Transformer

Fig. 3 shows the planar PCB transformer design for the inductive isolation. Fig. 3a and Fig. 3b are PCB layouts of the primary winding on the inverter side and the secondary winding on the rectifier side, respectively. In both figures, the red area indicates the top copper, the blue area indicates the bottom copper, green circles indicate vias, and the white hatch mark indicates areas not covered by solder mask. Table II lists geometrical parameters of the transformer layout.

Fig. 3c shows the cross-sectional view of the transformer to illustrate the placement of 3 mil- (76.2 μm-) thick Kapton sheets each of which is rated at 4.5 kV/mil dielectric strength. We use four sheets of 3 mil (76.2 μm) Kapton sheets between two transformer windings to provide dc blocking capability of 54 kV. The first two Kapton sheets from the top cover the bottom side of the rectifier in order to prevent arcing between rectifiers when dc-dc converters are stacked. For a similar reason, two Kapton sheets at the bottom are bent over to cover the bottom side of the inverter to provide dc blocking between the inverter and the primary winding of the dc-dc converter underneath in the multi-level configuration. Two ounce copper- (71 micron-) is used for the trace implementation. In

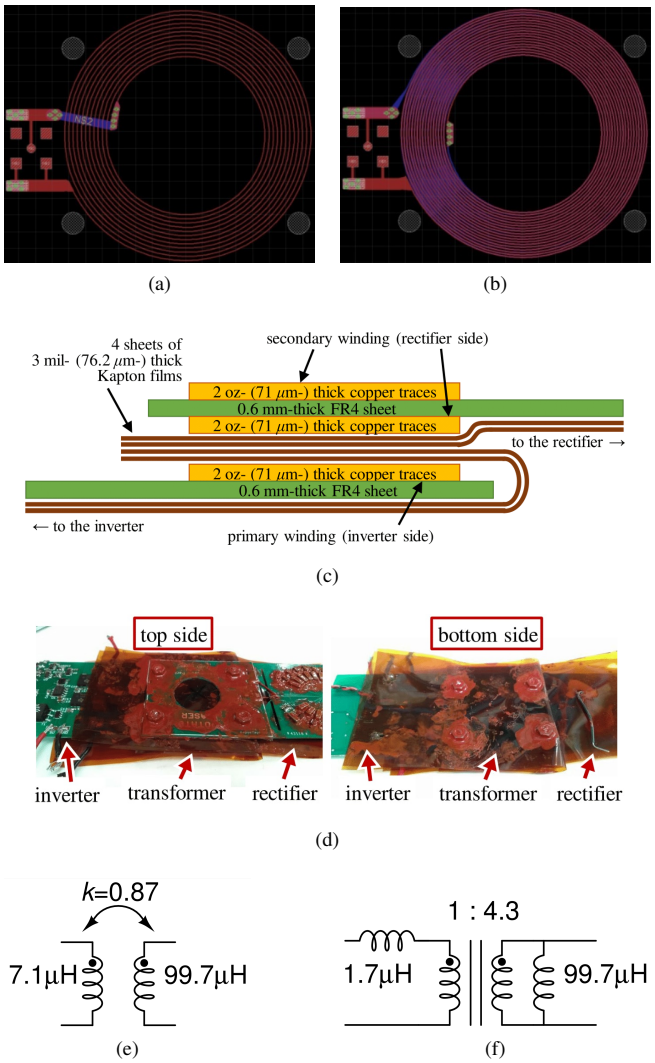
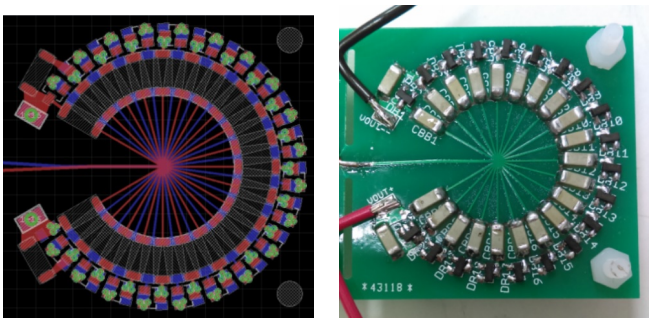


Fig. 3. Planar PCB transformer for inductive isolation. (a) PCB layout of the transformer primary winding (inverter side). (b) PCB layout of the secondary winding (rectifier side). (c) Cross-sectional view of the transformer illustrating Kapton sheet placements for high-voltage dc blocking. (d) Pictures of the implemented transformer, top and bottom sides. (e) Transformer coupled coil model. (f) Transformer leakage and magnetizing inductance model.

general, thicker copper is desirable because the ac resistance of the transformer winding at megahertz frequency is inversely proportional to the copper thickness. This is because of the current crowding toward the inner side of the copper trace at high frequency.

Fig. 3d shows the implemented transformer. We fasten circuit boards and Kapton sheets together by nylon screws and nuts. In order to prevent arcing through screw holes, the screw holes are filled with red-colored high voltage insulating coating shown in Fig. 3d. By following this design, we obtain a transformer with $L_p = 7.1$ μH, $L_s = 99.7$ μH, and $k = 0.87$, in reference to the schematic in Fig. 1c. Fig. 3e shows this coupled inductor model, and Fig. 3f shows the equivalent



(a) (b)

Fig. 4. The 20-stage cascaded class-DE rectifier for 6 kV dc output. (a) PCB layout of the rectifier. (b) Picture of the top side implementation.

TABLE III. PART NUMBERS OF THE COMPONENTS USED FOR THE RECTIFIER IMPLEMENTATION. COMPONENT NAMES ARE IN REFERENCE TO FIG. 1A.

Name	Description	Part Number	Manufacturer
C_{Bt}, C_{Bb}	33 pF X_1Y_2 C0G	885352010007	Wurth Electron.
D	240 V Si Schottky diodes	BAT 240A E6327	Infineon Tech.

leakage and magnetizing inductance model of the transformer.

C. Rectifier

Fig. 4 shows the 20-stage cascaded class-DE rectifier design and implementation. Fig. 4a is the PCB layout of the rectifier. Red, blue, green, and white hatched area indicate the same layers as described in subsection III-B for Fig. 3a and Fig. 3b. For blocking capacitors that correspond to C_{Bt} and C_{Bb} in Fig. 1a, we use 33 pF X_1Y_2-rated capacitor. For the diodes marked as D in Fig. 1a, we use two 240 V Si Schottky diodes connected in series as a single 480 V-rated rectifying device. Table III lists the part numbers of the components.

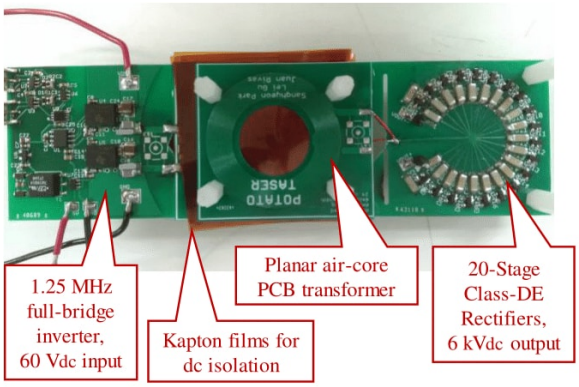


Fig. 5. The implemented 60 V-to-6 kV dc-dc converter. The size is 6 inches by 2 inches (15 cm by 5 cm).

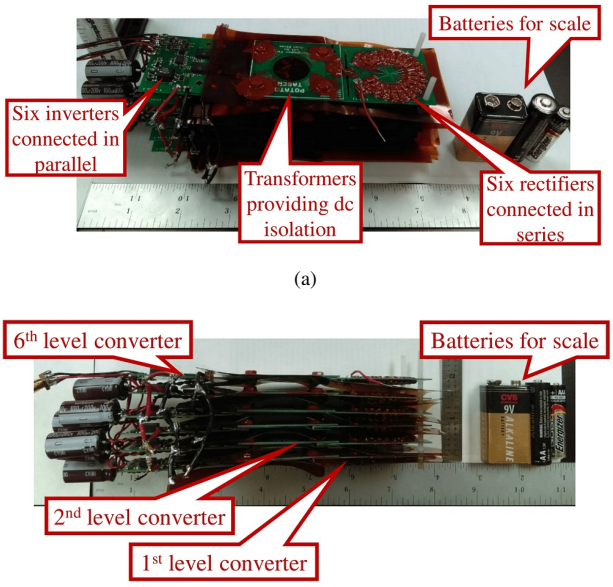


Fig. 6. The 60 V-to-35 kV dc-dc converter implemented by stacking six 60 V-to-6 kV dc-dc converters in Fig. 5. (a) The picture with an inch ruler at the bottom and batteris on the right for scale. (b) The lateral view that shows multiple levels of converters cascaded.

D. 60V-to-6kV, 24kV, 30kV, and 35kV dc-dc converter, single-level and multi-level cascaded

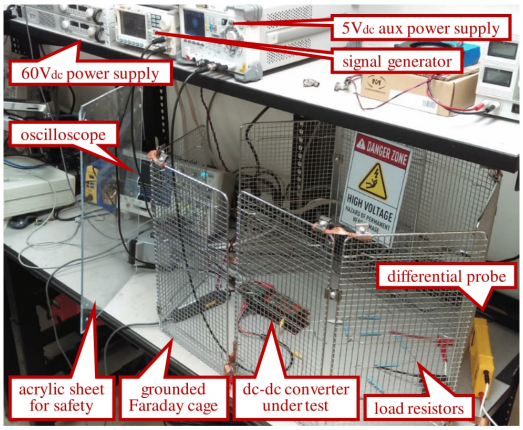
We combine the 60 V-to-RF inverter, the transformer, and the RF-to-6 kV rectifier previously described to make a 60 V-to-6 kV dc-dc converter shown in Fig. 5. The figure shows the transformer before the red insulating varnish is applied to screw holes.

Fig. 6 shows multiple 60 V-to-6 kV dc-dc converters stacked in a multi-level configuration. We stack from four levels up to six levels of dc-dc converters. Multiple units of 6 kV rectifiers are connected in series and 60 V inverters are connected in parallel. The dimension of the six-level converter is 8 inches $\times$ 2.5 inches $\times$ 2 inches (20 cm $\times$ 6 cm $\times$ 5 cm) in width, length, and height respectively as can be seen in Fig. 6a and the lateral view in Fig. 6b. The weight of the converter shown in Fig. 6 is 188 g.

IV. EXPERIMENTAL RESULTS

Fig. 7 shows the experimental setup. Since the experiment involves high voltage in the range of tens of kV, special care is taken to ensure that the experimenter is not exposed to any electrical or physical hazard. As shown in Fig. 7a, we surround the high-voltage converter and the load by a grounded Faraday cage that is shorted to a nearby water pipe. Also, we set up an acrylic sheet between the experimenter and the high-voltage converter to prevent possible injury from flying sparks or debris in case of (unlikely) catastrophic failure.

We use a differential probe (model number *CT4079*; manufactured by Elditest) that can measure a voltage up to $\pm$15 kV.



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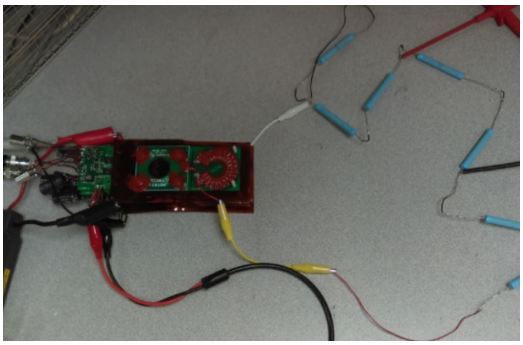


(b)

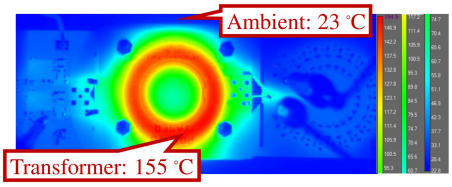
Fig. 7. Experimental setup. (a) Power supplies, probes and oscilloscopes connected to the high-voltage dc-dc converter under test. Also shown are the grounded Faraday cage and the acrylic sheet for safety. (b) Close-up picture of the converter under test.

Because of the limit in the probe's voltage rating, we measure the voltage of either one or two resistor units of the resistor chain as shown in Fig. 7b (each unit of the blue resistor is 1 MΩ). The measured voltage is scaled up by the voltage division ratio to estimate the end-to-end voltage applied to the resistor chain.

A. 60V-to-6kV dc-dc converter

Fig. 8 shows experimental results of the 60V-to-6kV dc-dc converter in Fig. 5. Although the converter peaks its output voltage at 0.9-1 MHz switching frequency range, we choose the switching frequency of 1.25 MHz in order to achieve the reasonably high output voltage and fast rise time simultaneously. Using 6.1 kV output voltage, we deliver 37 W power to 1 MΩ resistor for the load. Fig. 8a is the thermal image of the converter during continuous operation. The temperature of the planar PCB transformer increased slowly but steadily throughout the operation, and it reached 155 °C after 3 minutes of continuous operation at which point we turned off the converter to avoid damaging the transformer (we used an FR4 board with T_g rating of 130 °C).

Fig. 8b illustrates the output voltage waveform in a blue



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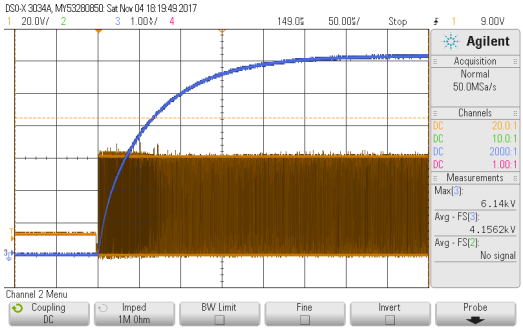

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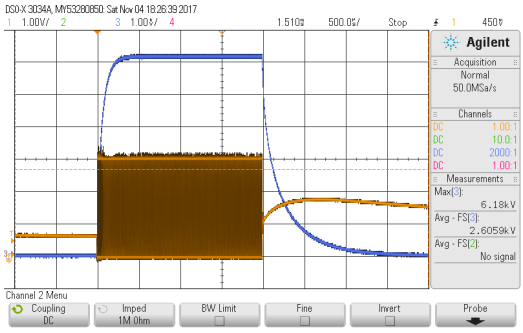


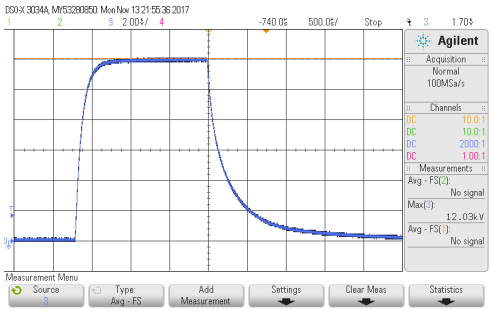
(c)

Fig. 8. Experimental results of the 60V-to-6kV dc-dc converter. (a) Thermal image after 3 minutes of continuous operation at 6 kV and 36 W output. (b) Waveforms of the output voltage (blue; horizontal scale 50 μs/div; vertical scale 1 kV/div) and the inverter half-bridge output (yellow curve) at the converter turn-on moment. (c) Zero-to-6 kV pulsed operation of the converter.

curve at the converter turn-on moment, from which the 10 %-to-90 % rise time is measured to be 135 μs. Fig. 8c shows a pulsed operation of the converter with the pulse width of approximately The output voltage in a steady state is 6.08 kV, and the dc-to-dc efficiency is 81 %.

B. 60 V-to-24 kV, 30 kV, and 35 kV dc-dc converter in a multi-level configuration

We vary the number of stacked dc-dc converter units from 4 to 6 and measure the performance of each configuration. Fig. 9 shows output voltage waveforms of 4-level, 5-level, and 6-level cascaded converters, from which the output voltages at the steady state are measured to be 23.9 kV, 30.4 kV, and 35.0 kV. Fig. 10 shows the performance variation of dc-dc converters at different numbers of 6 kV units cascaded. The efficiency tend to decrease with the number of stacked units, from 82 % in a single 6 kV unit down to 73 % in the 6-level configuration.



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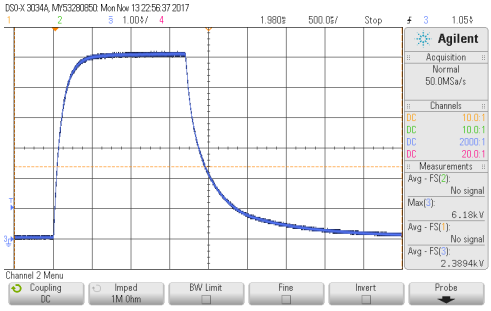

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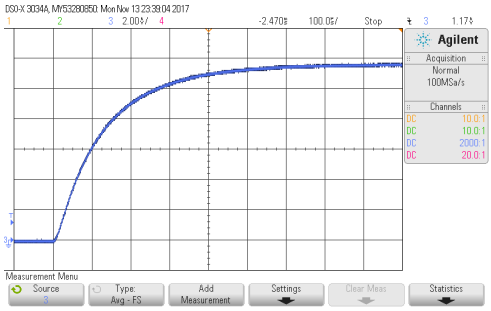

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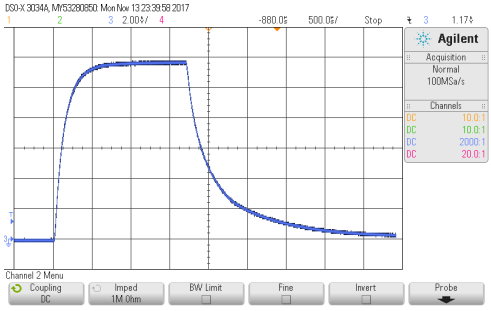
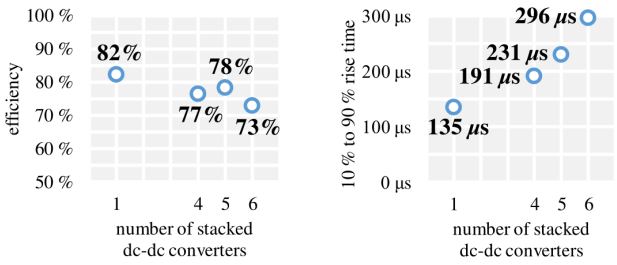


(d)

Fig. 9. Output voltage waveforms of the 4-level, 5-level, and 6-level dc-dc converters. (a) Pulsed operation of the 4-level 60 V-to-24 kV dc-dc converter. The horizontal scale is 500 μs/div and the vertical scale is 4 kV/div (the voltage is scaled down by 2:1 on the screen). (b) Pulsed operation of the 5-level 60 V-to-30 kV dc-dc converter. The horizontal scale is 500 μs/div and the vertical scale is 5 kV/div (the voltage is scaled down by 5:1 on the screen). (c) Turn-on moment of the 6-level 60 V-to-35 kV dc-dc converter. The horizontal scale is 100 μs/div and the vertical scale is 6 kV/div (the voltage is scaled down by 3:1 on the screen). (d) Pulsed operation of the 6-level 60 V-to-35 kV dc-dc converter. Horizontal and vertical scales are the same as those in Fig. 9c.



(a) (b)

Fig. 10. Performance variation of dc-dc converters at different numbers of 6 kV units stacked. (a) The efficiency. (b) The 10 %-to-90 % rise time.

One of possible reasons of this efficiency drop could be the close stacking of these multiple transformers causes the high frequency current distribution in the transformer winding to be different from the single stage case, and this increases the conduction losses in the planner PCB transformer. The rise time of the converter tend to increase with the number of stacked units, from 135 μs in a single unit to 296 μs in the 6 units cascaded. This increase is mainly attributed to the stray capacitance between the transformer primary and the secondary windings which needs to be charged up to half the voltage of the dc-dc converter output at the turn-on.

V. Conclusion

This paper presented a multi-level class-DE rectifier structure with inductive isolation. A high frequency operation allows fast transient response in the output voltage. The input-parallel output-series architecture using the air-core PCB transformer with high dc voltage blocking capability leads to high achievable output voltage of the dc-dc converter. We demonstrated a 60 V-to-6 kV dc-dc converter at 1.25 MHz switching frequency capable of delivering 36 W of power to the load and a high-gain dc-dc converter in a multi-level configuration that can deliver 35 kV voltage and 203 W power to the load while maintaining 73 % efficiency and can pulse the output at 296 μs rise time.

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