A Self-Bias Supply Scheme for the Control Circuit in Power Converter

Lijuan Shen
College of Electronic Engineering
Zhejiang University, Hangzhou, Zhejiang 310027, China
Email: shenlijuan@zju.edu.cn

Junming Zhang
College of Electronic Engineering
Zhejiang University, Hangzhou, Zhejiang 310027, China
Email: zhangjm@zju.edu.cn

Junjun Zhang
a) College of Information Science and Technology
Fudan University, Shanghai, 200433, China
b) State Key Laboratory of Operation and Control of Renewable Energy & Storage, China electric power research institute, Nanjing, 210003, China
Email: zhangjunjun@epri.sgcc.com.cn

Shuai Shao
College of Electronic Engineering
Zhejiang University, Hangzhou, Zhejiang 310027, China
Email: shaos@zju.edu.cn

***Abstract*—This paper proposes a novel self-bias supply scheme for the control circuit in dc-dc converters to improve the efficiency. Compared with existing methods such as auxiliary winding, linear voltage regulator, the proposed method can achieve better efficiency and more stable voltage for the control circuit. An auxiliary switch paralleled with the main switch is used to get the bias voltage for control circuit. This auxiliary switch works in an intermittent mode which can reduce the switching losses. The proposed method is validated on a 64-W flyback converter prototype.**

Keywords—self-bias; flyback

I. INTRODUCTION

The control circuit is one of the most important circuit for stable and reliable operation of a power converters, which is usually an integrated circuit (IC) controller with few external components for low power applications. The bias power for the control circuit is an interesting topic. There are mainly two conventional methods to feed the power into IC controllers. One is using another independent bias supply such as the linear regulator or a small switching DC-DC converter [1-3]. This straightforward method, though relative simple in control suffers low efficiency and high cost [4, 5]. The other employs an auxiliary winding to obtain energy for control circuits [6]. This one has higher efficiency, but the additional auxiliary winding means a more complex manufacturing process [7, 8] Even if adopting PCB winding based transformer, extra copper for winding increases cost. Moreover, the control circuit supply voltage may be affected by both the output voltage and load of the circuit, since a transformer has leakage inductance and thus the auxiliary winding and the secondary winding cannot be fully coupled [9, 10]. Therefore, there involves a challenging issue to feed the control circuit in an easy and high-efficient way.

Several revised self-bias supply schemes have been proposed to ease the concerns occurred in traditional methods. One method called Dynamic Self Supply (DSS) technique is already adopted by a few semiconductor companies [11]. For example, NCP1200 series developed by ON Semiconductor

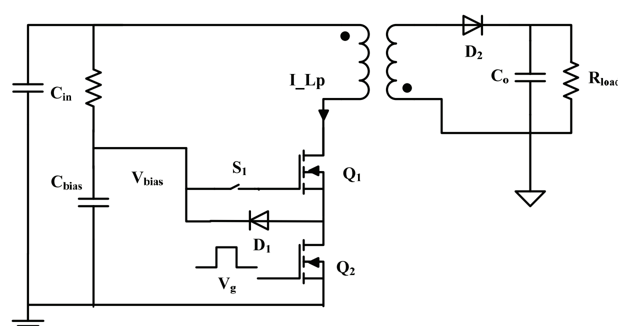

Fig.1 Source Drive Supply scheme

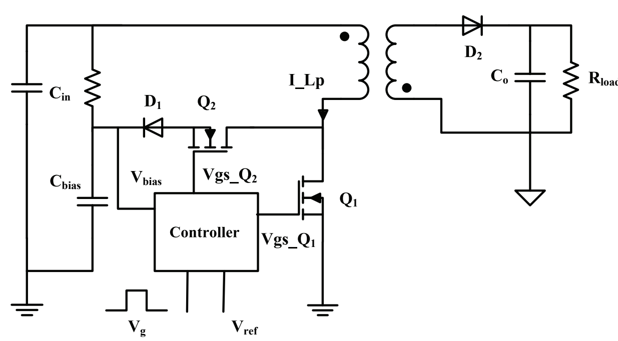

Fig.2 Paralleled Self-Bias Supply scheme

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and TinySwitchII series developed by Power Integration adopt DSS technique. DSS function is provided by the internal high-voltage current source. However, this technique is limited in low-power applications and the energy of self-bias supply which comes from the dc bus directly increases the input power. Alternatively, Source Drive Structure is a good way to improve the bias supply efficiency since the energy in inductors could be utilized to source the control circuit [12]. The topology is shown in Fig. 1. However, there are two extra switches needed, and the switching frequency of switch S_1 is twice higher than the main Switch Q_1. Therefore, this method increases the cost and the switching loss.

To overcome the previous problems in self-powered supply, a new scheme called Paralleled Self-Bias Supply (PSS) is proposed in this paper. This scheme provides reliable bias supply and maintains higher efficiency. Only one additional switch is needed compared to the Source Drive Structure. And the switching loss of the auxiliary switch is reduced by working at intermittent mode. The main circuit of the proposed method is presented in Fig. 2. As shown in Fig. 2, the switch Q_2 and diode D_1 are added into the conventional flyback topology

II. Analysis of the Proposed Self-Powered Scheme

The main feature of this scheme can be outlined as follows. Before the main switch Q_1 is turned on, the excitation current of the transformer directly charges the bias capacitor C_{bias} through the switch Q_2 without any other power dissipation. Q_2 works in an intermittent mode. If the voltage of C_{bias} is charged to the predefined upper threshold, Q_2 will be turned off for several cycles till the voltage of C_{bias} dropping to a minimum point. Then Q_2 will be turned on again to charge the C_{bias}. Q_2 works in an intermittent mode in a much lower frequency. Furthermore, the leakage energy in the transformer is reused to supply the control circut and hence the efficiency can be improved. Therefore, this method improves the overall efficiency effectively by employing one additional auxiliary switch without increasing its switching loss compared with the existed methods mentioned above.

The key working waveforms are shown in Fig. 3 and Fig. 4. And there are two operating modes.

During [T_0~T_{n1}] periods, as shown in Fig. 4(a), the bias voltage of C_{bias} rises (the waveform does not increase linearly, since when Q_2 is turned OFF, the voltage will decrease slightly). V_g is the driving PWM waveform generated by the control circut. When V_g is high, the excitation current rises, and this interval can be divided into two sub-intervals. In the first sub-interval [t_0~t_1], Q_2 is turned ON and Q_1 is turned OFF. The excitation current charges the C_{bias} via Q_2. As long as the energy from inductor is larger than the energy consumption of the control circut, the voltage of V_{bias} rises. It is noted that the length of this sub-interval needs to be carefully designed so that enough power will be ensured to supply the control circuit. The detailed procedure to set the length will be provided in next section. In the second sub-interval [t_1~t_2], Q_2 is turned OFF and Q_1 is turned ON. The excitation current flows via Q_1 and V_{bias} decreases.

During [T_{n1}~T_{n2}] periods, as shown in Fig. 4(b), Q_2 remains OFF and the driving waveform of Q_1 is the same as V_g shown in Fig. 4(b). During this interval, the circuit works exactly as the conventional flyback. Also, the V_{bias} will drop over time.

In each cycle of V_{bias}, the period of the intermission mode of the auxiliary switch depends on the time interval of the Q_2 ON time and the boundaries (V_H and V_L) of the voltage of C_{bias}.

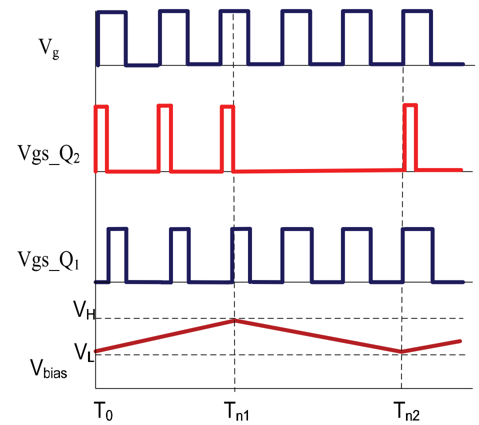

Fig. 3 The key waveforms of the proposed scheme

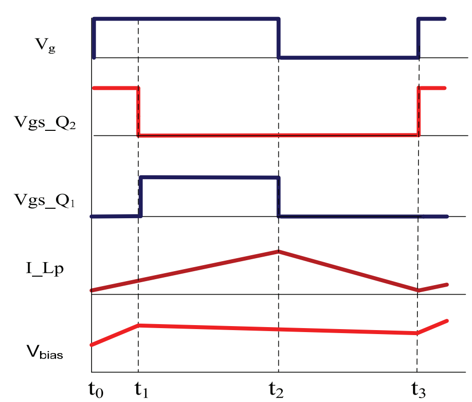

Fig. 4(a) The waveforms in [T_0~T_{n1}] periods

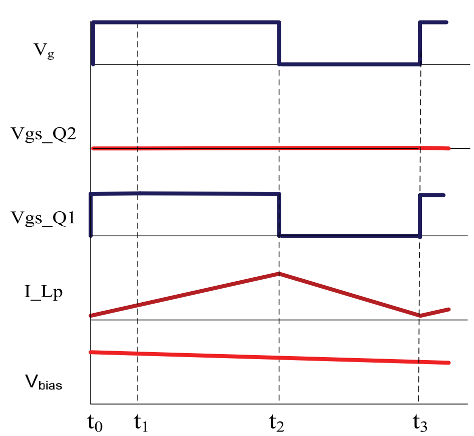

Fig. 4(b) The waveforms in [T_{n1}~T_{n2}] periods

III. Design of the Proposed Scheme

To achieve the function of intermittent working mode, the main logic circuit is designed as Fig. 5 shows. There are three input parameters V_{bias}, Vg and V_{ref}. V_{ref} is generated by control circuit and is set to 5V in latter experiment. The output parameters Vgs_Q1 and Vgs_Q2 are driving signals for Q_1 and Q_2. This logic circuit is consisted of three parts (comparator with Hysteresis, time delay circuit and logic gates).

The comparator with Hysteresis shown as F_1 is used to set the scope of the charging voltage of C_{bias}. If the supply for the comparator is V_{cc}. Then the thresholds V_H and V_L of V_{bias} are represented as following equations.

$$V_H = \frac{R_1}{R_1+R_2}V_{cc} + \frac{R_2}{R_1+R_2}V_{ref} \quad (1)$$

$$V_L = \frac{R_2}{R_1+R_2}V_{ref} \quad (2)$$

The delay circuit is a simple RC circuit shown as F_2. The charging current gradually charges C_1 via the resistance R_3. And through the diode D_1, C_1 can discharge quickly. The NOT gate serves as a Schmitt trigger. Only the voltage of C_1 is over the threshold of NOT gate (V_{th}), the output of the gate is changed. The schematic diagram is shown in Fig. 6.

The delay time $[t_0 \sim t_1]$ defined as t_d can be derived from the equation (3).

$$t_d = R_3 C_1 \times \ln\left(\frac{V_{o\_AND_2}}{V_{o\_AND_2} - V_{th}}\right) \quad (3)$$

In fact, the proposed self-bias supply scheme can be implemented using other logic circuit. However, the logic circuit in Fig. 5 has two advantages compared to other circuits. First, it contains minimum kinds of logic gates. Besides, every logic gate has its inherent time delay. To eliminate the influence of this inherent time delay, it is recommended that the two paths producing the driving signals for Q1 and Q2 have equal number of logic gates. There are four gates for each driving signal route in this design.

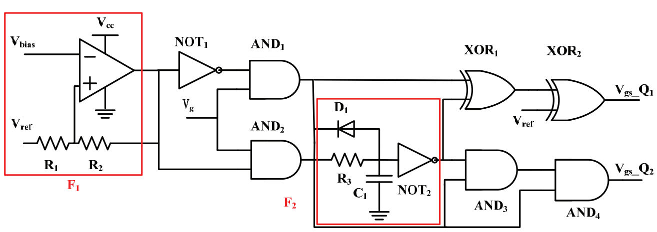

Fig. 5 main logic circuit for the proposed scheme

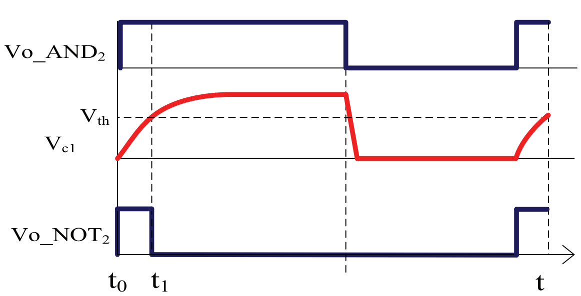

Fig. 6 The waveforms of time delay part

IV. Experimental Results

The proposed novel scheme is validated by experiment. The self-bias supply is adopted in a 64-W flyback converter. The system parameters are illustrated in Table. 1. Fig. 7~Fig. 8 show the experimental results, and Fig. 10 shows a photograph of the prototype.

TABLE 1: System Parameters

Parameter	Value
Input DC voltage	110~370V
Output voltage	19.5 V
Output current	3.3A
Excitation inductance	150uH
Transformer turns ratio	30: 5
Switching frequency	150kHz
IC controller	UC3843

Fig. 7 shows the voltage of V_{bias} ranges from 12V~15V as designed. The driving voltage of the Q_2 works in an intermittent mode.

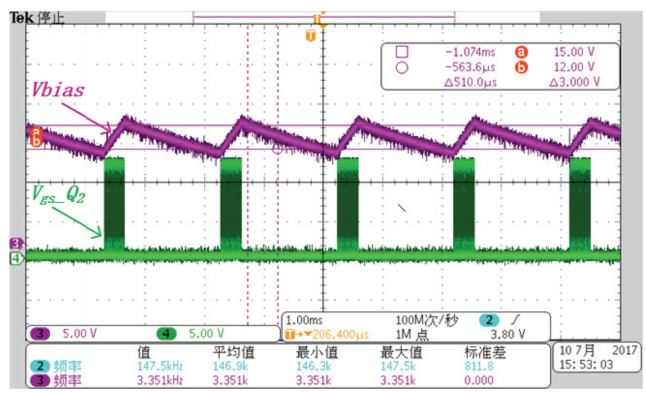

Fig. 7 The waveforms of V_{bias} and V_{gs}_Q_2

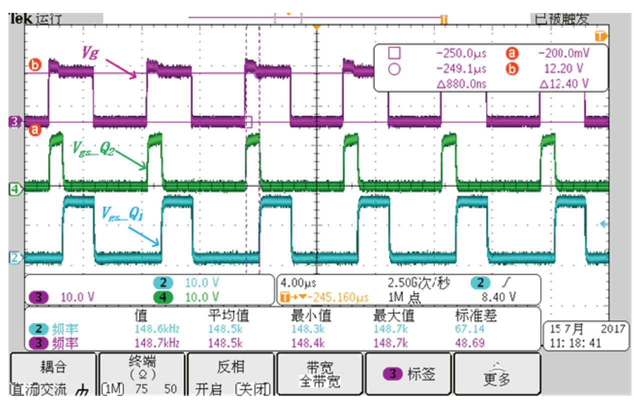

Fig. 8(a) V_g, V_{gs}_Q_2 and V_{gs}_Q_1 in charging periods

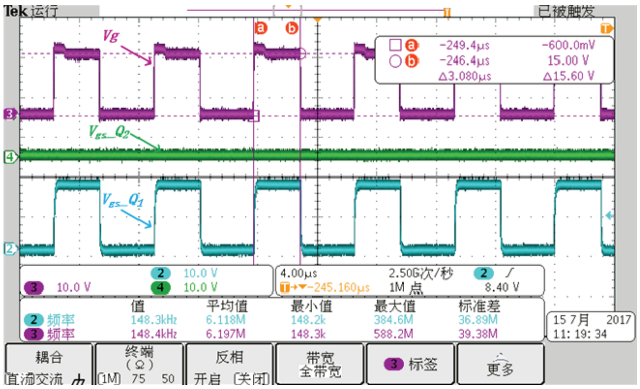

Fig. 8(b) V_g, V_{gs}_Q_2 and V_{gs}_Q_1 in discharging period

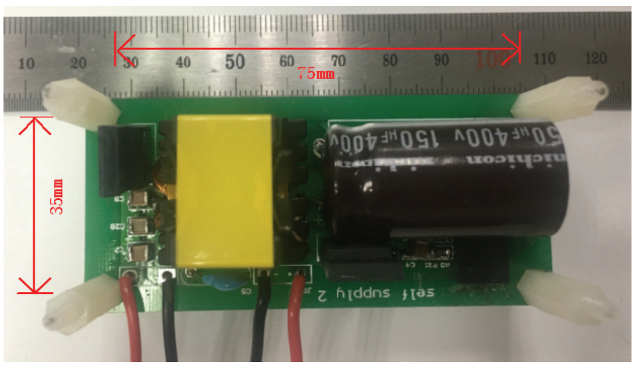

Fig. 10 Prototype of the flyback converter

Fig. 8 shows the driving signals of the Q_1 and the Q_2. When V_{bias} decreases to 12V. the waveforms of driving signals are shown in Fig. 8(a). V_{bias} starts to increase. When V_{bias} reaches 15V, the waveforms of driving signals are shown in Fig. 8(b). Then V_{bias} begins to decrease.

V. Conclusions

This paper has proposed a self-bias supply scheme called paralleled self-bias supply (PSS), which can provide more high-quality and high-efficiency power supply compared with conventional methods. This proposed circuit works in an intermittent mode to reduce the frequency of auxiliary switch and thus reduce the switching loss. The main principle of this new topology is realized by an additional switch, a diode and the logic circuit presented in section III.

The proposed method is implemented in a flyback converter. The feasibility of this scheme is verified by experimental results.

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