A SiC-Based Power Electronics Interface for Integrating a Battery Energy Storage into the Medium (13.8 kV) Distribution System

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***Abstract*—This paper describes the study of a topology of modular multilevel converters for integrating battery energy storage into a medium (13.8 kV) distribution system. The main benefit of this topology is to remove the need for a bulk 60 Hz transformer that is normally used to step up the output of a voltage source inverter to the medium voltage level. A SiC-based power electronics interface presented in this paper provides an efficient solution without the large and costly transformer. Using medium voltage SiC devices (⩾ 10 kV SiC MOSFETs), with their high breakdown voltage, enables the system to meet and withstand medium voltage application, using a minimized number of cascaded modules. This SiC-based power electronics interface significantly reduces the complexity usually faced when Si devices are used directly in medium voltage applications. The voltage and state of charge balancing control for battery modules is also simplified and performs well. The simulation and experimental results, performed on a low-voltage prototype, verify the proposed topology that is presented in this paper.**

Keywords*—*SiC-Based Power Electronics Interface, Battery Energy Storage, Medium Voltage Distribution System, Decoupled Current Control

I. INTRODUCTION

The utility-scale battery energy storage systems (BESS) can provide grid support and smooth the output of renewable energy systems. The advancement of battery material chemistry and the decrease in cost of semiconductor devices is fueling the research interest in developing the power electronics interface as an enabling technology for connecting utility-scale BESS to the medium-voltage grid. Many topologies have been proposed in the literature. Conventional grid-connected power electronics interfaces for BESS consist of a simple two-level converter with a 60 Hz bulk line frequency transformer. The transformer is used to boost the voltage from hundreds of volts to medium voltage levels. To avoid the losses and cost associated from line-frequency transformers, directly connected utility-scale BESS solutions have been developed, [4]. Transformerless topologies using a two-level converter or three-level neutral-point clamped converter can be achieved using a series connection of semiconductors.

The direct connection to the MV ac grid without the use of a line frequency transformer can be achieved through the use of modular multilevel converters. Modular multilevel converters (MMC) have become one of the most attractive topologies in power electronics applications regarding the medium voltage distribution system. There are several types of MMC, such as flying capacitor, neutral point clamped, and cascaded H-bridge (CHB) modular multilevel converters, etc. The CHB multilevel inverter is suitable for battery energy storage systems in the medium voltage distribution system applications [1]. The CHB multilevel inverter is the best candidate for directly connecting the battery energy storage system into the medium voltage ac grid, [2],[3],[4]. It integrates low-voltage battery strings into its modular structure and has a wide application range by scaling up to higher voltage ratings with the simple addition of modules. The modular structure also allows only a short string of batteries to be taken out of service in the case of a battery fault or overheating, thus increasing the reliability of a BESS. Another advantage of the CHB multilevel inverter topology is that it provides easy grid connection with low filtering requirements. As a result, it is a cost-effective and provides a higher energy efficiency comparing to other configurations reported in literature, [4].

Although the circuit structure of a modular multilevel converter is naturally modular, the control structure is highly centralized making it more complicated, [5]-[6]. It involves the communication of a large amount of information, and complex submodule management. For this reason, wide-bandgap devices are used in this paper to take advantage of higher voltage ratings, resulting in a greatly reduced number of submodules, thus lowering the total component count, and simplifying the control and management system. The major goal of utilizing medium voltage SiC MOSFETs in a CHB is to analyze the trade-offs between the control complexity, the converter reliability and the ac filter size, by taking advantage of the high-switching frequency and high break-down voltage of SiC devices. Two optimization targets of this study are (1) to significantly reduce the number of submodules for the multilevel inverter, and (2) to reduce the complexity of control algorithms with the capability of meeting the medium voltage requirements without the need of step-up 60 Hz transformer, as shown in the block diagram in Fig.1. The topology in [7]-[8] proposes the utilization of a single large dc-link battery, which does not benefit from the lower submodule voltage levels. In this paper, the modular multilevel CHB three-phase inverter is chosen to support a large dc-battery storage system and benefit from submodule battery voltage levels, Fig. 2. The PWM switching method such as phase shifted

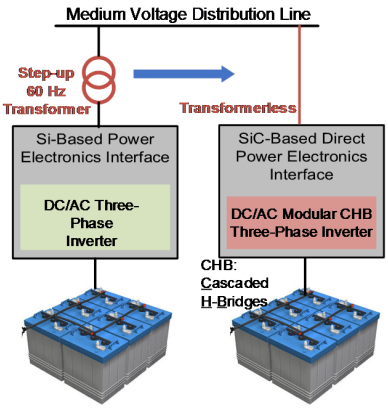

Fig. 1. Battery energy storage into a medium voltage ac grid

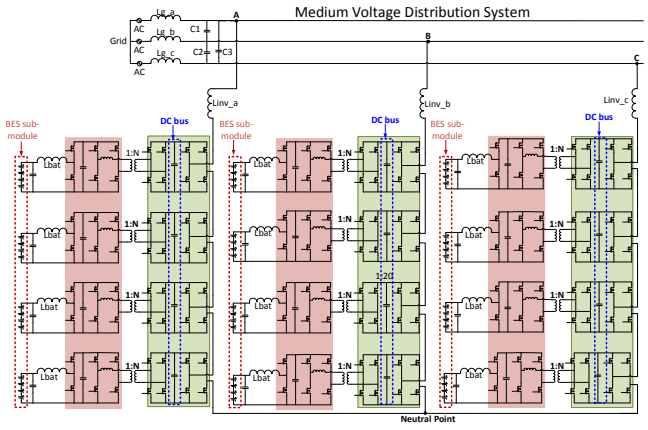

Fig. 2. Nine Level CHB, with high gain dc/dc converters integrated

PWM (PS-PWM) is used for CHB for symmetrically balancing the thermal behavior of switching devices.

II. TOPOLOGY DESCRIPTIONS

Recent advances in high-voltage power semiconductor devices based on silicon carbide (SiC), a wide-bandgap (WBG) material, are paving the way to the realization of a direct interface for battery energy systems into the medium voltage distribution grid. Modular multilevel converters, currently Si based, have been reported in literature, but they present a high level of complexity due to the limitation in the voltage rating of available Si power devices. The goal of this topology is to realize a SiC-based interface without the complexity required by silicon power semiconductor devices. A three phase CHB multilevel inverter is shown in Fig. 2. Each CHB cell consists of a dc voltage, E, and four switches. The dc bus voltage, E, is regulated by a dc/dc gain converter, such as shown in Fig. 2, Fig. 4, and Fig. 5. The nine level cascade multilevel inverter produces nine level output: which are: 4E, 3E, 2E, E, 0, - E, -2E, -3E and -4E. The number of the CHB cells is N .The output voltage of each CHB cell is v_{H1} to v_{Hn}, from cell1 to cell N. The output voltage of a single phase CHB multilevel inverter (V_{AN}) is the sum of v_{H1} to v_{Hn}, Fig. 5. To avoid using a kV battery bank for the dc bus, a high-gain dc/dc converter is used to boost the low voltage battery bank to kV dc voltage level that is needed for each cell in medium voltage application, such as a13.8 kV distribution system.

A. Voltage Scalability to kV Level

For the topology to produce the correct medium voltage output, a high dc bus voltage (in kV range) for each module is needed. To meet a kV dc bus, it would require connecting many batteries in series [7]-[9]. If this method of connecting many batteries in series is considered, the system will be inefficient, unreliable, and very expensive, due to the inaccurate state of charge (SOC) balancing when a high voltage battery bank is used, [6]. To solve this problem, the proposed SiC-based power electronics interface for integrating battery energy storage into the medium (13.8 kV) distribution system, does not only use the dc to ac H-bridge inverter, it also uses dc/dc converter to minimize the voltage requirement for battery bank and SOC balancing control for each cell. When a high gain dc/dc converter is not used, the battery bank for each module is in kV-level. On the other hand, using a high gain dc/dc converter provides the advantage of rating the battery bank for each module in low-voltage, V-level, resulting in a more cost effective battery bank. The most important unit in the dc/dc stage is the high frequency transformer (HF-XFMR) to provide a high step-up gain, [10]. The system topology is chosen to ensure lower current ratings for HF-XFMR, which minimizes the cost. The magnetic materials for each HF-XFMR would be very expensive, especially for MW power level, if each battery bank is selected with high current ratings. To ensure lower current rating for HF-XFMR, two or three dc/dc converters are operated in parallel, and to balance the dc bus for each cell, the dc-droop control is used.

B. Power Scalability to MW Level

For voltage scalability, the dc/dc converter stage is applied to reduce the required battery voltage bank and meet the medium voltage level requirements. This method of using a low-voltage battery bank and boosting it to the kV level is suitable for low rated power application, but if the rated power is scaled to megawatts (MW), it would require high current ratings, resulting in low efficiency. To achieve higher efficiency, it requires both low voltage battery bank and low current ratings. To scale the system power rating to the MW level, interleaved or parallel connected dc/dc converters present the best solution for boosting the battery bank at low voltage with low current ratings, [10]-[11].

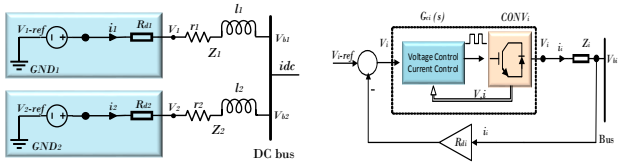

Fig. 3: Example of two parallel operation of dc/dc stage and the droop control for each converter (*CONVi*)

The modularity of the proposed interface for integrating the BESS into a medium voltage distribution system at any power rating provides better reliability advantages. In case there is a

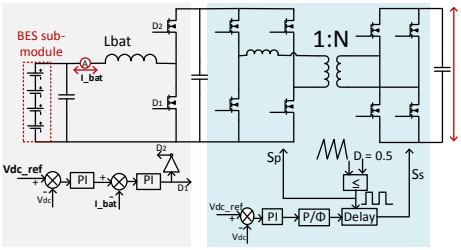

Fig. 4: Controls for dc/dc converter

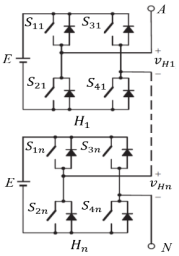

Fig. 5: *n* Level CHB, one phase

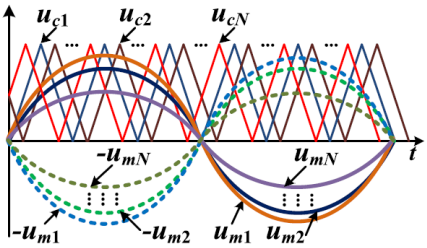

Fig. 6. Unipolar PS-PWM control for CHB converter

fault at any battery cell, the system continues to supply power with the healthy cells. The dc droop control algorithm is used for dc/dc parallel converters to prevent high amplitude currents being drawn from the batteries. Thus, the parallel operation of dc/dc converters, in Fig. 7, potentially preserves the battery life span, with reduced power losses in the battery packs.

An example of the droop control applied to two parallel converters V_1 and V_2 with initial reference voltages V_{1_ref} and V_{2_ref} connecting to the dc bus to send power to H-bridge cell1, Fig. 7 and Fig. 3. The terminal bus voltages are V_{b1} and V_{b2}. Typically, the initial reference voltages are equal as $V_{1\_ref} = V_{2\_ref}$. The steady-state relationship between the current sharing and the droop resistances is

$$\frac{i1}{i2} = \frac{Rd2+r2}{Rd1+r1} \qquad \text{(Eq. 1)}$$

Where i_1 and i_2 are the supplying currents, $r1$ and $r2$ are the equivalent line resistances from each dc/dc converter to the dc bus, and $Rd1$ and $Rd2$ are the droop resistances. The droop resistances are used to create a new set-point for the output voltage of each dc/dc converter to control the current sharing between battery banks of each cell. The droop control in Fig. 3 for one DC source is supposed to be carried out via one power converter ($CONVi$). The relationship between the voltage reference and the output voltage of each dc converter is expressed by the following equation: $V_i = (V_{iref} - R_{di}\, i_i)\, G_{Ci}(s)$, (Eq. 2), where the subscript (i) refers to the index of dc/dc converter in the system (i = 1, 2), V_{iref} is initial voltage references of each dc/dc converter, and G_{Ci} (s) is the transfer function. The interconnecting cable impedance is expressed as a series combination of resistance and inductance with the following relationship: $V_i - V_{bi} = r_i\, i_i + l_i\, (di_i/dt)$ (Eq. 3)

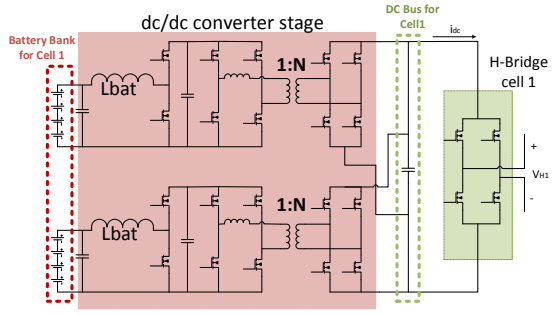

Fig. 7: Parallel operation of dc/dc converters for power scalability

C. *Number of Modules Needed to Meet the Medium Voltage Level*

To directly connect the battery energy storage to a 13.8 kV distribution system, using 10 kV SiC MOSFET, at least a 5-level CHB inverter is needed, with a dc bus that is approximately equal to 6.0 kV at each cell. To decide the number of cells and the dc bus voltage ratings, the calculation is done using the equation, Eq. 4, as in [12]. The calculation is completed considering hard switching, a 40% safety margin, and an amplitude modulation, ma ≈ 1. For reliability purposes, a nine-level CHB inverter is selected, as shown in Fig. 1, and Fig. 2. With this number of cells, four per phase, in case there is a fault, one cell or two cells are down in any phase-leg of three phase inverter, a balanced 13.8 kV rms, 3Φ output will still be generated. The dc/dc converter with a variable gain is used. The dual-active bridge (DAB) converter with a high frequency transformer which has a fixed turns-ratio, (1: N), in Fig. 2. A synchronous buck/boost converter is integrated with DAB converter both to control the current flowing in and out of the battery, and to provide a variable dc gain. For example, if four cells per phase are operating, the dc bus for each cell is regulated at 2.8 kV to 3.0 kV, for the inverter to generate a balanced 13.8 kV rms, 3Φ output. However, if there is a fault, and for example two cells are down, the gain is adjusted by the duty-cycle, (D1) as shown in Fig. 4, for the synchronous buck/boost converter to regulate the dc bus at 5.6 kV to 6.0 kV for the inverter to generate a balanced 13.8 kV rms, 3Φ output, $V_{AB(\max)}$ as expressed in the following equation.

$$[V_{AB(\max)} = 0.612\ (m-1)\ V\_dc] \qquad \text{(Eq. 4)}$$

Where $m = 2N+1$, and N= number of cells per phase

The DAB is controlled using phase shifted square wave modulation to manage the power flow between two dc sources, and active harmonic suppression strategy, [13]. For the cascaded H-bridge cells, the unipolar carrier phase shifted sinusoidal PWM is adopted, which is shown in Fig. 6. The signals $u_{c1}, u_{c2}, \ldots$, and u_{cN} are the triangle carrier waveforms for the H-bridges of cell 1, cell 2,…, and cell *N,* respectively. These carrier waveforms have the same shape but are phase-shifted by *Tc/N*, where *Tc* is the period of these carrier signals and *N* denotes the number of H-bridge cells. The signals $u_{m1}, u_{m2}, \ldots$, and u_{mN} are the modulation waveforms for the corresponding left legs of the H-bridge cells. These modulation waveforms share the same phase angle. While, the signals, $-u_{m1}, -u_{m2}\ldots$, and $-u_{mN}$ are the opposite values of the aforementioned modulation waveforms, respectively.

D. The Controls Applied at Each Stage (dc/dc Stage and dc/ac Stage)

Fig. 6 shows typical phase-shifted carrier waveforms and bridge-cell modulation references that are used to control CHB inverter. Fig. 11 and Fig.12 show the resultant bridge-cell output waveforms, staircase voltages with nine levels for four cells per phase. They are inverter output voltages before the filter, as Fig. 11 and Fig. 12 show. For dc-to-ac conversation, the three-phase CHB is controlled using the decoupled current control for both charging the batteries from grid, and discharging the batteries to send the power to the grid. Both the decoupled current control and the active power control, Fig. 8, for the inverter have been tested and showed a good performance in the previous works, [14]-[16]. The dc bus voltage balancing control for each cell described in the literatures [17],[18] is not considered in this design, since the high gain dc/dc converter in each cell regulates and balances the dc independently in charging and discharging mode. This method of using the dc/dc gain converter to balance the dc bus voltage for each cell, offers a flexibility, a simplicity, a robust transient and a steady-state response, Fig. 9. The conventional phase-shift (CPS) technique is a simple way to regulate the power flow of DAB converters, since the waveforms of the two voltages generated by the two active bridges are both square waves with 50% duty ratio, Fig. 4 and it only controls the phase-shift ratio between the two voltages [19]-[21]. To reach the MW power level, the dc droop control is used for balancing and regulating the dc bus of each H-bridge cell, as shown in Fig.3. The dc/dc converters are operated in parallel to avoid circulating current, Fig. 7

The inverter works as a current source for both supplying the power to the grid or sinking the power from the grid to charge the batteries. Both the active power control of individual converter cells and the active-power control of the whole three-phase converter cells are controlled, as presented in [15]. The feedback loop, is used to make sure that the power at the dc side of each cell, $\boldsymbol{P_{un}}$, is equal to the respective command at the ac side, $\boldsymbol{P^*_{un}}$. The PI controller is used with a proportional gain, Ki and a time integral, T, as shown in Fig. 8. The power-handling capacities of all the twelve battery banks in Fig. 2 are equal, the respective active power commands for each phase are equal ($\boldsymbol{P^*_{un}} = \boldsymbol{P^*_{vn}} = \boldsymbol{P^*_{wn}}$). $\boldsymbol{P^*_{un}}$ denotes the ac active power command for phase A. $\boldsymbol{P^*_{vn}}$ denotes the ac active power command for phase B. $\boldsymbol{P^*_{wn}}$ denotes the ac active power command for phase C. The modulating signals are solely determined by the active power control of the whole converter cells, $\boldsymbol{P^*}$. The active power control is explained in the paper [14]. As shown in Fig. 8, the decoupled current control is used following the power command, $\boldsymbol{P^*}$ to either charge or discharge the batteries.

Based on the decoupled current control, shown in Fig. 8, the current signals are sensed for each phase. $\boldsymbol{i_u}$ is the current sensed before the filter in phase A. $\boldsymbol{i_V}$ is the current sensed before the filter in phase B. $\boldsymbol{i_w}$ is the current sensed before the filter in phase C. The grid voltages are also sensed for each phase. $\boldsymbol{V_{g\_u}}$ denotes the sensed voltage for grid voltage phase A. $\boldsymbol{V_{g\_v}}$ denotes the sensed voltage for grid voltage phase B. $\boldsymbol{V_{g\_w}}$ denotes the sensed voltage for grid voltage phase C. The d-q transform is applied on both the sensed currents and

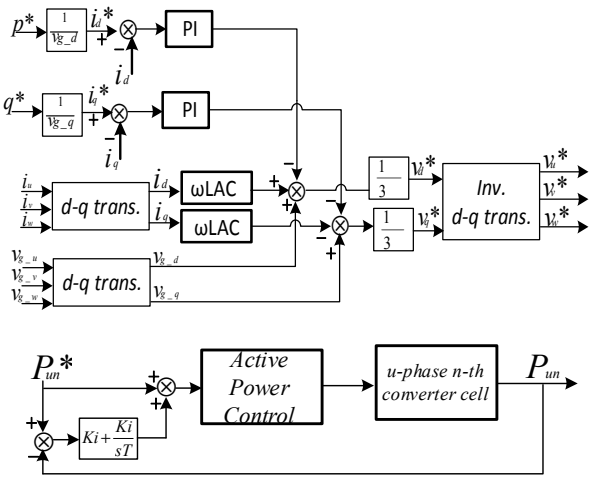

Fig. 8. Decoupled current control and active power control.

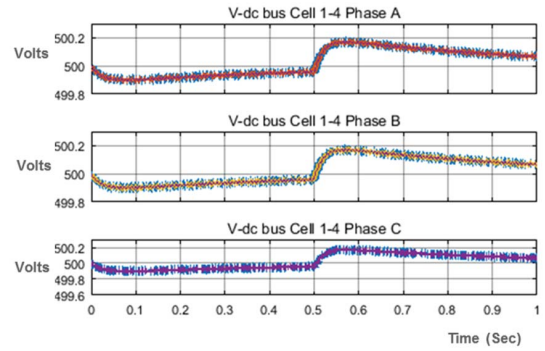

Fig. 9. Cells DC links voltages

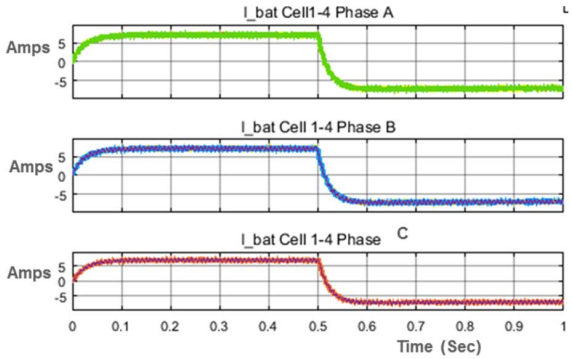

Fig. 10. Both discharging and charging and modes

voltages. The resulting current reference ($\boldsymbol{i_d^*}$) is computed proportionally to the power command, $\boldsymbol{P^*}$, for the overall three-phase CHB modular multilevel inverter. The modulating signals for CHB dc/ac converter are generated using phase-shift control, for the switching devices to equally share the thermal stress, [2], [3], and [12].

III. SIMULATION RESULTS

A detailed MATLAB/Simulink model was developed and the respective controls were applied to examine the performance

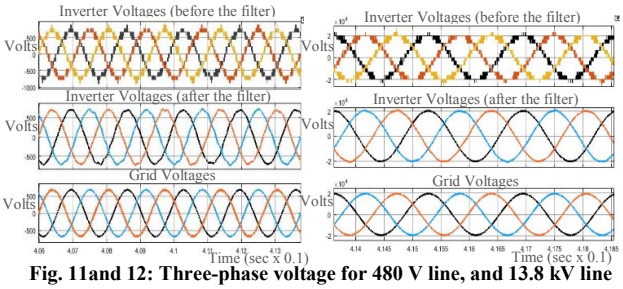

Fig. 11and 12: Three-phase voltage for 480 V line, and 13.8 kV line

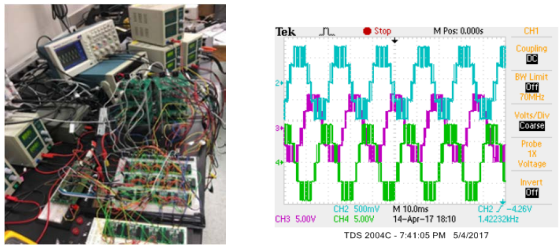

Fig. 13 and 14. Three-phase voltage, low-voltage, 5-level CHB converter, and experimental results

of the topology to integrate the BESS into a medium voltage distribution without the use of a 60 Hz bulk transformer. The simulation for both discharging and charging the battery modules are presented in Fig. 9 and Fig. 10. Fig. 9 shows the performance of the dc bus voltage control described in Fig. 4 for a dc/dc stage of each cell. In Fig. 9, from 0 to 0. 5 seconds, for example, the voltage is regulated at 500 V during discharging mode. At 0. 5 sec, when the system transitions from discharging mode to charging mode, the dc bus voltage is still regulated at 500 V with a good transient response. From 0.5 sec to 1 second, the system is in charging mode. All the battery banks for each cell and each phase are charging at the same rate, -5 A. Similarly, in discharging mode, all batteries are discharging at the same rate, 5 A. The simulation results in Fig. 9 and Fig. 10 proves that the system can operate with a balanced SOC, by making sure that all batteries are discharging and charging at the same rate. The output waveforms of the overall three-phase modular multilevel inverter and the grid voltages are shown in Fig. 11 and 12, for a 480 V line and a 13.8 kV line respectively. A more extensive study of a system controls response in case of imbalance faults in the distribution system will be reported in the future publications.

IV. EXPERIMENTAL VERIFICATION

To extensively analyze the performance of the SiC-based power electronics interface to integrate the BESS into a medium voltage distribution system, three different versions of prototypes are built. The first version, a 5-level CHB inverter, a low voltage prototype up to 240 V rms, in Fig. 13 and Fig. 15, has been tested. Fig. 13 shows the hardware for a 5-level CHB inverter, for both the dc/dc stage and dc/ac stage. Fig. 14 shows the output three-phase voltage of a low-scale 5-level modular multilevel converter. Fig. 16 shows a voltage per phase, which is sensed before the filter in the prototype. Fig. 17 and Fig. 18 show the testing results of dc/dc stage and ac voltage at the point of coupling with the grid respectively. In Fig. 18, CH3 shows the ac voltage and CH1 shows the phase current.

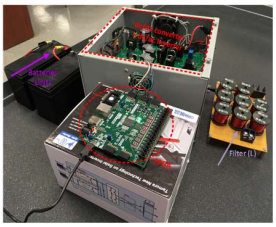

Fig. 15. A 240 Vrms prototype

Fig. 17. The dc/dc converter waveforms

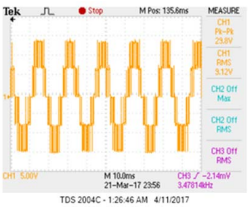

Fig. 16. Phase-voltage before the filter

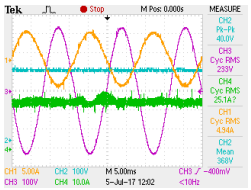

Fig. 18. Results for one phase

A medium voltage version of the prototype at the kV scale is being constructed, using CREE 1.2 kV SiC MOSFETs switching devices, part# HT-3201-R; its experimental results at kV scale will be presented in a future paper. By using 1.2 Kv SiC MOSFETs, the maximum voltage that nine-level CHB three-phase inverter can generate is 3 kV rms, 3Φ output. The experimental results of 3 kV rms, 3Φ output prototype will be analyzed and used to optimize the design and construction of the final prototype rated at 13.8 kV rms, 3Φ output. The prototype for a 13.8 kV rms, 3Φ output, will be built using 10 kV SiC MOSFETs.

The controls are implemented using a DSP TMS320F28335 and verified on a low-voltage prototype, Fig. 13 and 15. Moreover, an FPGA Artix-7, "xc7a100tcsg324-1" is used, and the controls are developed using the Nexys 4 DDR board. The experimental results of the dc/dc converter are shown both in Fig. 17 and Fig. 18; such as the current flowing in the primary side of the HF-XFMR, (CH4, green) in Fig. 17. The current flowing through the synchronous buck/boost converter, (CH4) and dc bus voltage (CH2) are shown in Fig. 18.

V. CONCLUSIONS

This paper presents a selected prototype, a cascaded H-bridge modular multi-level inverter, for a SiC-based power electronics interface to integrate a battery energy storage into the medium distribution system. The topology and respective controls have been verified. The plan for both the kV scalability and MW power scalability of the topology have also been presented. The dc droop control is considered for balancing the dc bus for each cell for MW power-scale application. The dc bus balancing control is simplified by using the dc/dc gain converter to regulate the dc bus for each cell. The simulation results at kV scale and the experimental results of the low voltage prototype provides the verification of the topology and controls. More extensive study will be presented in the future papers. The comparison between the design method of using series-connected battery banks or parallel battery banks with high gain dc/dc converters to provide the required dc bus voltage for medium voltage application will also be described in the future publication

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