# *A Novel Single-Stage High-Frequency Boost Inverter for PV Grid-Tie Applications*


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***Abstract*— this paper proposes a new topology for a single-phase grid-tie DC-AC boost inverter for the application of PV systems that utilize high-frequency transformer for galvanic isolation. In the first stage, a new single-stage high-frequency boost inverter is proposed to boost and convert the DC output voltage of the PV modules to a high-frequency single-phase square waveform in addition to extracting maximum power point (MPP) from PV modules. The second stage is a direct single-phase AC-AC matrix converter that interfaces the system to the grid. Therefore, a single-phase high-frequency transformer is used to link both stages and provide isolation between the AC and DC sides. The proposed system has many advantages such as increasing the inverter output voltage level, maximum power point tracking (MPPT), high reliability, safety, small size and light weight. The proposed topology has been verified analytically by using PSIM software and experimentally by using a laboratory prototype.**



***Keywords—photovoltaic; grid connected; boost inverter; high frequency transformer.***


## I. INTRODUCTION

In the last few years' renewable energy has the greatest growth compared to other energy resources due to its reliability, availability, maintainability , safety, free, green and inexhaustible [1-3]. Therefore, many literatures have been recently published in solutions to increase the reliability of the solar energy resources. PV grid-connected system should perform maximum power tracking (MPPT), voltage boosting, galvanic isolation for safety purposes, injection of high quality low harmonics AC power to the grid and using high efficient and reliable implementation [4-7].

Several topologies for PV grid connected inverter have been presented; generally, there are two types of grid-connected PV systems, those with galvanic isolation and without galvanic isolation. Galvanic isolation can be implemented with either a line frequency or a high frequency transformer. By contrast, topologies without galvanic isolation are transformerless topologies.

Due to the high voltage boost required to interface the low output voltage of the PV module to the grid, the use of a line frequency transformer is widespread [8-9]. Besides stepping up the voltage, it plays an important role in safety purpose and personal protection by providing galvanic isolation between the grid and the PV system, thus eliminating leakage current and avoiding dc current injection into the grid. Nevertheless, the line frequency transforms are large, heavy, and expensive, the whole system is bulky and hard to install as a result of its low frequency [10-11]. Therefore, the topology with line frequency transformer is regarded as a poor solution and thus is increasingly replaced by high-frequency transformers (HFT). Using HFT [12-15] guarantees galvanic isolation between the grid and the PV system, in addition to overcoming the disadvantages of using conventional line frequency transformer as mentioned [16-17]. However, there is a rarity in scientific research for using HFT in PV systems in a way that performs all the required functions, especially MPPT.

Transformerless topologies [18-22] are more efficient, lighter, less bulky, and less costly than the isolated inverters. However, a main concern to be addressed in nonisolated PV inverters is the grounding and the leakage ground currents through the solar panel parasitic capacitance in addition to dc current injected to the grid [23]. Dangerous leakage current increases system losses, reduces the grid-connected current quality, induces severe conducted and radiated electromagnetic interface and causes personal safety problems. To keep the leakage and dc currents injected to the grid under control requires more complex solutions.

In [24], a Single-Stage transformerless topology is presented; the proposed topology is simple, symmetrical and easy to control. These features encourage redesigning the topology in this paper to obtain a 10-kHz square wave output voltage instead of the fundamental grid voltage. Therefore, special design boost inverter is proposed to meet the requirements of HFT and configure a multi-featured system.

This paper is organized as follows; firstly, the circuit configuration of the proposed system is described. Secondly, the operation modes of the proposed topology are presented. Thirdly, MPPT algorithm is discussed. Fourthly, mathematical analysis and power stage parameters design are deduced. Finally, the fundamental operation waveforms of the proposed system are considered by simulations and experiments.

## II. CIRCUIT TOPOLOGY

### *A) conventinal topology*

In order to interface the PV inverters to the grid, a voltage stepping up operation is required to meet the low voltage PV panels, which is normally achieved by transformers. A simple topology is shown in Fig. 1. This topology uses a line frequency (60Hz) transformer to step up the inverter voltage and interface to the grid. Furthermore the transformers provide electrical isolation which is important from safety perspective. The boost-stage is used for MPPT, which is performed on the boost converter switch. This topology is suitable for low power ratings of few hundreds of watts. As the power level increases, the size of the interface transformer increases. This results in bulky power circuit and losses in magnetics can also be significant.

### *B) proposed topology (basic version)*

The proposed system consists of two stages, high-frequency boost inverter (HFBI) cascaded by single-phase direct AC-AC matrix converter, as shown in Fig. 2. In this paper the discussions are focused on the first stage. Therefore, the second stage is simply approximated by a resistor. The proposed topology is designed to provide a 10-kHz square wave output voltage to meet the requirements of HFT. The topology consists of two buck-boost converters connected as shown in Fig. 3. Each one of these two converters operates sequentially in DCM for one half cycle of the targeted 10 kHz square waveform. DCM operation prevents the circulating currents between the inductor and the parallel connected switch in the next operating half cycle. The power MOSFETS $SW_1$ and $SW_3$ is switched at high frequency of 100 kHz while $SW_2$ (or $SW_4$) is kept continuously ON during the positive half cycle (or negative half cycle) of the targeted 10 kHz square waveform.

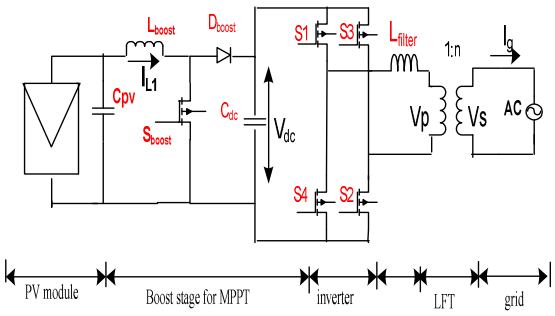


Fig. 1. Conventional topology with line frequency transformer

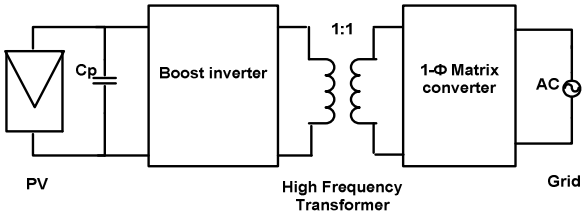


Fig. 2. The proposed system.

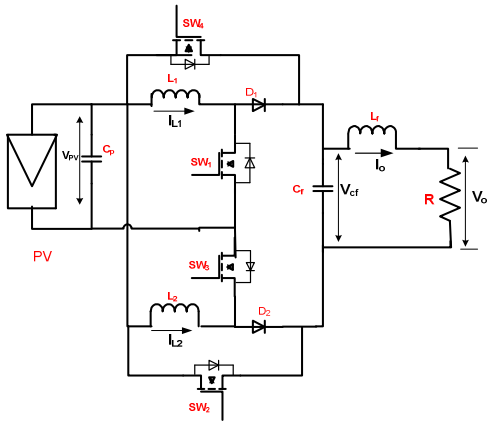


Fig. 3. Configuration of the single-stage HF buck-boost inverter.

Switches $SW_1$ and $SW_2$ operate to provide the positive boosted half-cycle, whereas $SW_3$ and $SW_4$ operate to provide the negative boosted half-cycle. When $SW_1$ is ON (or $SW_3$), energy is stored in the buck-boost inductor "$L_1$" (or $L_2$) by the PV source. When $SW_1$ (or $SW_3$) is OFF, $D_1$ (or $D_2$) gets forward biased, discharging the stored inductor energy into capacitor $C_f$, which continuously feeds current to the load. The switched gate signals Vg1, Vg2, Vg3 and Vg4 for $SW_1$, $SW_2$, $SW_3$ and $SW_4$ respectively are shown in fig. 4.

### *C) Modified proposed topology*

The target of the proposed topology is a 10 kHz square waveform output voltage that is linked to the matrix converter input by HFT. Therefore, the topology is designed to achieve many features of the complete system as mentioned previously. But at the instant of turning the operation between the two buck boost, the polarity of the capacitor voltage $V_{cf}$ cannot change instantaneously. Although this time is very short (2 ns) but two paths of surge current appear due to high value of $V_{cf}$ compared to the input voltage. Assuming the polarity of $V_{cf}$ changed from the positive half cycle to negative half cycle and by referring to fig. 3, the first path of surge current flows through capacitor $C_f$, switch $SW_4$ and body diode of switch $SW_2$. The second path of surge current flows through capacitor $C_f$, switch $SW_4$, input capacitor $C_p$ and body diode of switch SW3. In order to limit this surge current, two stages of modification have been

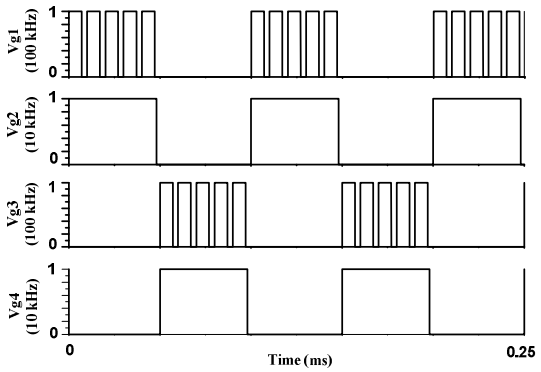


Fig. 4. The switching pulses at the gates of switches.

proposed. The first one by using bi-directional switch for $SW_2$ and $SW_4$ and adding series diode in opposite direction of the body diode of $SW_1$ and $SW_3$. Consequently, the capacitor current $I_{cf}$ is limited by flowing through inductor $L_2$. Although, the surge current is limited, it is added to the source current in inductor $L_2$ ($SW_3$ is on) at the instant of changing the polarity of $V_{cf}$, resulting in rising the output voltage at the begging of each half cycle. In order to obtain proper square wave shape, the second stage of modification was done by keeping $SW_1$ and $SW_3$ in OFF state at this instant. The modified switched gate signals Vg1 and Vg3 for $SW_1$ and $SW_3$ respectively are shown in fig. 5.

## III. THE OPERATION MODES

During the positive half-cycle, the boost inverter has three modes of operation based on the switching of $SW_1$ during its switching time period $T_s$ as shown in fig. 6, since the switch $SW_2$ is always ON during these three modes. In Mode1, switch $SW_1$ is ON and energy is stored in the buck boost inductor $L_1$ by the PV source. In Mode 2, switch $SW_1$ is OFF and $D_1$ is forward biased, discharging the stored inductor energy into capacitor $C_f$, which feeds current to the load (R). In Mode 3, both $SW_1$ and $D_1$ are OFF as a result of DCM operation.

In mode 1 ($0 < t \leq T_{on}$), inductor voltage and capacitor current in this mode are given as follows;

$$V_{L_1}(t) = L_1 \frac{dI_{L_1}(t)}{dt} = V_{pv}(t) \quad (1)$$

$$I_{c_f}(t) = C_f \frac{dV_{c_f}(t)}{dt} = -\frac{V_o(t)}{R} \quad (2)$$

In mode 2 ($T_{on} < t \leq T_{off}$), inductor voltage and capacitor current in this mode are given as follows;

$$V_{L_1}(t) = L_1 \frac{dI_{L_1}(t)}{dt} = -V_{c_f}(t) = -V_{L_f}(t) - V_o(t) \quad (3)$$

$$I_{c_f}(t) = C_f \frac{dV_{c_f}(t)}{dt} = I_{L_1}(t) - \frac{V_o(t)}{R} \quad (4)$$

In mode 3 ($T_{off} < t \leq T_{d\text{-}off}$), inductor voltage and capacitor current in this mode are given as follows;

$$V_{L_1}(t) = L_1 \frac{dI_{L_1}(t)}{dt} = 0 \quad (5)$$

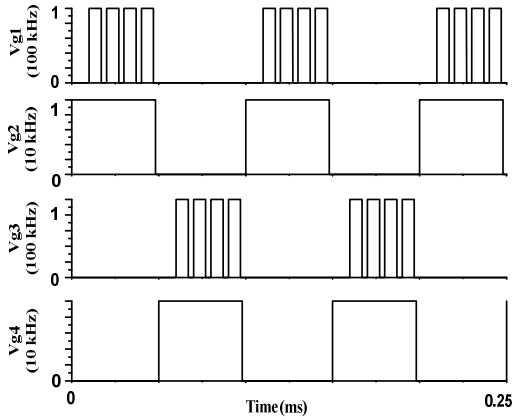


Fig. 5. The modified switching pulses at the gates of switches.

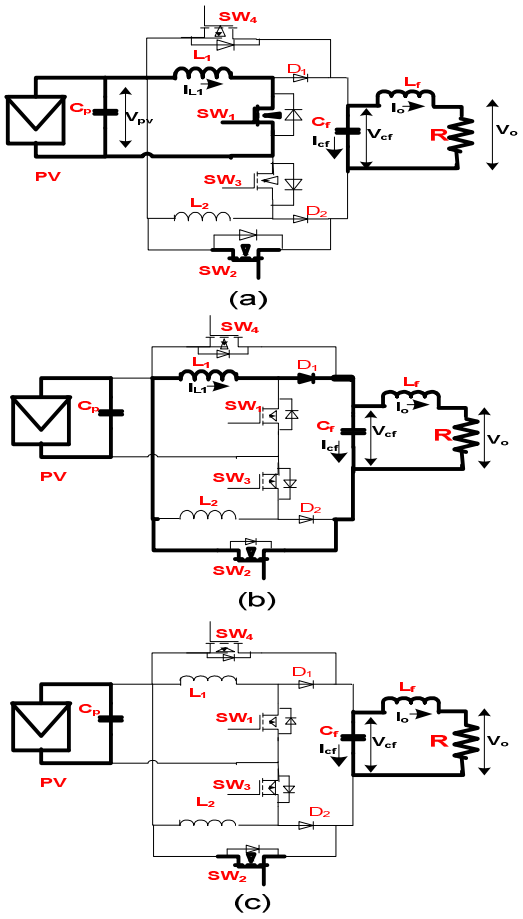


Fig. 6. Operation modes (a) when $SW_1$ is on, (b) when $SW_1$ is off and $D_1$ is on, (c) when $SW_1$ and $D_1$ are off.

$$I_{c_f}(t) = C_f \frac{dV_{c_f}(t)}{dt} = -\frac{V_o(t)}{R} \quad (6)$$

Likewise, the inductor voltage and capacitor current can be obtained in the negative half-sycle of the high frequancy output voltage when the second buck boost inverter is activated.

## IV. ANALYSIS AND PARAMETERS DESIGN

For simplification some assumptions for analyzing the proposed topology have been considered as follow,

1. Switching frequency is (n) times the square wave output voltage where (n) is even number.
2. DCM operation during each cycle of the output voltage.
3. The output voltage is constant during each half cycle.
4. The value of the duty cycle ($D = T_{on} / T_s$) is constant during each cycle of the output voltage.
5. The PV capacitor $C_{pv}$ provides constant voltage during each cycle of the of the output voltage.
6. The nonideality of the boost inverter is neglected.

### A. *Boost inverter voltage gain*

Related to the assumption (1 and 2) the stored energy in the buck-boost inductor $L_1$ (or $L_2$) is discharged into capacitor $C_f$ which feeds it into the load. Using assumption (5), the energy delivered into the load $E_o(t)$ is equal to the energy

drown from the source $E_{pv}(t)$ during the switching time period $T_s$.

$$E_{pv}(t) = \frac{1}{2} L_1 I_{L_1}^2 \quad (7)$$

According to (1), the peak value of the inductor current can be formulated as follows;

$$I_{L_1} = \frac{V_{pv}}{L_1} D T_s \quad (8)$$

Substituting by (8) in (7) yields:

$$E_{pv}(t) = \frac{V_{pv_1}^2}{2L_1} D^2 {T_s}^2 \quad (9)$$

The energy transferred into the load during switching time period $T_s$ is given by:

$$E_o(t) = V_o \times I_o \times T_s = \frac{{V_o}^2}{R} T_s \quad (10)$$

Equalizing (9) and (10) yields the formula of the boost converter voltage gain as follows,

$$\frac{V_o}{V_{pv}} = \sqrt{\left(D^2 \times T_s \times \frac{R}{2L_1}\right)} \quad (11)$$

### B. *Condition for DCM*

According to the principle of inductor volt-second balance and capacitor charge balance [25], the dc component of the voltage applied to an inductor must be zero. Also, the dc component of current applied to a capacitor must be zero. These principles for any circuit that operate in steady state. by applying these principles to (1), (3) and (5) and using the assumption (5) yields:

$$V_{L_1}(t) = L_1 \frac{dI_{L_1}(t)}{dt} = V_{pv} T_{on} - V_o T_{off} + 0\, T_{d-off} = 0 \quad (12)$$

Consequently,

$$T_{off} = V_{pv} T_{on} / V_o \quad (13)$$

For critical conduction mode or DCM during switching period,

$$T_{on} + T_{off} \leq T_s \quad (14)$$

Using (14) in (13) yields;

$$D T_s + (V_{pv} D T_s / V_o) \leq T_s \quad (15)$$

This lead to the condition of the DCM of the boost inverter

$$D \leq \frac{1}{1 + V_{pv}/V_o} \quad (16)$$

### C. *Boost inverter parameters design*

As a result of DCM operation, the energy stored in the inductor $L_1$ is completely transferred into capacitor $C_f$ which feeds it into the load during each switching period. Therefore (11) is used to determine the value of the inductor $L_1$ and (16) is taking into consideration to guarantee DCM operation, resulting the following expression:

$$L_1 \leq \frac{V_{pv}^2 D^2 T_s}{2P} \quad (17)$$

where; P is the rated power transferred into the load.

To determine the value of $C_f$ [24], the energy stored in the inductor $L_1$ during the ON mode can be equated to the change in capacitor energy during the OFF mode, yields the following expression:

$$C_f \leq \frac{L_1 I_{pk-L1}^2}{4V_o \Delta V} \leq \frac{V_o T_s}{2R \Delta V} \quad (18)$$

where; $\Delta V$ is the ripple of the capacitor voltage.

The high switching frequency component in the current waveform is filtered by inductor filter ($L_f$). Its design depends on the cut-off frequency ($F_c$) as follows;

$$L_f = \frac{1}{(2\pi \times F_c)^2 \times C_f} \quad (19)$$

## V. MAXIMUM POWER POINT TRACKING ALGORITHM

The operating point of the PV sources may change randomly during the operation of the system . Therefore, a MPPT algorithm is necessary so that the maximum instantaneous power can be extracted and delivered to the load. Several MPPT techniques have been proposed in the last decades. P&O MPPT algorithm [26-27] is one of simple hill-climbing algorithms and widely used in practical PV systems because of its simplicity, In addition; it does not require prior study or modeling of the source characteristics. Fig. 7 depicts a flow chart explaining P&O MPPT algorithm. It operates by perturbing the PV array voltage (i.e. incrementing or decreasing) and comparing the PV output power with that of the previous perturbation cycle. If the perturbation leads to an increase (decrease) in array power, the subsequent perturbation is made in the same (opposite) direction, respectively. When the perturbation of the algorithm has three-level at steady-state, it means that the algorithm is stable and swings around the MPP.

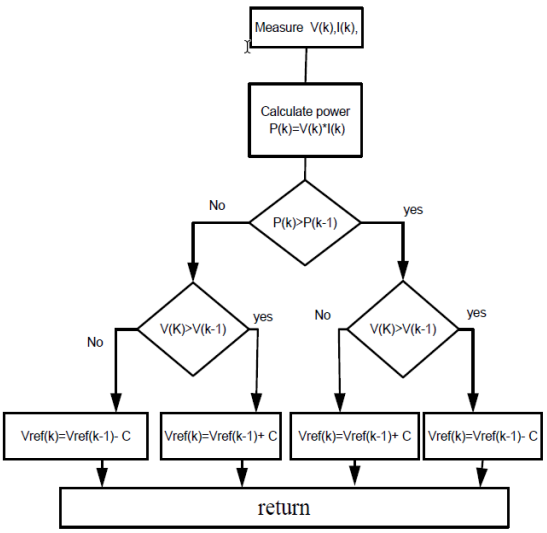


Fig. 7. Flowchart of the P&O algorithm.

## VI. SIMULATION RESULTS

In order to validate the operation of the proposed topology, it has been carried out in PSIM software (ver. 10.0). the second stage of the proposed system is simply approximated by a resistor. 250W PV module is simulated at 25° C temperature and 1000W/m$^2$ radiation. The simulated circuit parameters for a PV module voltage $V_{pv}$ =45 V, output voltage $V_o$= 220 V, resistor R= 200 Ω and ripple of the capacitor voltage $\Delta V = 0.1V_o$ are calculated as the following; Using (16), the value of duty cycle $D \leq 0.83$. The value of buck-boost inductor $L_1$ and $L_2$ for 250 W PV power and $T_s$ is 10µs are given by using (17), $L_{1,2} \leq 28$ µH. In PSIM simulation a lower value of $L_1$ and $L_2$ are used to a void CCM operation for power greater than the rated power. The value of $C_f$ is given by (18), $Cf \leq 250$nF. The value of filter inductor $L_f$ for 100 kHz switching frequency is given by (19), Lf = 10 µH. The simulated circuit parameters and the electrical characteristics of PV module at MPP are listed in Table I.

TABLE I. PROPOSED SIMULATED CIRCUIT PARAMETERS

| Symbol | Meaning | Value |
|---|---|---|
| $L_1$=$L_2$ | HFBI inductors | 20 µH |
| $C_f$ | HFBI Filter capacitor | 250 nF |
| $L_f$ | HFBI Filter inductor | 10 µH |
| $V_{pv}$ | Electrical characteristics of PV module at MPP. | 45 V |
| $I_{pv}$ | | 5.6 A |
| $P_{pv}$ | | 250 W |

Fig.8 shows the PV outputs ($V_{pv}$, $I_{pv}$ and $P_{pv}$) at MPP and the duty cycle perturbation (output of MPPT algorithm). It is clear that the duty cycle perturbation has three-level at steady-state, which indicates that P&O MPPT algorithm is stable and swings around the MPP.

The important waveforms corresponding to the basic version of the proposed topology are shown in fig. 9. Switches $SW_1$ and $SW_3$ are responsible of boosting the input voltage

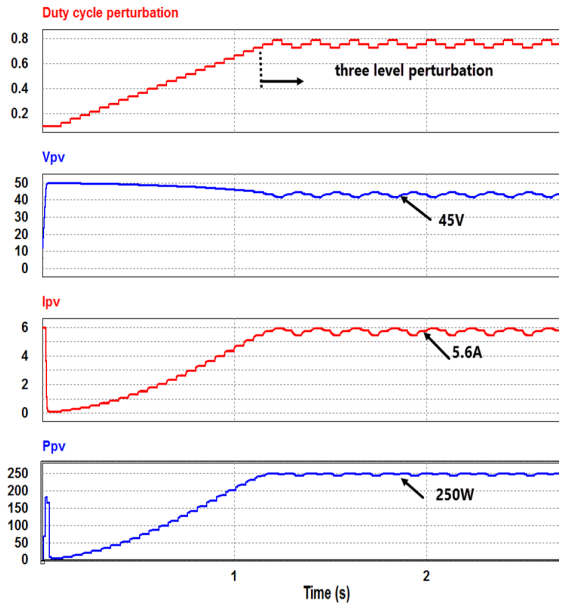


Fig. 8: Simulation Results of $I_{pv}$, $V_{pv}$ and $P_{pv}$ of PV module at MPP and the duty cycle perturbation.

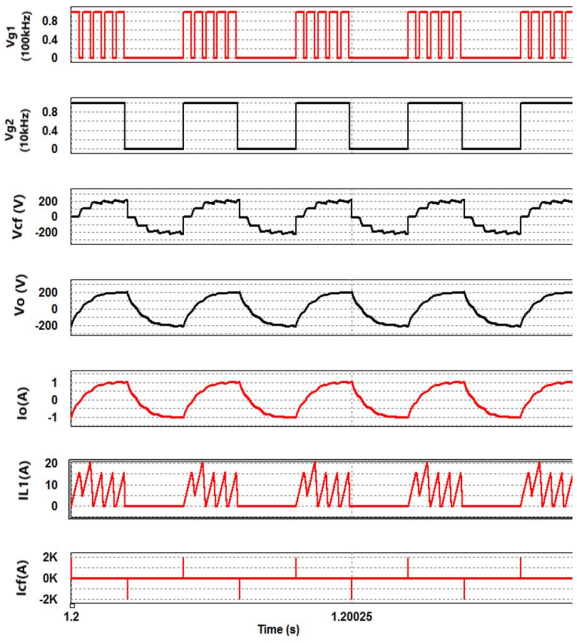


Fig. 9. Simulated waveforms of the basic version of the proposed topology.

Therefore; the switch gate signal Vg1 and Vg3 are obtained by gate driver after modulating the duty cycle by MPPT algorithm and compered by 100 kHz saw-tooth carrier signal to give five pulses during each half cycle of the output voltage. Switches $SW_2$ and $SW_4$ are responsible of inverting process therefore; the switch gate signal Vg2 and Vg4 are obtained by gate driver after comparing 0.5 dc reference signal by 10 kHz saw-tooth carrier signal to give the targeted 10 kHz output voltage. It is clear that capacitor voltage ($V_{cf}$) is dropped rabidly at the instant of inverting process due to the short circuit capacitor current flowing in this instant as discussed is section II. The inductor $L_{1,2}$ are designed by taking in consideration DCM condition as shown in fig. 9 the inductor current equal zero at the end of its operating half cycle which is mean that, the energy stored in the inductor $L_{1,2}$ is completely transferred into capacitor $C_f$. Otherwise, this stored energy causes circulating current between inductor and the parallel connected switch in the next operating half cycle.

The simulated waveforms corresponding to the modified proposed topology are shown in fig. 10 and 11. By using bi-directional switch for $SW_2$ and $SW_4$ and adding diode in opposite direction of the body diode of $SW_1$ and $SW_3$ in the first stage of modification, the surge current of capacitor $C_f$ is limited as shown in fig. 10. Although the short circuit current is limited, it is added to the source current in inductor of the next operating half cycle at the instant of changing the polarity of $V_{cf}$, resulting on raising the output voltage at the begging of each half cycle. In order to obtain proper square wave shape the second stage of modification is done by modifying switched gate signals of $SW_1$ and $SW_3$ as shown in fig. 5. The modified simulated results of the proposed topology are shown in fig. 11.

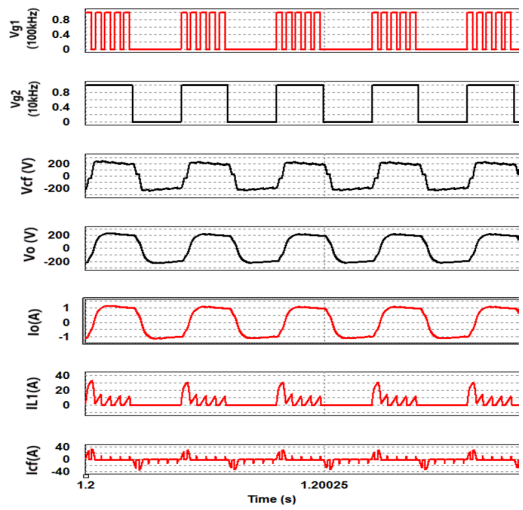


Fig. 10. Simulated waveforms of the first stage of modification.

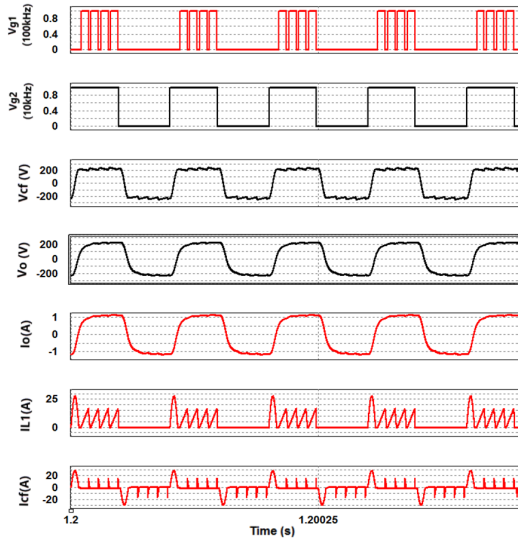


Fig. 11. Simulated waveforms of the modified proposed topology.

## VII. EXPEREMENTAL RESULTS

A200-W experimental prototype has been carried out in the laboratory to verify the operation of the proposed topology. The second stage of the proposed system is simply approximated by a resistor and PV module is considered as dc source with 45V. Fig. 12 shows the photograph of the experimental prototype. The PWM switching signals, which are applied to the gate drives, are obtained by using FPGA (PE-Expeart3). For design and selection of devices, the peak and RMS values of currents and voltages are required which were determined using simulations. Fig.13 shows the experimental results of the modified proposed topology at 45 V input voltage of the dc supply considering same parameters of the circuit. The capacitor voltage is square wave with 200 V amplitude and 10 kHz. Also the voltage across the resistor and the output current are shown with 190 V and 1.5A peak values, respectively. The inductor current of the buck-boost inverter is DCM in order to guarantee discharging all its energy and confirming no circulating current during negative half cycle.

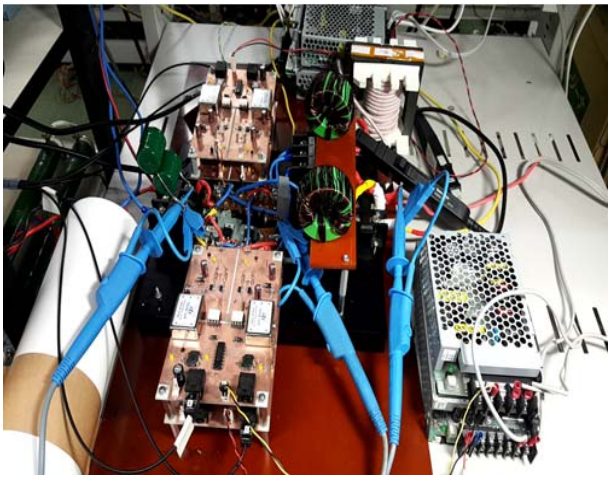

Fig. 12. Photograph of the experimental prototype.

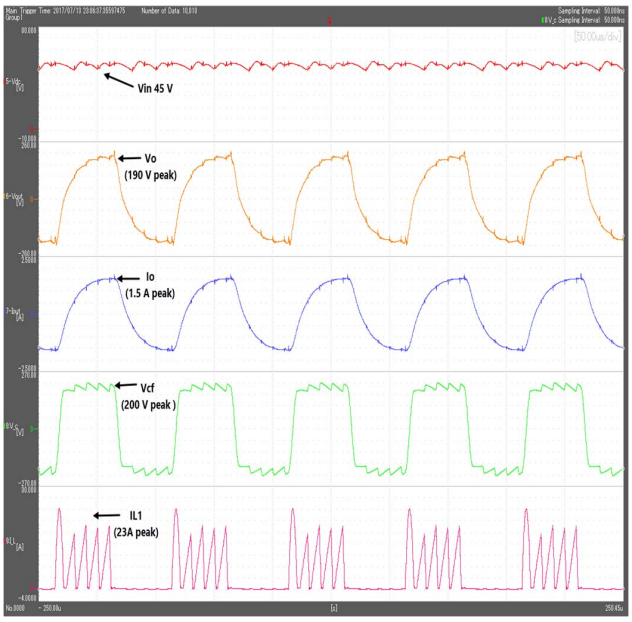


Fig. 13. Experimental results of the modified proposed topology.

## VIII. CONCLUSIONS

This paper has proposed a new single-stage high-frequency boost inverter for PV grid-tie applications. the topology has been designed, analyzed, simulated and implemented in laboratory. The topology provides many features such as boosting the PV voltage, MPPT, in addition to providing the high frequency square wave output voltage that allows the use of HFT and matrix converter to connect PV system to the utility grid. This proposed system performs MPPT, voltage boosting, galvanic isolation between grid and PV system for safety purposes, small size and light weight and reliable implementation. The proposed topology uses only one stage with reduced power switches compared with the conventional topology.

Analysis of the operation modes of the proposed topology and a design procedure has been performed. The functionality and switching operation of single-stage boost

inverter in closed loop have been depicted with simulation results to verify the operation modes of the topology and extracting MPP from PV module. The functionality and switching operation of proposed topology in open loop have been depicted with experimental results for resistive load.

the presented experimental results show a boosting of more than 4 times, which means that low PV array voltages (typically 40- 100 V range) can be boosted up to levels capable of interfacing with the grid voltage (110- 230 V ac). Consequently, a few number of PV modules connected in series is sufficient and this helps in overcoming the environmental variations such as shadow, which reduce the utilization of the PV modules.

Simulation and experimental results, emphasizing the performance of the proposed topology of single-stage high frequency boost inverter is validated.

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