Two-Phase X-Type Current Source Rectifier With Reduced Active Switch Count for Open-End Permanent-Magnet Synchronous Generator

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***Abstract*— In this paper two two-phase current source open-end asymmetric rectifiers are proposed. These new rectifiers are derived from an improved multi-phase crossed switches current source converter, named X-type CSC. The X-type CSC presents independent full quadrant operation, lower DC-bus current value, high magnetic power density, higher efficiency (when compared to similar ones), and high AC output voltage waveform quality. Being used exclusively as a rectifier, the X-type CSC can be even further improved. One can replace the series switch-diode configurations by only diodes, resulting in an asymmetric converter with only four active switches. With this modification, the efficiency can be increased and the cost reduced. The two-phase asymmetric X-type current source rectifiers are presented with their respective pulse-width modulation technique and also proper control technique. Simulation and experimental results are presented in order to validate the theoretical approach. At last, a comparison of the studied topologies is made and the best converter is selected.**

I. Introduction

With the increase demand for power for the development of humankind and the damage caused to the planet by the use of fossil fuels, renewable and alternative power generation technologies have been gaining attention. The wind energy conversion system (WECS) are one of the main renewable power sources [1], and the power electronics are a key component of these systems. The power conversion system that drives the generators have been of increase interest of many researchers. The voltage source converters (VSCs) have been widely used as the power converters for permanent-magnet synchronous generator (PMSG) drives [2]–[7]. On the other hand, the current source converters (CSCs) are not as explored as the VSCs for PMSG drives [8], [9]. Most of the CSC solutions are for high-power applications.

Even thought the CSCs are used for PMSG drives, they are less attractive when compared to the VSCs due to two main facts: high conduction losses in the switches and the DC-bus elements (inductors); and the low power density of the inductors.

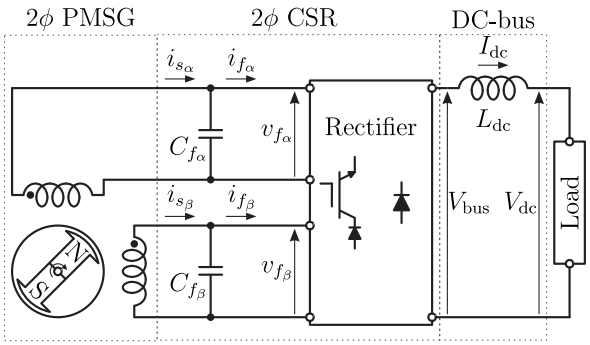


Fig. 1. Two-phase X-type CSRs family driving a PMSG and supplying a generic load.

Despite those drawbacks, the CSCs have some inherent characteristics that are advantageous when compared to the VSCs, such as: natural protection against short-circuit through the DC-bus; boost inverter or buck rectifier capability due to the current modulation; and low $\mathrm{d}v/\mathrm{d}t$ in the AC side of the converter [10]. Also, new IGBTs with reverse blocking capability (RBIGBTs) [8], [11], that present lower conduction losses, are bringing the CSCs to the same level of efficiency when compared to the VSCs. These characteristics show that the CSCs are a family of converters that are viable alternative to the VSCs.

This paper presents two two-phase current source rectifiers (CSRs). The two new converters e.g. can be applied as a PMSG drive unit. Two-phase systems are an alternative solution for low and medium power applications. They use equal or less components than the three-phase solutions, and have a higher power density than the single-phase converters. Some papers are addressing two-phase PMSG drives using VSCs [4]–[7], but none are using two-phase CSCs.

This paper presents two similar two-phase CSR topologies, which are idealized to drive an open-end PMSG. Replacing part of the active switches by diodes, an asymmetric technique, which is commonly used in VSRs [4], [5], [12], can be used

in asymmetric CSRs [13]. The proposed converters have an improved two-phase crossed switches CSC (X-type CSC or XCSC) as basis, which was proposed in [14], further generalized in [15], and selected as the best one of a family of two-phase CSCs in [16]. However, the proposed converters have four RBIGBTs and four diodes, which replace the other four RBIGBTs of the original topology. Due to this modifications, new PWMs are required.

From the improved XCSC, as shown in Fig. 2, one can find the two new topologies that are presented in this paper: the High/Low Asymmetric X-type Current Source Rectifier (HL-aXCSR) (Fig. 4(a)), which replaces the middle switches by diodes; and the Middle Asymmetric X-type Current Source Rectifier (M-aXCSR) (Fig. 4(b)), which replaces the top and bottom switches by diodes. It is worth to note that due to the diodes, the input AC currents and voltages must be synchronized, which is the main reason that these converters are suitable for an open-end PMSG drive (Fig. 1).

II. Current Source Rectifiers Operation and PWM

By using an electric machine (EM) in open-end being driven by a VSCs, the DC-bus voltage can be reduced [12]. In order to drive an EM in open-end using a conventional CSC, one would have to connect n legs of the converter in parallel. However, the parallel connection for the CSCs implies in a larger DC-bus current, resulting in an increase of conduction losses and the need for bulkier inductors and semiconductors. In order to solve this problem, the series connection of the converters is more suitable, as it is shown in the following subsection.

A. Full-controlled

The series connection of full-controlled H bridge single-phase CSCs allow to operate with a reduced DC-bus current. However this implies in more switches to be conducting per switching cycle, once, in CSCs, one switch per row must conduct at any time. Thus the full controlled two-phase CSR will present four conducting switchers per cycle in two-phase systems.

Despite the achievement of a lower DC-bus current, the number of conducting switches will increase the switching and conduction losses. In order to reduce the conduction losses, an improved converter was proposed in [14], and selected as the best converter of a family of two-phase CSCs [16]. The two-phase improved converter with reduced number of conducting switches is presented in Fig. 2. The PWM for the improved two-phase converter can be found in [14], and it is replicated in Fig. 3.

However, when operating exclusively as a rectifier, the XCSR (from now on studied as a rectifier only) can be even further improved. As it can be seen for VSRs [4], [5], [12] and for CSRs [13], a reduction of the active switches count can increase the converter efficiency and reduce the costs. On the other hand it brings some limitations for the operation of the converter.

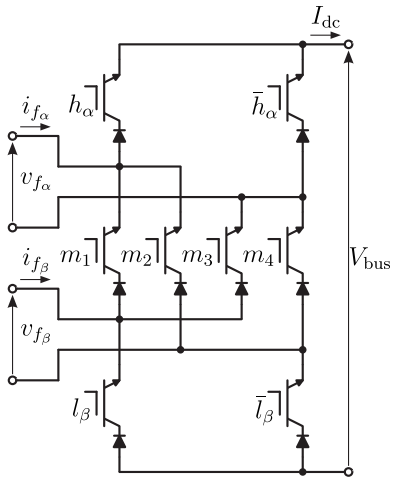


Fig. 2. Two-phase XCSR [14].

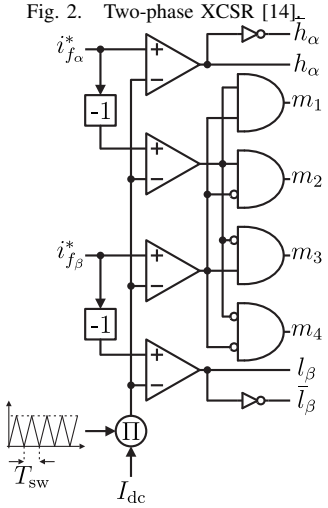


Fig. 3. PWM block diagram for the XCSR [14].

B. Asymmetric

The technique of doing active switch count reduction is an improvement that can easily be applied for the CSRs. As briefly presented in the last subsection, some papers have already shown the feasibility of this technique. However there are two important points: the replacement of the active switches by diodes demands synchronized input voltage and current waveforms [13]; and modifications of the converter PWM are needed (at least for the proposed topologies in this paper).

Using the strategy presented in [13] and using the PWM of the XCSC presented in [14], the PWMs for the asymmetric XCSCs can be achieved. It is worth to note that in this paper, the replacement of switches by diodes is made in an entire row, and it is alternated, such as shown in Fig. 4. This rule guarantees that there always will be a controlled row of semiconductors per phase, allowing both phases to be half-controlled. Different combinations, such as two diodes and two active switches in a single row, are not discussed in this paper.

Once having the active switches replaced by diodes, the

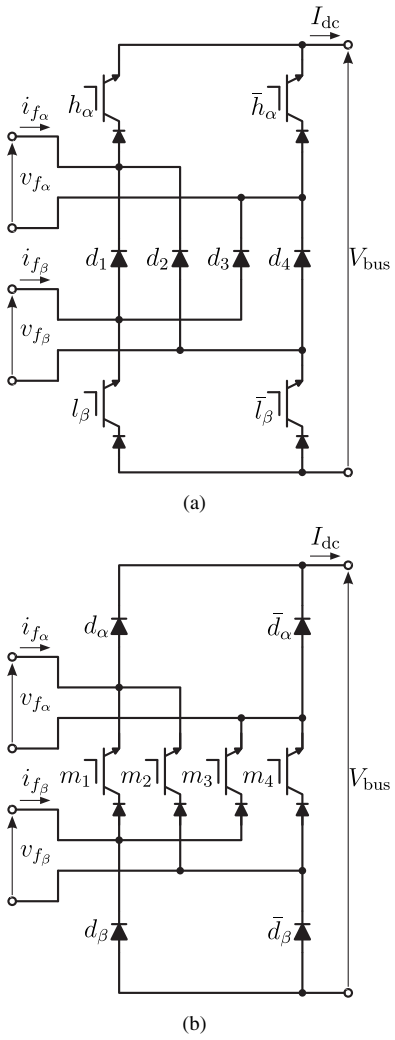


Fig. 4. Proposed two-phase crossed switches asymmetric CSRs topologies: (a) High/Low - HL-aXCSR; and (b) Middle - M-aXCSR.

PWM for the full-controlled XCSR will not work anymore for the new topologies. By using the theory presented in [13] for single-phase asymmetric CSRs, one can find the PWMs for the proposed topologies of this paper.

1) HL-aXCSR: In the HL-aXCSR, as shown in Fig. 4(a), the top and bottom switches are the active ones. In [13] it is shown that for the correct operation of the converter, there must be an alternating logic for the main and for the complementary switches.

The operation of HL-aXCSR is described as follows: for the input currents i_{f_α} and i_{f_β} during a switching cycle, one can find that

$$I_{f_\alpha} = (D_{h_\alpha} - (D_{d_1} + D_{d_2}))I_{\rm dc}, \tag{1}$$

$$I_{f_\beta} = ((D_{d_1} + D_{d_3}) - D_{l_\beta})I_{\rm dc}, \tag{2}$$

where $0 \leq D_{h_\alpha}, D_{l_\beta} \leq 1$ are the conduction times (duty cycle) of the respective switch, and $0 \leq D_{d_j} \leq 1$, being $j = 1, 2, 3, 4$, is the conduction time of the respective diode.

TABLE I

CONDUCTING DIODE FOR EACH INPUT VOLTAGE POLARITY OF THE HL-AXCSR

v_{f_α}	v_{f_β}	d_j
+	+	3
+	-	4
-	+	1
-	-	2

Since it is a CSC, there must always be a single conducting path per row, which can be written as

$$\sum_{j=1}^{4} D_{d_j} = 1. \tag{3}$$

Thus, knowing that

$$D_{f_\alpha} = \frac{I_{f_\alpha}}{I_{\rm dc}}, \tag{4}$$

$$D_{f_\beta} = \frac{I_{f_\beta}}{I_{\rm dc}}, \tag{5}$$

one can calculate the conduction time of the h_α and l_β switches. The conduction time of the diodes is indirect controlled by the active switches. It is worth to note that the polarity of the input voltages v_{f_α} and v_{f_β} will dictate which diode will conduct during each switching period. The conducting diodes of the HL-aXCSR based on the polarity of the input voltages are listed in Table I.

During the positive semi-cycle of the reference current, h_α and $\bar{l}_\beta$ must act as the main switch. Thus h_α and $\bar{l}_\beta$ must conduct during the calculated time in order to achieve the desired mean value of the current. The same logic is applied to $\bar{h}_\alpha$ and l_β during the negative semi-cycle of the reference current. Since the middle row is entirely composed of diodes, no gating actions are needed for this row.

The polarity of the reference current is used only to determine the main and the complementary switch. The conducting time is achieved by comparing the absolute value of the reference current with a high frequency triangular waveform (as shown in Fig. 5). In order to alternate the main and the complementary switch, an XOR logical gate is used.

The XOR will work as a logical inverting block, alternating the main and the complementary switch in each semi-cycle. The inputs of the XOR are: the conduction time; and a flag that indicates the polarity of the reference current (reference current compared with zero).

Since the outputs of the converter operate individually [14], the explained logic can be used for both reference currents $i^*_{f_\alpha}$ and $i^*_{f_\beta}$. However, it is worth to note that during the positive semi-cycle of the reference currents, both h_α and $\bar{l}_\beta$ will be the main switches. During the negative semi-cycle of the reference currents, both $\bar{h}_\alpha$ and l_β will be the main switches. This logic is resumed in Fig. 5. The possible states of the HL-aXCSR are listed in Table II, and States I to VIII are illustrated in Fig. 6.

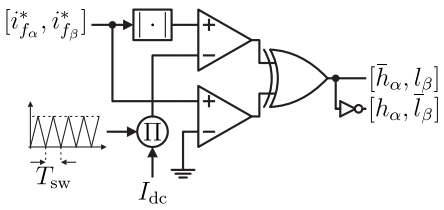


Fig. 5. PWM block diagram for the HL-aXCSR.

TABLE II
POSSIBLE STATES FOR THE HL-AXCSR

h_α	d_j	l_β	i_{f_α}	i_{f_β}	State
0	4	0	0	0	I
0	4	1	0	$-I_{\rm dc}$	II
0	3	0	0	$+I_{\rm dc}$	III
0	3	1	0	0	IV
0	2	0	$-I_{\rm dc}$	0	V
0	2	1	$-I_{\rm dc}$	$-I_{\rm dc}$	VI
0	1	0	$-I_{\rm dc}$	$+I_{\rm dc}$	VII
0	1	1	$-I_{\rm dc}$	0	VIII
1	4	0	$+I_{\rm dc}$	0	IX
1	4	1	$+I_{\rm dc}$	$-I_{\rm dc}$	X
1	3	0	$+I_{\rm dc}$	$+I_{\rm dc}$	XI
1	3	1	$+I_{\rm dc}$	0	XII
1	2	0	0	0	XIII
1	2	1	0	$-I_{\rm dc}$	XIV
1	1	0	0	$+I_{\rm dc}$	XV
1	1	1	0	0	XVI

2) M-aXCSR: The M-aXCSR (Fig. 4(b)) needs a combination of the PWM of the original CS-CSR [14] with the PWM of the HL-aXCSR. In the M-aXCSR there is no clear distinction of the middle switches l_α, $\bar{l}_\alpha$, h_β, and $\bar{h}_\beta$. Thus the logic for the middle switches of the original CS-CSR must be used.

The operation of the M-aXCSR is described as follows: for the input currents i_{f_α} and i_{f_β} during a switching cycle, one can find that

$$I_{f_\alpha} = (D_{d_\alpha} - (D_{m_1} + D_{m_2}))I_{\rm dc}, \tag{6}$$

$$I_{f_\beta} = ((D_{m_1} + D_{m_3}) - D_{d_\beta})I_{\rm dc}, \tag{7}$$

where $0 \leq D_\alpha, D_\beta \leq 1$ are the conduction times (duty cycle) of the respective diode, and $0 \leq D_{m_j} \leq 1$, being $j = 1, 2, 3, 4$, is the conducting time of the respective switch. Again, being a CSC, there must always be a single conducting path per row, so it can be written that

$$\sum_{j=1}^{4} D_{m_j} = 1. \tag{8}$$

Thus, knowing that

$$D_{f_\alpha} = \frac{I_{f_\alpha}}{I_{\rm dc}}, \tag{9}$$

$$D_{f_\beta} = \frac{I_{f_\beta}}{I_{\rm dc}}, \tag{10}$$

TABLE III
CONDUCTING DIODE FOR EACH INPUT VOLTAGES POLARITY OF THE M-AXCSR

v_{f_α}	v_{f_β}	Diode pair
+	+	$d_\alpha, \bar{d}_\beta$
+	-	d_α, d_β
-	+	$\bar{d}_\alpha, \bar{d}_\beta$
-	-	$\bar{d}_\alpha, d_\beta$

TABLE IV
POSSIBLE STATES FOR THE M-AXCSR

d_α	m_j	d_β	i_{f_α}	i_{f_β}	State
0	4	0	0	0	I
0	4	1	0	$-I_{\rm dc}$	II
0	3	0	0	$+I_{\rm dc}$	III
0	3	1	0	0	IV
0	2	0	$-I_{\rm dc}$	0	V
0	2	1	$-I_{\rm dc}$	$-I_{\rm dc}$	VI
0	1	0	$-I_{\rm dc}$	$+I_{\rm dc}$	VII
0	1	1	$-I_{\rm dc}$	0	VIII
1	4	0	$+I_{\rm dc}$	0	IX
1	4	1	$+I_{\rm dc}$	$-I_{\rm dc}$	X
1	3	0	$+I_{\rm dc}$	$+I_{\rm dc}$	XI
1	3	1	$+I_{\rm dc}$	0	XII
1	2	0	0	0	XIII
1	2	1	0	$-I_{\rm dc}$	XIV
1	1	0	0	$+I_{\rm dc}$	XV
1	1	1	0	0	XVI

one can calculate the conduction time of the m_j switch, having the conduction time of the diodes indirect controlled by the active switches. Again, it is worth to note that the polarity of the input voltages v_{f_α} and v_{f_β} will dictate which diode will conduct during each switching period. The conducting diodes of the M-aXCSR based on the polarity of the input voltages are listed in Table III.

In [14] it is shown for the two-phase series H bridge CSC that the bottom switches of the top converter, and the top switches of the bottom converter have their logical states rearranged in order to build the XCSC topology. Since the two rows of the middle are replaced by a single row, some new logics are used in order to correctly drive the middle switches. Since the top and bottom switches are replaced by diodes, no gating actions are needed for these rows.

Using an XOR logical gate presented for the HL-aXCSR, and the XCSC middle switches logic, one can achieve the PWM block diagram presented in Fig. 7. The possibles states of the M-aXCSR are listed in Table IV, and the States IX to XVI are illustrated in Fig. 8.

III. CONVERTER CONTROL

Despite presenting a reduced number of conducting and active switches, the new aXCSRs topologies must have synchronized input voltages and currents. Thus, a phase-locked loop (PLL) is used to achieve a power factor close to unity. In order to validate the CSRs topologies, a DC-bus current control is used. The complete system is composed of: two-phase AC voltage source, two-phase CSR, DC-bus, and a

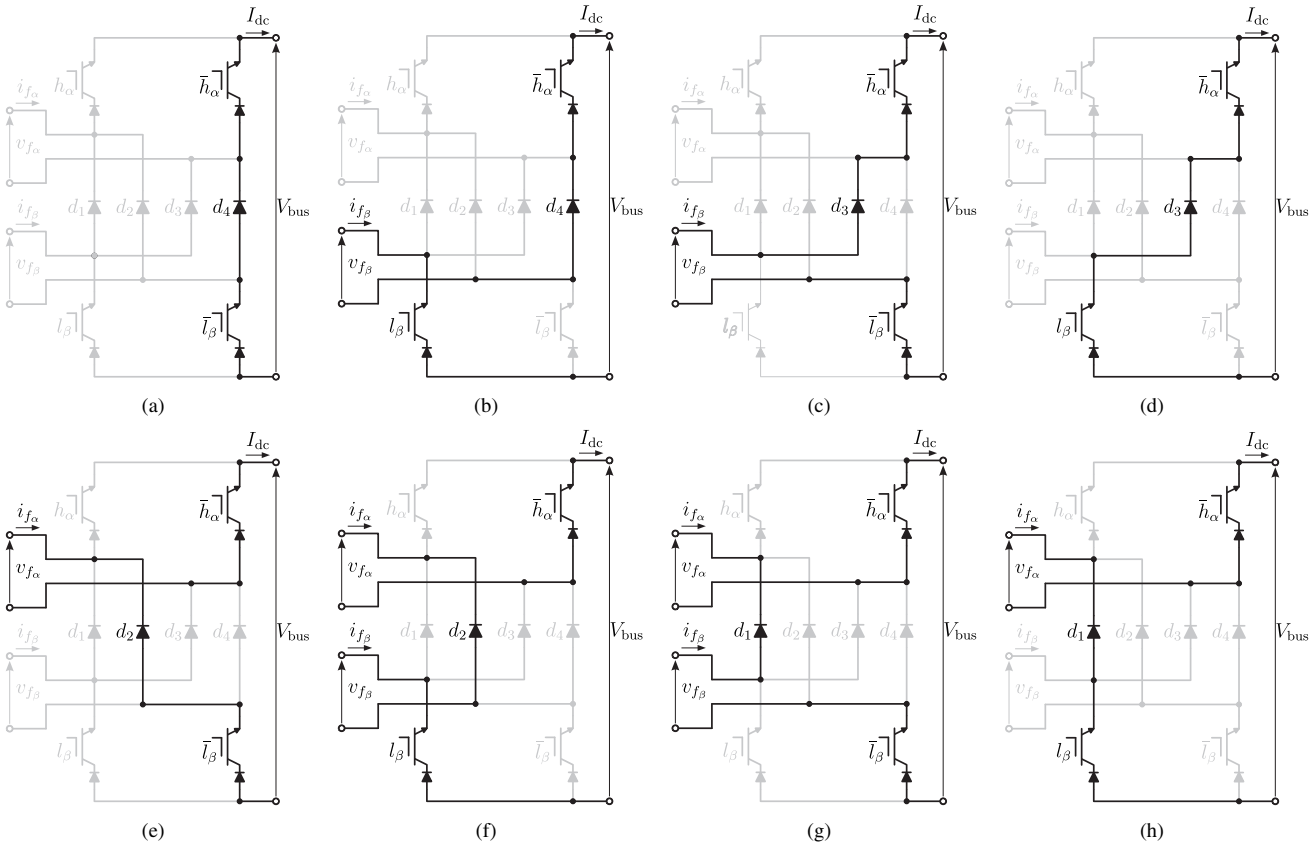


Fig. 6. Possible states for the HL-aXCSR (see Table II): (a) I; (b) II; (c) III; (d) IV; (e) V; (f) VI; (g) VII; (h) VIII.

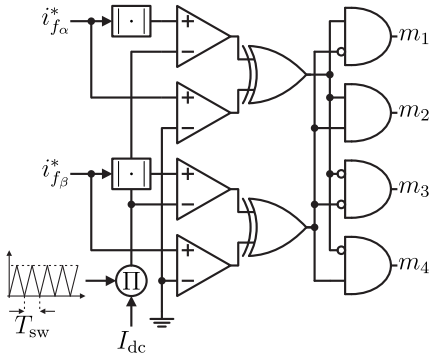


Fig. 7. PWM block diagram for the M-aXCSR.

resistive load. The complete system is shown in Fig. 9.

As presented in Fig. 9, the control strategy is responsible for generating the reference currents $i^*_{f_{\alpha,\beta}}$, aiming to control the DC-bus current $I_{\rm dc}$. The current $i^*_{f_{\alpha,\beta}}$ is synchronized with $v_{f_{\alpha,\beta}}$ using a PLL. It is worth to note that the AC voltages are delayed by $\pi/2$ radians. For the presented control, it is necessary to measure $I_{\rm dc}$ and $v_{f_{\alpha,\beta}}$. The PI controller is responsible to keep the DC-bus current $I_{\rm dc}$ controlled, which has to be large enough to obtain a correct operation of the converter. The PI controller generates the current $I^*_{f_{\alpha,\beta}}$ (peak value) that defines the absorbing power from the AC voltage source. Multiplying the reference peak value by the cosine generated by the PLL, one can find the sinusoidal reference currents $i^*_{f_{\alpha,\beta}}$, and thereby controlling the DC-bus to a reference value.

IV. Simulations and Experimental Results

Simulations and experimental results were taken in order to validate the presented theory for the asymmetric CSRs. The test scenario is shown in Fig. 9 and it uses a two-phase voltage source supplying a resistive load using the presented converters. Table V lists the power electronics component values: AC filter capacitor C_f; AC frequency $f_{\rm ac}$; switching frequency $f_{\rm sw}$; reference DC-bus current $I^*_{\rm dc}$; AC source internal inductance $L_{\rm ac}$; DC-bus inductance $L_{\rm dc}$; load power P_l; load resistance R_l; simulation time step T_s; AC source voltage $V_{\rm ac}$. Table VI lists the efficiency η, power factor (PF), total harmonic distortion (THD), switch (SW) and diode (DD) count.

The simulation results were taken using MATLAB®/Simulink®, using the SimPowerSystems™ library. The XCSC prototype it is shown in Fig. 10. The prototype was built using IGBTs IRG4PC40UPbF from International Rectifier®, in series with diodes RHRP1560 from Fairchild Semiconductors® in order to achieve the reverse blocking capability. The converter was controlled using a DSP TMS320F28335 from Texas Instruments®. The prototypes of the M- and HL-aXCSR were achieved by forcing the switches that would be replaced by diodes to the ON state.

The results presented in Fig. 11 show simulations and

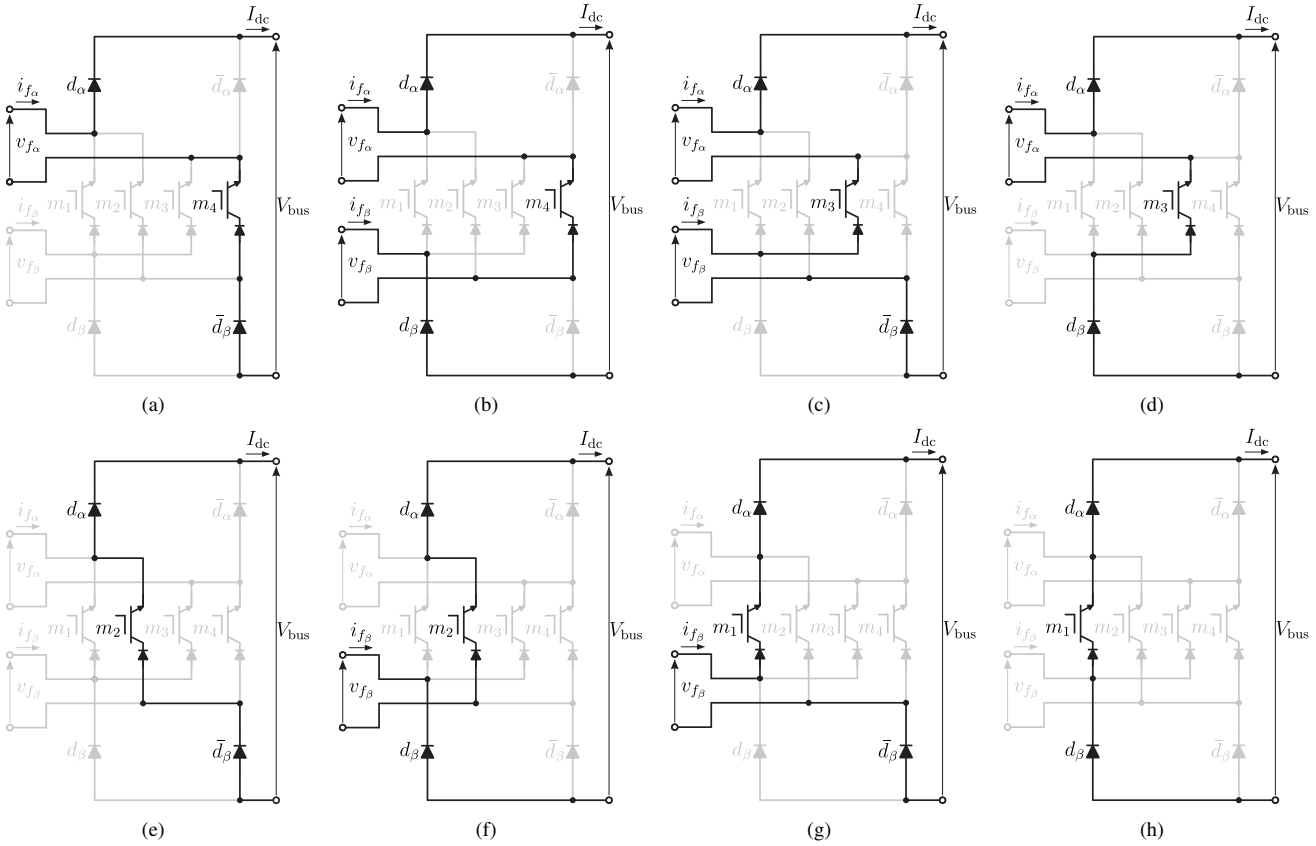


Fig. 8. Possible states for the M-aXCSR (see Table IV): (a) IX; (b) X; (c) XI; (d) XII; (e) XIII; (f) XIV; (g) XV; and (h) XVI.

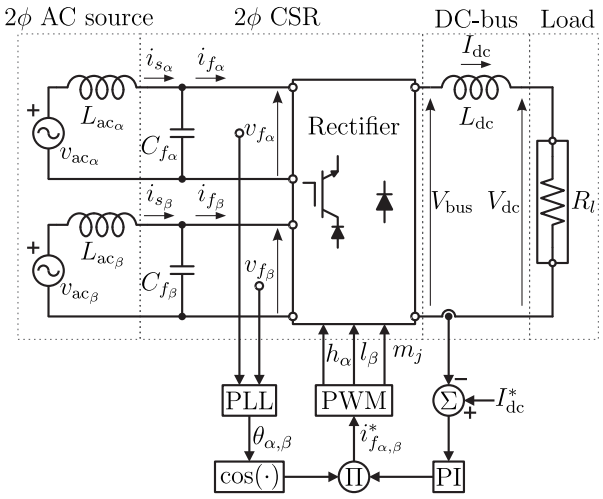


Fig. 9. Test setup with the two-phase AC Source, two-phase CSR, DC-bus, resistive load, and its control block diagram.

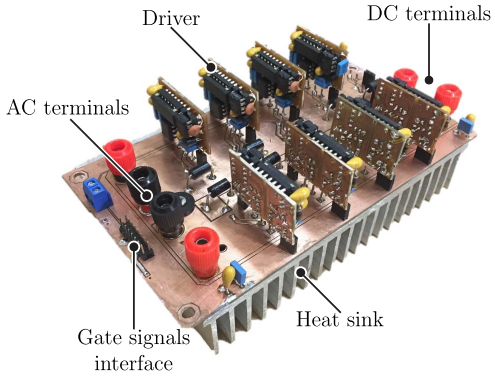


Fig. 10. X-Type Current Source Converter prototype detail.

experimental results, verifying that the rectifiers work properly. The input PFs are close to unity, which is the aimed operation point. The THDs of the input currents of all topologies are lower than 5%, and the DC-bus current is controlled in 4 A for all the converters.

The i_{s_α}, i_{s_β} vector plot figures are shown in Fig. 12. The vector plot figures show that the two currents are exactly delayed by $\pi/2$ radians, resulting in a circular figure. Since they are not ideal sinusoidal waves, the waveforms are not ideal circles either as expected.

Table VI lists the merits for the compared topologies. First of all, the proposed topologies (HL-aXCSR and M-aXCSR) have 4 active switches and 4 diodes, compared with 8 actives switches of the original XCSC. The efficiency of the asymmetric converters are higher than the XCSC. The THD of the M-aXCSR is the highest one, but this converter is, on the contrary, the most effective.

Both asymmetric topologies show higher efficiency than the XCSC. However, both half-controlled converters demonstrate a lower power factor, compared to the original XCSC. In respect to the THD, the HL-aXCSR has the lowest value, but

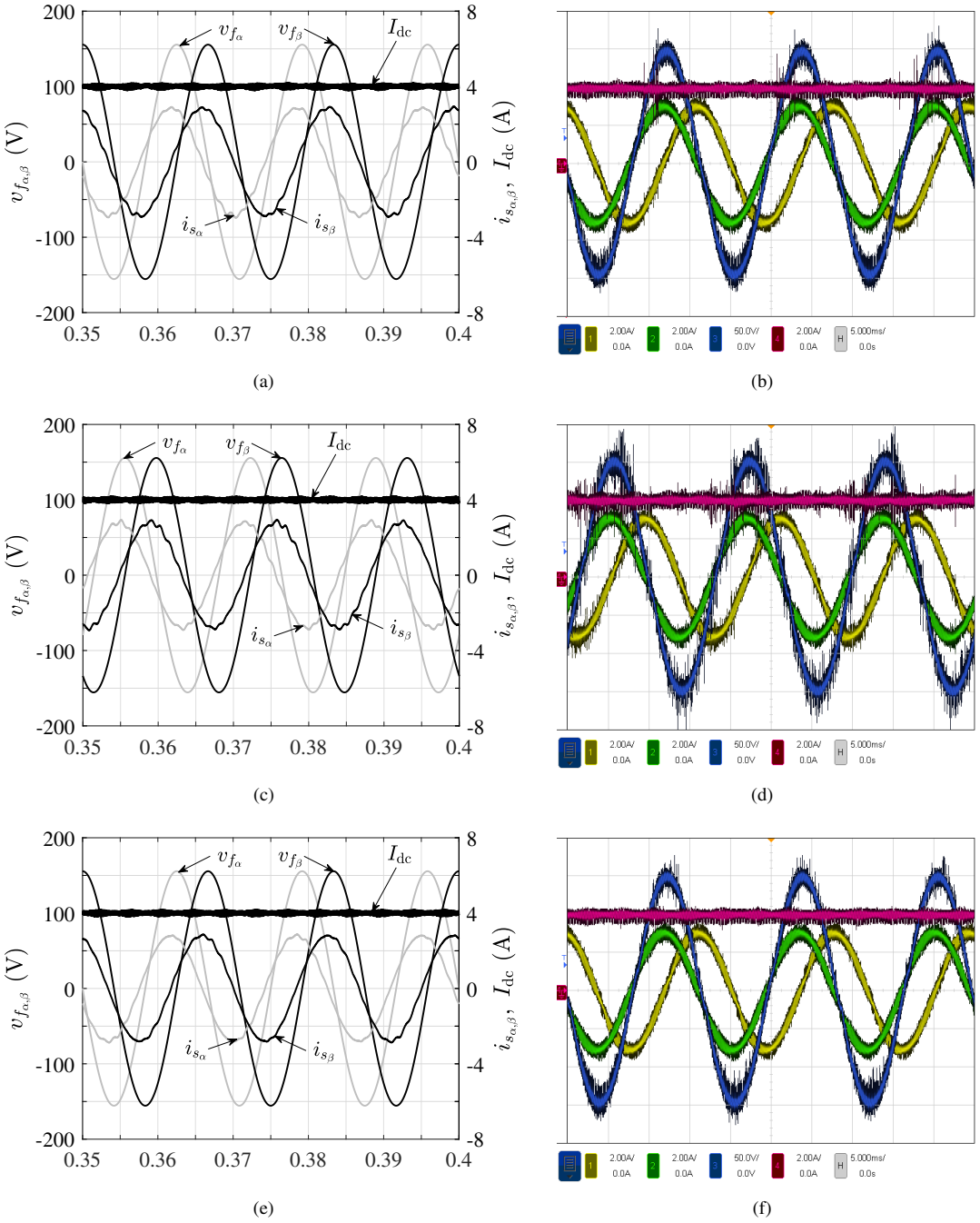


Fig. 11. Simulation (left) and experimental (right) results, where the x-axis is Time in seconds for the original XCSR: (a) and (b); M-aXCSR: (c) and (d); and HL-aXCSR: (e) and (f). Where CH1 (2 A/div): i_{s_α}, CH2 (2 A/div): i_{s_β}, CH3 (50 V/div): v_{f_α}, and CH4 (2 A/div): $I_{\rm dc}$.

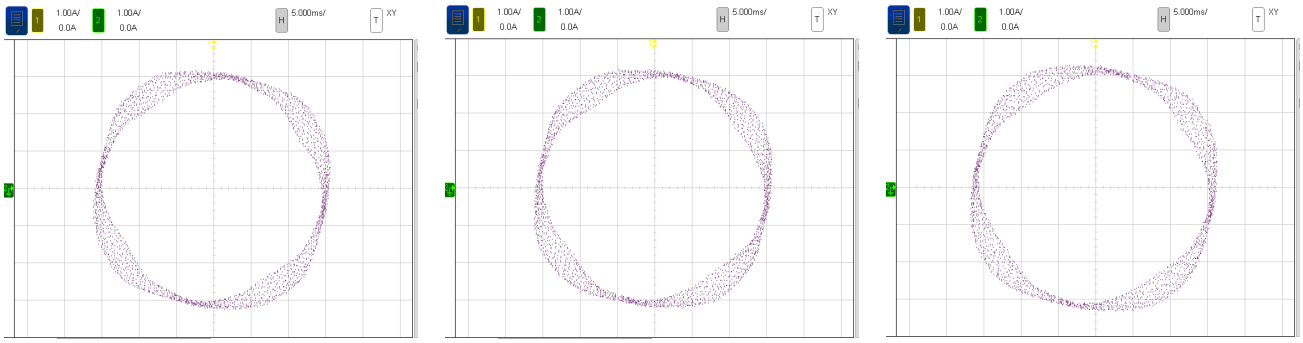
it shows also a good efficiency. Based on that, the HL-aXCSR is elected as the best converter in this paper.

Conclusion

Despite the large use of VSCs, the CSCs are viable solutions for future power electronics applications. Some technology advances and some inherent advantages of the CSCs compared to the VSCs, are bringing these two families of converters to a similar level of effectiveness. This paper has proposed two new topologies for two-phase open-end PMSG systems for low and medium power.

The asymmetric technique is an improvement of the originally bidirectional converters, as they are intended to be used only as rectifiers. Despite introducing some operational limitations to the rectifiers, the asymmetric technique improves the efficiency and reduces the costs. Even further for the CSCs, the replacement of an entire row of RBIGBTs by diodes is an improvement, mitigating one of the major disadvantages of these converters that is the conduction losses.

This paper has presented two new topologies of two-phase



(a) (b) (c)

Fig. 12. Measured vector plots: (a) original XCSR; (b) M-aXCSR; and (c) HL-aXCSR. Where CH1 (1 A/div): i_{s_α}, and CH2 (1 A/div): i_{s_β}.

TABLE V

SIMULATION AND EXPERIMENTAL PARAMETERS

Parameter	Value
C_f	15 μF
f_{ac}	60 Hz
f_{sw}	10 kHz
I^*_{dc}	4 A
L_{ac}	3 mH
L_{dc}	13 mH
P_l	400 W
R_l	25 Ω
T_s	2 μs
V_{ac}	110 Vrms

TABLE VI

SIMULATED TWO-PHASE CSRS COMPARATIVE DATA

Converter	η (%)	PF (%)	THD (%)	SW	DD
CS-CSR	93.77	96.05	2.92	8	0
M-aXCSR	95.86	95.73	3.04	4	4
HL-aXCSR	95.56	95.67	1.99	4	4

asymmetric CSRs, having the XCSC as basis. The adaptations for the PWM and a simple control diagram have been presented, and validated via simulation and experimental results. A deeper analysis was made using the simulation results, studying efficiency, power factor and THD. A comparative analysis has shown that the HL-aXCSR is the best topology studied in this paper, based on the relativity high efficiency and lowest THD.

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