Generalized Tri-state PWM Method Based High Frequency SiC Three-Phase Inverter

Junzhong Xu, Yong Wang*, Erlong Zhu, Khurram Hashmi, Xiaoyu Zha, Jingwen Han and Houjun Tang
School of Electronic Information and Electrical Engineering
Shanghai Jiao Tong University
Shanghai, China
*Email: wangyong75@sjtu.edu.cn

***Abstract*—In this paper, a generalized tri-state pulse width modulation method (GTSPWM), which decreases the common-mode voltage and current (CMV/CMC), is proposed for Silicon Carbide (SiC) based three-phase two-level voltage-source inverters (VSIs). Mathematical analysis, simulations, and experimental results show that GTSPWM has superior characteristics in terms of reduced switching losses, lesser output current harmonic distortion, reduced DC link current ripple, and lower common mode voltage (CMV). With the usage of SiC MOSFETs, the switching frequency of VSIs can be increased appreciably and the performance of proposed PWM method could be further improved.**

Keywords*—Silicon Carbide (SiC), generalized tri-state pulse width modulation (GTSPWM), common-mode voltage (CMV)

I. Introduction

With the development of power electronics, three-phase voltage source inverters (VSIs) are widely used in industry applications. Traditional VSIs based on Silicon (Si) devices are undergoing significant changes with the application of wide band gap semiconductor devices, such as silicon carbide (SiC), due to their higher switching speed capability and greater thermal conductivity. These characteristics improve the performance of VSIs remarkably. The efficiency of SiC three-phase inverter can be increased to 99% by using synchronous rectification [1]. SiC MOSFET devices enable a 50%−90% reduction in hard-switching losses, relative to Si devices [2]. With SiC devices, the sizes of the passive components and heat-sink can be distinctly reduced [3]. However, due to higher switching speed, the problem of high common-mode current (CMC) caused by excessive common-mode voltage (CMV) with sharp edges becomes especially serious [4].

Pulse width modulation (PWM) technique with fixed switching frequency is a standard approach to operate the VSIs that has been in use for many years. In recent years, various PWM methods have been investigated to reduce CMV such as active zero state PWM (AZSPWM1, AZSPWM2, and AZSPWM3), remote state PWM (RSPWM1, RSPWM2, and RSPWM3, and near-state PWM (NSPWM) [5], [6]. Such methods can reduce the peak value of CMV by adjusting the utilized vectors. However, the current ripple of these methods is large, especially at low modulation index M_i ($M_i = V_{1\mathrm{m}}/(2V_{\mathrm{dc}}/\pi)$, where V_{1m} is the magnitude of reference voltage). Moreover, the voltage linearity characteristics of RSPWM and NSPWM methods are limited [5]. Tri-state PWM (TSPWM) can reduce the CMV to one third of traditional SVPWM and DPWM methods, where the reference voltage vector has the high M_i. Whereas, with low M_i, TSPWM shows better output performance than other CMV reduction PWM (CMVRPWM) methods [7], [8]. However, there is a lack of systematic and conclusive investigation into waveform quality, switching losses, CMV characteristics and the comparison between TSPWM and CMVRPWM methods.

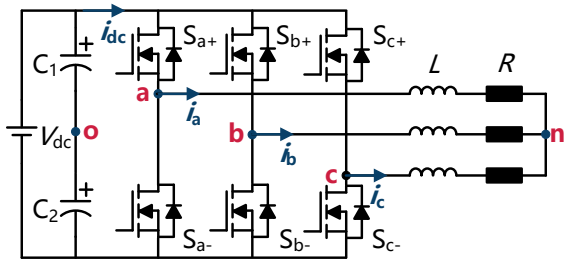


Fig. 1. Three-phase, two-level, and three-wire VSI.

In this paper, a high performance CMV reduction PWM method, named, generalized TSPWM (GTSPWM) method is proposed to maximize the performance of high-frequency SiC based three-phase, two-level inverters. Firstly, principles and switch logic signals of traditional CMVRPWM methods are reviewed. Thereafter, GTSPWM method is described through generalized scalar approach [9]. Then, the modulation characteristics are studied for comparison between GTSPWM and commonly-used PWM methods (SVPWM, DPWM1, and AZSPWM1) to show its superior. Finally, simulations and experimental results are presented to verify the capabilities and advantage of the proposed PWM method.

II. Review of Traditional CMVRPWM Methods

Fig. 1 shows a widely used three-phase, two-level SiC VSI. CMV of the inverter can be expressed as in (1) [6].

$$V_{\mathrm{no}} = \frac{V_{\mathrm{ao}} + V_{\mathrm{bo}} + V_{\mathrm{co}}}{3} \tag{1}$$

Where V_{ao}, V_{bo}, and V_{co} represent output phase to DC neutral point voltages and take the values of $\pm V_{\mathrm{dc}}/2$. With CMVRPWM methods, the maximum CMV is successfully reduced from $\pm V_{\mathrm{dc}}/2$ to $\pm V_{\mathrm{dc}}/6$ or the peak-to-peak value

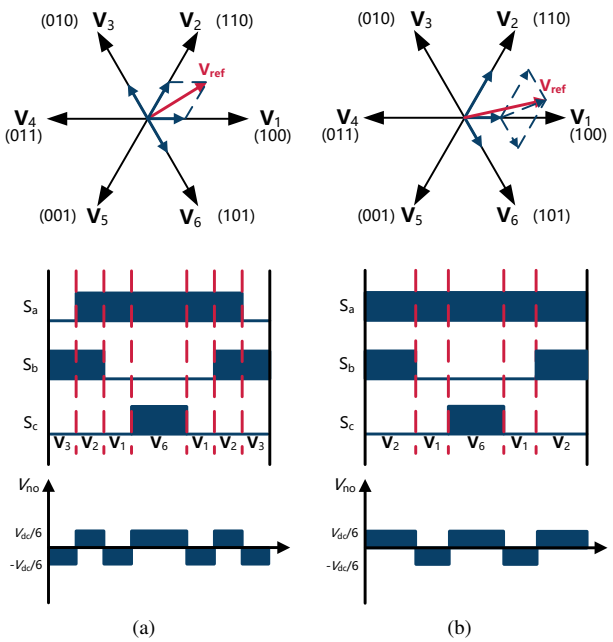


Fig. 2. Illustrations of various AZSPWM1 and NSPWM (a) AZSPWM1 (b) NSPWM.

of the CMV is reduced to $V_{\rm dc}/3$ in every switching period T_s relative to traditional space vector PWM (SVPWM) and discontinuous PWM (DPWM).

Except for AZSPWM1, NSPWM and TSPWM, all other CMVPWM methods have simultaneous inverter-leg switchings, which prohibits their practical application [5].

A. AZSPWM1

The AZSPWM1 methods utilize the same active vectors to construct the reference voltage vector as the SVPWM. Instead of zero vectors, two opposite active vectors with equal action time are used. The way that active vectors complemented with either two near opposing active vectors defines AZSPWM1. The simple illustration of AZSPWM1 is given in Fig. 2(a)

B. NSPWM

The NSPWM method [10] utilizes a group of three active voltage vectors to synthesize the desired reference voltage. These three active vectors are selected such that the inverter voltage vector closest to reference voltage vector and its two neighbors are utilized. A simplified illustration of NSPWM is given in Fig. 2(b).

III. The Working Principle of Proposed Method

Observing similarities between TSPWM, NSPWM, and DPWM [11], an attempt toward unifying them leads to the development of GTSPWM to maximize the performance of high-frequency operating SiC VSI. According to generalized scalar PWM approach [9], modulation waveforms $V_{\rm a}^{**}$, $V_{\rm b}^{**}$, and $V_{\rm c}^{**}$ of GTSPWM can be represented as in (2). Where V_0

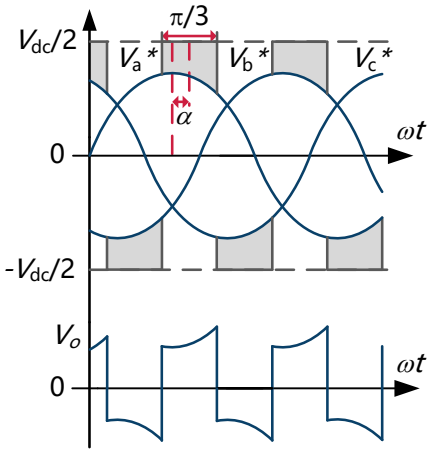


Fig. 3. GTSPWM zero-sequence signal generation method

is the zero sequence voltage added to the voltage references and $\omega t = \theta$ represents the angle of the reference voltage vector.

$$\begin{cases} V_{\rm a}^{**} = V_{\rm a}^{*} + V_0 = V_{1\rm m}\cos(\omega t) + V_0 \\ V_{\rm b}^{**} = V_{\rm b}^{*} + V_0 = V_{1\rm m}\cos(\omega t - 2\pi/3) + V_0 \\ V_{\rm c}^{**} = V_{\rm c}^{*} + V_0 = V_{1\rm m}\cos(\omega t + 2\pi/3) + V_0 \end{cases} \tag{2}$$

TABLE I
Choice of Sector-dependent Carrier Wave

	B_1	B_2	B_3	B_4	B_5	B_6
Phase a	V_{tri}	$-V_{tri}$	$-V_{tri}$	V_{tri}	V_{tri}	V_{tri}
Phase b	V_{tri}	V_{tri}	V_{tri}	$-V_{tri}$	$-V_{tri}$	V_{tri}
Phase c	$-V_{tri}$	V_{tri}	V_{tri}	V_{tri}	V_{tri}	$-V_{tri}$

Instead of single polarity carrier wave, two phase opposed triangular carriers $+V_{tri}$ and $-V_{tri}$ are utilized to produce gate pulses of the inverters [9]. The choice of the triangular carrier to be compared with the modulation waves is sector dependent as given in TABLE I. Via adjusting the clamped phase of modulation waves, GTSPWM method can realize the minimum switching loss characteristic under different load. To aid the description of GTSPWM and unify the expression of V_0, load power factor angle α is introduced, as shown in Fig. 3. All three reference modulation signals $V_{\rm a}^{*}$, $V_{\rm b}^{*}$ and $V_{\rm c}^{*}$ are phase shifted by α. The three new signals thus obtained: $V_{\rm a\alpha}^{*}$, $V_{\rm b\alpha}^{*}$ and $V_{\rm c\alpha}^{*}$ shown in (3) determining the zero sequence signaling as in (4), where the one with maximum magnitude among $V_{\rm a\alpha}^{*}$, $V_{\rm b\alpha}^{*}$ and $V_{\rm c\alpha}^{*}$ is first defined as $V_{\rm x\alpha}^{*}$ and $V_{\rm x}^{*}$.

$$\begin{cases} V_{\rm a\alpha}^{*} = V_{1\rm m}\cos(\omega t - \alpha) \\ V_{\rm b\alpha}^{*} = V_{1\rm m}\cos(\omega t - 2\pi/3 - \alpha) \\ V_{\rm c\alpha}^{*} = V_{1\rm m}\cos(\omega t + 2\pi/3 - \alpha) \end{cases} \tag{3}$$

$$V_0 = \text{sign}(V_{\rm x\alpha}^{*}) \cdot V_{\rm dc}/2 - V_{\rm x}^{*} \qquad x \in \{a, b, c\} \tag{4}$$

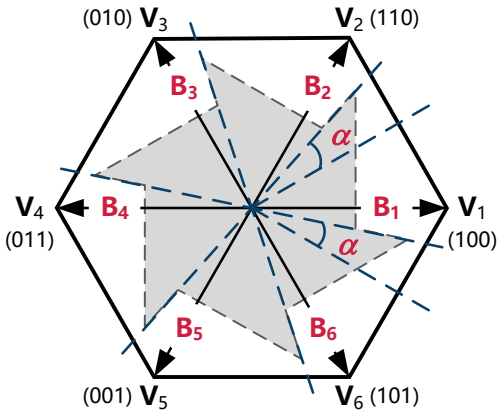


Fig. 4. Voltage vector plane of the proposed GTSPWM strategy.

Furthermore, the utilized space sectors should be rotated by α. The allocation of voltage vector plane is shown in Fig. 4. To keep the modulator linear, the range of α is confined to the interval $[-\pi/3, \pi/3]$. If load power factor angle is outside this range, α is limited at $-\pi/3$ or $\pi/3$.

IV. Comparison with Traditional PWM Methods

A. Switching Losses

Switching losses of VSI are load-current dependent and vary with the PWM method employed [11], [12]. Assuming a linear dependence of switching losses, per device switching losses, per fundamental cycle $P_{\rm sw}$ can be derived as follows:

$$P_{\rm sw} = \frac{V_{\rm dc} f_{\rm s}(t_{\rm on} + t_{\rm off})}{4\pi} \int_0^{2\pi} i_{\rm sa}(\omega t)\, {\rm d}\omega t \tag{5}$$

In (5), $t_{\rm on}$ and $t_{\rm off}$ can be approximately regarded as turn-on and turn-off time of the devices, $f_{\rm s}$ represents the switching frequency of the devices. $i_{\rm sa}(\omega t) = 0$ when the switching state of corresponding phase is clamped at "0" or "1" and $i_{\rm sa} = |i_{\rm a}(\omega t)|$ otherwise. Normalizing $P_{\rm sw}$ to $P_{\rm sw\_0}$ in (6), that is the switching loss of the Si VSI using SVPWM method under base frequency $f_{\rm s\_0}$. Switching loss function (SLF) of GTSPWM can be derived as shown in (7) and (8). Where $K_{\rm f} = f_{\rm s\_0}/f_{\rm s}$, and $K_{\rm s}$ is a coefficient whose value depends on device materials. Since switching losses in SiC devices reduced by at least 50% compared to conventional Si devices under same $f_{\rm s}$ [2], $K_{\rm s} = 1$ for Si IGBTs and 2 for SiC MOSFETs,

$$P_{\rm sw\_0} = \frac{V_{\rm dc} I_{\rm max} f_{\rm s\_0}}{\pi} \times (t_{\rm on\_Si} + t_{\rm off\_Si}) \tag{6}$$

$$SLF_{\rm GTPWM} = \frac{P_{\rm sw\_GTSPWM}}{P_{\rm sw\_0}} \tag{7}$$

$$= \begin{cases} \dfrac{1}{2K_{\rm s}K_{\rm f}} & |\varphi| \le \dfrac{\pi}{6} \\ \dfrac{2 + \sin(|\alpha| - \dfrac{2\pi}{3})}{2K_{\rm f}K_{\rm s}} & \dfrac{\pi}{6} \le |\varphi| \le \dfrac{\pi}{2} \end{cases} \tag{8}$$

SLF characteristics of various PWM methods are compared in Fig. 5. Since SVPWM and AZSPWM1 are continuous

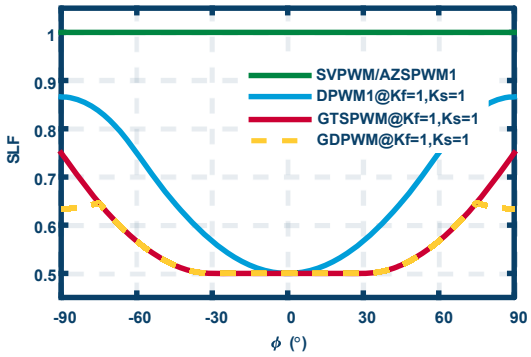


Fig. 5. SLF characteristics of different PWM methods.

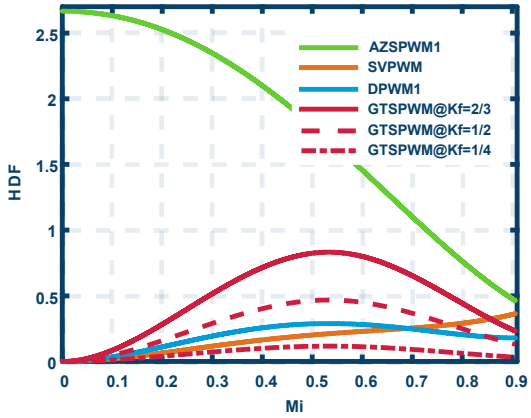


Fig. 6. HDF comparison between various PWM methods.

PWM methods, their SLF is same and independent of the φ. Different from GDPWM method in [12], outside the range of $-75° \le \varphi \le 75°$, DPWM3 can not be combined into proposed GTSPWM method. GTSPWM based SiC inverters can make less switching losses, which leads to a smaller heat sink and higher power density of the inverter.

B. Output Current Ripple

The performance of the inverter output current ripple can be studied theoretically through harmonic flux trajectories [5], [11]. The conceptual harmonic flux $\lambda_{\rm h}$ is defined to evaluate the performance of the output current ripple, because the phase harmonic current is proportional to $\lambda_{\rm h}$. $\lambda_{\rm h}$ investigated in terms of the time integral of the harmonic voltage vector in a N th PWM cycle $\lambda_{\rm hn}$ is shown as follows [11]:

$$\lambda_{\rm hn}(M_{\rm i}, \theta, V_{\rm dc}) = \frac{\pi}{V_{\rm dc} T_{\rm s}} \int_{(N-1)T_{\rm s}}^{NT_{\rm s}} (V_k - V_{\rm ref}) {\rm d}t \tag{9}$$

The RMS harmonic flux $\lambda_{\rm hn-rms}$ over a PWM cycle is given in (10), where d is duty cycle. Taken the switching losses into account, $K_{\rm f}$ is introduced in the calculation of harmonic

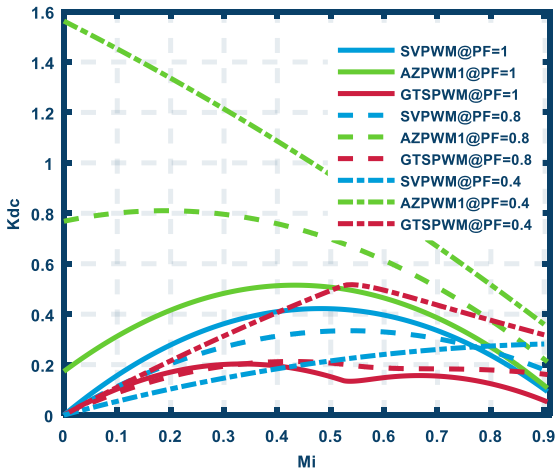


Fig. 7. KDF=$f(M_{\rm i})$ characteristics of different PWM methods under constant inverter switching losses and unit load power factor

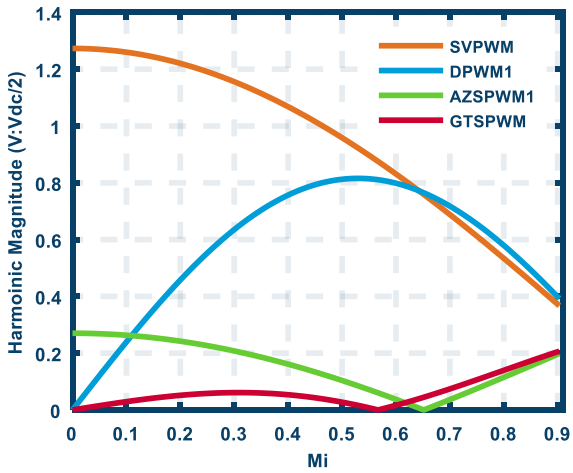


Fig. 8. Harmonic magnitude of different PWM methods @ $m=1$, $n=0$ for SVPWM and DPWM1, and $n=3$ for AZPWM1 and GTSPWM

distortion factor (HDF) normalized over a fundamental cycle as (11).

$$\lambda_{\rm hn-rms}(M_{\rm i},\theta)=\sqrt{\int_0^1 \lambda_{\rm hn}^2 {\rm d}d} \tag{10}$$

$$\text{HDF}=f(M_{\rm i})=K_{\rm f}^2\times\frac{288}{2\pi^3}\int_0^{2\pi}\lambda_{\rm hn}^2{\rm d}d \tag{11}$$

The HDF characteristics of GTSPWM and other common used PWM methods under unit load power factor are calculated in Fig. 6. It can be seen that GTSPWM is superior to AZPWM1 under equal switching number, where $K_{\rm f}=2/3$. In the SiC application, with same switching losses the value of $K_{\rm f}$ can take $1/4$ and the performance of GTSPWM method is better than SVPWM.

C. Input Current Ripple

The current RMS value $I_{\rm rms\_dc}$ of DC-link capacitor is important for DC-bus capacitor size design and is a function of M_i and α [13]. To compare this characteristic of the PWM methods, DC-link current coefficient $K_{\rm dc}$ is defined as (12) in [5], where RMS value of ac output fundamental component current $I_{\rm 1rms}$ is evaluated.

$$K_{\rm dc}=\frac{I_{\rm rms\_dc}^2}{I_{\rm 1rms}^2} \tag{12}$$

The $K_{\rm dc}$ factor for SVPWM and AZPWM1 are given as follows [11], [5]

$$K_{\rm dc}^{\rm SVPWM}=\frac{2\sqrt{3}}{\pi^2}M_i+(\frac{8\sqrt{3}}{\pi^2}-\frac{18}{\pi^2}M_i)M_i\cos^2\alpha \tag{13}$$

$$\begin{aligned}K_{\rm dc}^{\rm AZSPWM1}&=1+(\frac{9\sqrt{3}}{\pi^2}M_i-\frac{3\sqrt{3}}{\pi^2})\cos 2\alpha\\&\quad-\frac{18}{\pi^2}M_i^2\cos^2\alpha\end{aligned} \tag{14}$$

The calculations of $K_{\rm dc}$ for GTSPWM are performed numerically via computational software. In Fig. 7, $K_{\rm dc}=f(M_{\rm i})$ curves of SVPWM, AZPWM1 and GTSPWM are illustrated employing PF as a parameter. For a high PF of 0.8-1, common condition in the practice, $K_{\rm dc}$ of GTSPWM is lower than all other PWM methods. For a low PF of 0.4, $K_{\rm dc}$ of GTSPWM is inferior to SVPWM, but it is still superior to AZPWM1.

D. CMV

The CMV characteristics influence the inverter performance significantly in terms of high frequency behavior, leading to unavoidable common mode current. To determine the Influence of CMV on CMC, double Fourier integral analysis is applied to calculate the harmonic components of CMV for different PWM methods [14]. In general terms, the harmonic component of the switched phase leg output voltage under given carrier index variable m and baseband index variable n can be expressed as

$$C_{mn}=\frac{1}{2\pi^2}\sum_{i=0}^{6}\int_{y_s(i)}^{y_e(i)}\int_{x_r(i)}^{x_f(i)}2V_{\rm dc}e^{j(mx+ny)}{\rm d}x{\rm d}y \tag{15}$$

CMV can be expressed according to its harmonic components. Fig. 8 shows the maximum harmonic component of CMV around the $1st$ switching frequency where $m=1$, $n=0$ for SVPWM and DPWM1, and $n=3$ for AZPWM1 and GTSPWM. As illustrated in Fig. 8, GTSPWM and AZPWM1 are advantage over SVPWM and DPWM1. In the range of $0\le M_{\rm i}\le 0.61$, GTSPWM is lower than all other PWM techniques.

V. Simulation and Experimental Results

In order to verify the proposed GTSPWM method, PLECS based simulation model has been developed. The circuit used for the simulation is the same as the one given in Fig. 1. Three-phase Y connected R-L load is used, with 10 Ω and 10 mH value. The frequency of output voltage is 50 Hz. The DC-Link voltage is chosen to be 800 V. The DC-Link capacitance

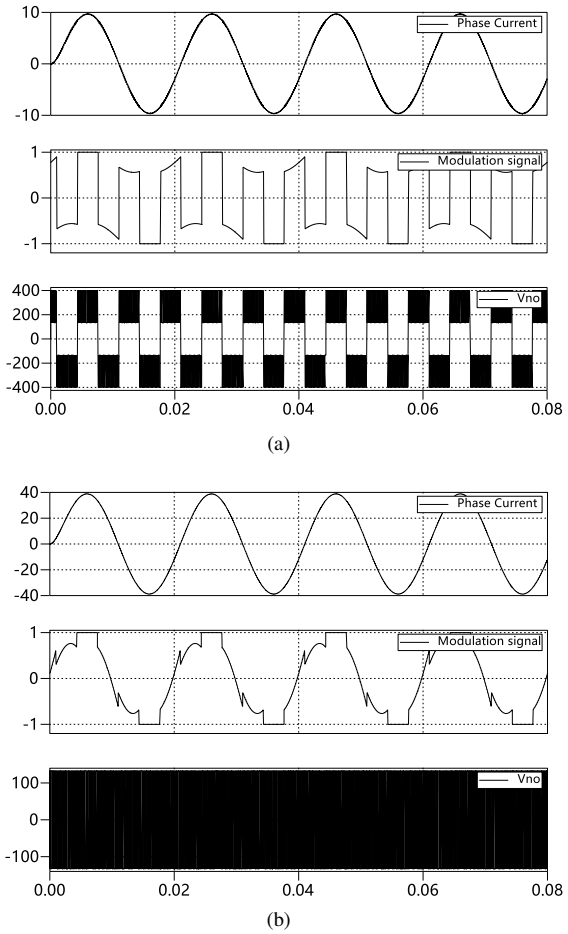


Fig. 9. Simulation waveforms for GTSPWM(a) $M_i = 0.2$ (b) $M_i = 0.8$.

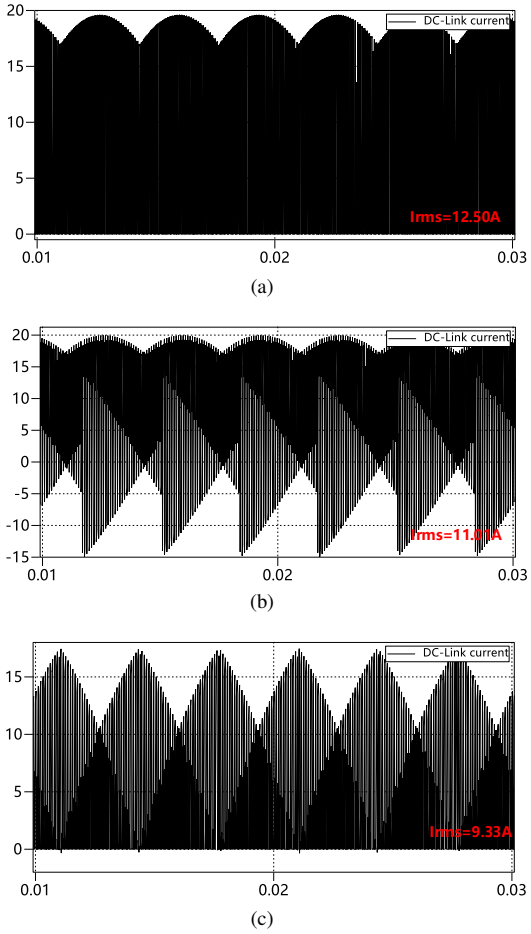


Fig. 10. DC-Link current waveforms for various PWM method when $M_i = 0.4$ (a) SVPWM (b) AZSPWM1 (c) GTSPWM.

is 470 μF. The switching frequency of simulation system is set low, 10 kHz, to improve the calculation accuracy.

Simulation waveforms of output phase current, modulation signal, and CMV for GTSPWM are shown in Fig. 9. With the adjusted modulation signals, the minimum switching losses action can be achieved. Meanwhile, CMV is reduced. The normalized harmonic component of CMV around the $1st$ switching frequency for $M_i = 0.2$ is 0.0625, and that for $M_i = 0.8$ is 0.1612, which accords with the previous analysis.

Fig. 10 shows the DC-Link current waveforms for various PWM methods. The rms value of the DC-Link current for GTSPWM is 9.33 A, which is lesser than others.

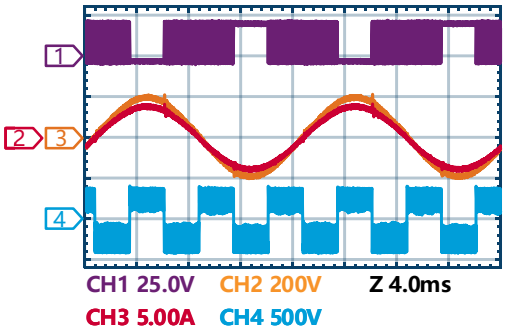
To ensure the feasibility of the proposed method, a 5 kW prototype of SiC-based inverter with LCL output filter is built. The inverter specifications are given in TABLE II.

Experimental results with GTSPWM with 100 kHz switching frequency under inductive load are shown in Fig. 11. Fig. 11(b) shows the CMV is successfully reduced to Vdc/6 and Fig. 11(a) shows that although the maximum value of CMV is Vdc/2, the peak-to-peak value of the CMV is reduced to Vdc/3 in every switching period. Furthermore, with the discontinuous switching action, switching losses reduces overall M_i.

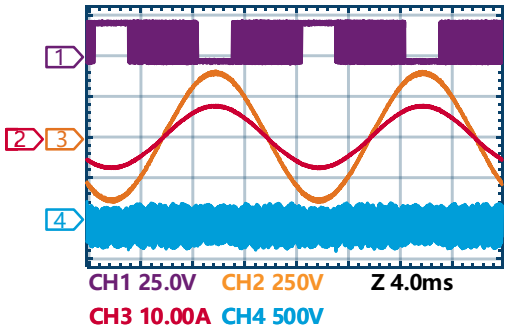
TABLE II
SPECIFICATIONS OF SIC VSI

Parameter	Value
DC-link voltage	800 V
DC capacitor	470 μF
Output frequency	50 Hz
Switching frequency	100 kHz
Inverter side inductor	262 μH
Load inductor	47 μH
Output capacitor	5μF
Load	54 Ω
SiC module	10-PZ126PA080MR-M909F28Y

Comparison of the total harmonic distortion (THD) in current is shown in Fig. 12. For a fair comparison, SVPWM and AZSPWM1 are operated at 40 kHz, while that of DPWM1 and GTSPWM is 60 kHz. For a low M_i, GTSPWM and AZSPWM1 have lower performance in terms of THD as compared to SVPWM and DPWM1 methods. However, the current THD of GTSPWM method is much smaller than that of AZSWPM1 methods. In the high M_i range, current THD



(a)



(b)

Fig. 11. Simulation waveforms for GTSPWM(a) $M_i = 0.2$ (b) $M_i = 0.8$.

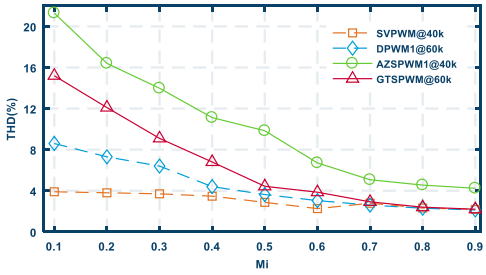


Fig. 12. Comparison results of current THD

.

of GTSPWM, DPWM1, and SVPWM are close.

As shown in Fig. 5, comparing with SVPWM working at 40 kHz, GTSPWM at 100 kHz achieves higher efficiency and better current THD by using SiC MOSFETs. The efficiency is measured by Voltech PM6000 power analyzer. Thus, GTSPWM shows its superiority relative to SVPWM in high frequency application.

VI. Conclusion

This paper has proposed a GTSPWM method for high-frequency three-phase two-level SiC VSIs. A simple scalar implementation of GTSPWM has been presented. Both analysis and experimental results verify that GTSPWM can achieve lower switching losses. Considering equivalent switching losses, GTSPWM shows better input and output current ripple characteristics than other CMVRPWM methods. Therefore, GTSPWM based SiC inverters can not only achieves higher

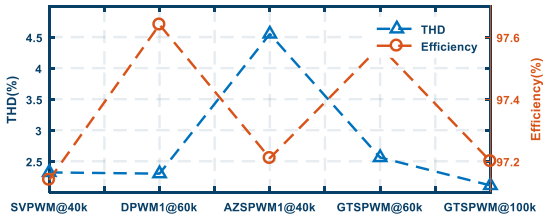


Fig. 13. Comparison results of current THD and efficiency for M_i= 0.8

.

efficiency and lower CMV/CMC under high-frequency switching, but also makes up for the shortcoming of large current ripples for other CMVRPWM methods.

References

[1] S. Yin, K. J. Tseng, C. F. Tong, R. Simanjorang, C. J. Gajanayake, and A. K. Gupta, "A 99% efficiency SiC three-phase inverter using synchronous rectification," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 2942–2949.

[2] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched All-Si, Si-SiC, and All-SiC device combinations," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2393–2407, May. 2014.

[3] C. Chen, Y. Chen, Y. Li, Z. Huang, T. Liu, and Y. Kang, "An sic-based half-bridge module with an improved hybrid packaging method for high power density applications," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8980–8991, Nov 2017.

[4] C. C. Hou, C. C. Shih, P. T. Cheng, and A. M. Hava, "Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1971–1979, Apr. 2013.

[5] A. M. Hava and E. n, "Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage-source inverters," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 241–252, Jan. 2009.

[6] H. Chen and H. Zhao, "Review on pulse-width modulation strategies for common-mode voltage reduction in three-phase voltage-source inverters," *IET Power Electronics*, vol. 9, no. 14, pp. 2611–2620, 2016.

[7] H. Lu, W. Qu, X. Cheng, Y. Fan, and X. Zhang, "A novel PWM technique with two-phase modulation," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2403–2409, Nov. 2007.

[8] H. Lu, X. Cheng, W. Qu, S. Sheng, Y. Li, and Z. Wang, "A three-phase current reconstruction technique using single dc current sensor based on TSPWM," *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1542–1550, Mar. 2014.

[9] A. M. Hava and N. O. etin, "A generalized scalar PWM approach with easy implementation features for three-phase, three-wire voltage-source inverters," *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1385–1395, May. 2011.

[10] E. Un and A. M. Hava, "A near-state PWM method with reduced switching losses and reduced common-mode voltage for three-phase voltage source inverters," *IEEE Transactions on Industry Applications*, vol. 45, no. 2, pp. 782–793, Mar. 2009.

[11] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *IEEE Transactions on Power Electronics*, vol. 14, no. 1, pp. 49–61, Jan. 1999.

[12] ——, "A high-performance generalized discontinuous PWM algorithm," *IEEE Transactions on Industry Applications*, vol. 34, no. 5, pp. 1059–1071, Sep. 1998.

[13] J. W. Kolar and S. D. Round, "Analytical calculation of the rms current stress on the dc-link capacitor of voltage-pwm converter systems," vol. 153, no. 4, pp. 535–543, 2006.

[14] D. G. Holmes and T. A. Lipo, *Modulation of ThreePhase Voltage Source Inverters*. Wiley-IEEE Press, 2003, pp. 215–258. [Online]. Available: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=5311949