Pulse-Width Modulation Scheme for a ZVS Single-Phase Inverter in Rectifier Operation

Yenan Chen
College of Electrical Engineering
Zhejiang University
Hangzhou, China
chenyenan@zju.edu.cn

Dehong Xu
College of Electrical Engineering
Zhejiang University
Hangzhou, China
xdh@zju.edu.cn

***Abstract*—This paper proposes a new pulse-width modulation scheme for a Zero-Voltage-Switching (ZVS) single-phase inverter to operate in rectifier mode. The ZVS single-phase inverter and its ZVS-SPWM modulation scheme is reviewed. The commutation in rectifier mode is analyzed to design the proper modulation scheme. ZVS turn-on of switching devices is achieved as well as the reverse recovery of body-diode is relieved with the new modulation in rectifier mode. The principle of ZVS rectifier operation is explained in detail and verified on a 100kHz ZVS single-phase inverter prototype. The modulation scheme of rectifier operation makes the ZVS single-phase inverter suitable for bidirectional power conversion applications such as energy storage system and vehicle-to-grid (V2G) chargers.**

Keywords—inverter; rectifier; zero voltage switching; pulse width modulation;

I. INTRODUCTION

With the increasing installation of distributed power generation systems, it is necessary to install battery energy storage systems to balance the power fluctuation in the grid [1]. For a battery energy storage system, bidirectional DC-AC converter is needed. It operates as an inverter when the power is transferred from DC energy source to the grid while it works as a rectifier when the battery is charged by the grid [2]. High power efficiency and high density are strongly demanded for this converter. However, the MOSFET devices with severe reverse recovery charge become the obstacle in the achievement of high frequency and efficient converters.

As a solution to reduce the commutation loss, soft-switching technique has been investigated by predecessors. For AC-DC conversion the bridgeless totem-pole PFC converter has lower conduction loss [3]. Zero-voltage switching can be realized with Triangular Current Mode (TCM) and the symmetrical topology of bridgeless totem-pole converter is also suitable for bidirectional operation [4]. In order to reduce the current ripple and input filter in critical mode, interleaved totem-pole converter is used [5], which will increase the cost and complexity. In a continuous conduction mode boost PFC converter, ZVS of all fast switches is achieved as well as the diode reverse recovery is relieved by employing an active clamping branch [5]. While the topology has higher conduction loss and can only operate with unidirectional power flow due to the diode rectifier bridge.

This work was supported by the National Natural Science Foundation of China (51337009).

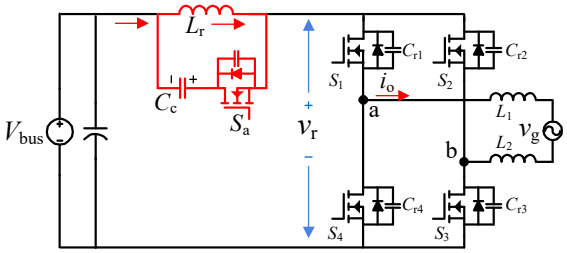

Fig. 1 ZVS single-phase inverter

For DC-AC stage a number of soft-switching inverters also has been proposed [6]-[10]. The resonant DC link concept is one of the most classical soft-switching technique [6][7]. With which the DC voltage of the switch bridge is oscillated to zero periodically. Zero switching losses is obtained by synchronizing switching transient to the zero-voltage state of the switch bridge. A ZVS single-phase inverter and the ZVS sinusoidal pulse-width modulation (ZVS-SPWM) is presented in [8] and the topology is shown in Fig. 1. In 90% of the duty cycle the ZVS single-phase inverter operate in SPWM mode and in the rest 10% of the duty cycle the DC side voltage of the switch bridge resonates with the auxiliary branch, providing ZVS condition for all switching devices. The auxiliary branch consisting of inductor L_r, capacitor C_c and MOSFET S_a has the capability of bidirectional power transmission, which makes the ZVS single-phase inverter a candidate of bidirectional DC-AC converter.

In this paper, the modulation scheme of the ZVS single-phase inverter for rectifier operation is designed after analyzing the commutation in rectifier mode. A group of unified equations is given to explain the resonant processes in both inverter mode and rectifier mode. The ZVS condition of rectifier mode is also derived and the theoretical analysis is verified on a 100kHz ZVS single-phase inverter prototype.

II. REVIEW OF ZVS SINGLE-PHASE INVERTER

The DC side voltage of switch bridge v_r in ZVS single-phase inverter is no longer a DC constant voltage. It is determined by the switching state of the auxiliary switch S_a. When S_a is conducting, the positive pole of switch bridge is directly connected to the clamping capacitor C_c and v_r is clamped to $V_{bus}+V_{cc}$, where V_{cc} is the voltage of clamping capacitor C_c. The

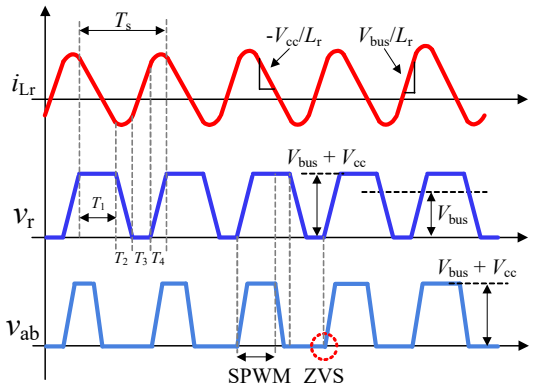

Fig. 2 Schematics of i_{Lr}, v_r and v_{ab} in inverter mode

resonant inductor current i_{Lr} is discharged by the clamping capacitor with the slope of $-V_{cc}/L_r$ at the same time. The clamping capacitor C_c is assumed to be large enough to ensure its voltage remaining unchanged in a switching cycle. The duration of high-voltage clamp is T_1, as shown in Fig. 2.

When the auxiliary switch S_a is in off state, the DC voltage source V_{bus}, the resonant inductor L_r and the resonant capacitors $C_{r1} \sim C_{r4}$ form a series resonant circuit. If the resonant inductor current i_{Lr} is negative enough, it is able to fully reset the charge in the resonant capacitors and the switch bridge voltage v_r is discharged to zero. The duration of discharging the switch bridge is T_2 in Fig. 2.

Then ZVS can be realized after the switch bridge voltage v_r is discharged to zero. All the switches in the switch bridge are also turned on by ZVS-SPWM to hold the switch bridge voltage v_r at zero for a certain duration T_3 to charged the resonant inductor. The charging slope is V_{bus}/L_r.

If the resonant inductor current i_{Lr} is charged to a sufficient positive level, it is able to charge the switch bridge voltage v_r back to $V_{bus}+V_{cc}$ and the charging time is T_4 in Fig .2.

The output voltage of switch bridge v_{ab} still shapes as an SPWM voltage, as shown in Fig. 2. The pulse width of v_{ab} is decided by SPWM strategy, which varies from 0 to mT_s. T_s is the switching period and m is the modulation ratio.

The simplified circuits of two typical hard-switching transients in inverter is presented in Fig. 3 and Fig. 4. Fig. 3 shows S_4 is turned off and its body-diode D_4 conducts for freewheeling the grid current i_o. When S_1 is turned on, the body-diode D_4 is forced to turn off with severe reverse recovery current, which causes high switching loss and stress. It is necessary to accomplish the body-diode's turn-off during zero-voltage state of switch bridge.

As shown in Fig. 4, S_1 is turned off and the output capacitance of MOSFET C_{oss1} is charged by the grid current i_o meanwhile C_{oss4} is discharged. Once the output capacitance C_{oss4} is discharged to zero, the body-diode D_4 conducts firstly and S_4 can realize ZVS turn-on if the dead-time is long enough.

The ZVS-SPWM for inverter mode in the positive half cycle ($v_g > 0$ and $i_o > 0$) is given in Fig. 5(a). The body-diode D_2 and D_4 will conduct for freewheeling and be forced to turn

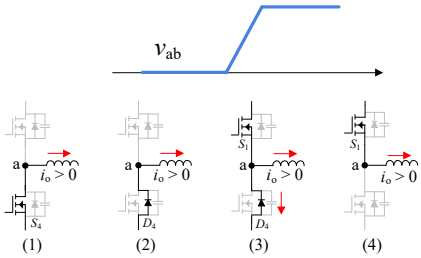

Fig. 3 Simplified switching waveform from body-diode to MOSFET in inverter mode

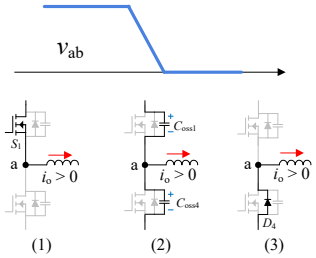

Fig. 4 Simplified switching waveform from MOSFET to body-diode in inverter mode

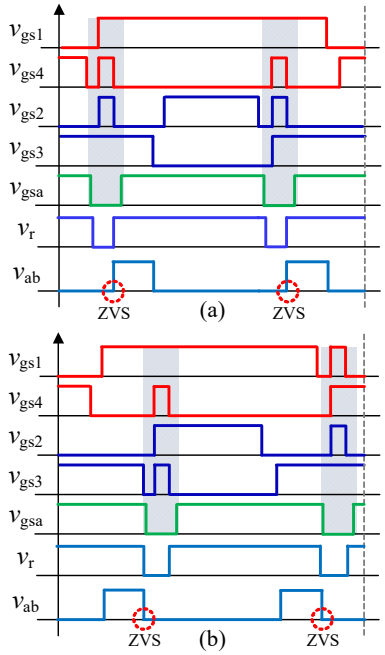

Fig. 5 ZVS-SPWM for (a) inverter mode (b) rectifier mode

off with reverse recovery when S_3 and S_1 are turned on. Therefore, the turn-on rising edge of gate-drive pulses v_{gs3} and v_{gs1} are synchronized to the zero-voltage state of the switch bridge v_r. Analogously, the the turn-on rising edge of gate-drive pulses v_{gs2} and v_{gs4} are synchronized to the zero-voltage state of the switch bridge in the negative half cycle ($v_g < 0$ and $i_o < 0$).

III. ZVS Modulation Scheme Design for Rectifier Operation

The key to design the ZVS modulation scheme in rectifier mode is to locate the body-diode's turn-off commutation in the

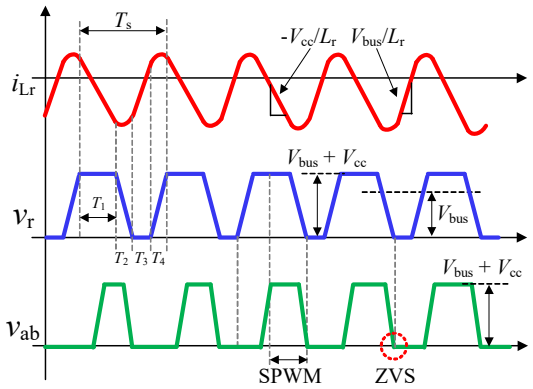

Fig. 6 Schematics of i_{Lr}, v_r and v_{ab} in rectifier mode

Table I SPECIFICATIONS OF THE ZVS SINGLE-PHASE INVERTER

V_{bus}	360V	T_s	10μs
V_g	230Vac/50Hz	C_{r1}~ C_{r4}	0.47nF
L_1 & L_2	190μH	L_r	7.2μH
C_{bus}	2.35mF	C_c	20μF

switching cycle. For rectifier mode in the positive half cycle ($v_g > 0$ and $i_o < 0$), the commutation from body-diode to MOSFET is D_3 to S_2 and D_1 to S_4. Therefore, the drive pulses of auxiliary switch v_{gsa} and short-circuit pulse v_{sc} are shifted to synchronize the turn-on rising edge of gate-drive pulses v_{gs2} and v_{gs4}, as shown in Fig. 5(b). Similarly the the drive pulses of auxiliary switch v_{gsa} and short-circuit pulse v_{sc} are synchronized to the turn-on rising edge of gate-drive pulses v_{gs1} and v_{gs3} in the negative half cycle ($v_g < 0$ and $i_o > 0$).

The schematics of resonant inductor current i_{Lr}, switch bridge voltage v_r and output voltage of switch bridge v_{ab} are illustrated in Fig. 6. The amplitude of i_{Lr} in rectifier mode is different from inverter mode because of the reverse power flow and the mathematical analysis is given in the next section. The falling edge of v_{ab} is synchronized to the zero-voltage state of switch bridge in rectifier mode.

The specifications and some parameters of the ZVS single-phase inverter are given in Table I. In rectifier mode the DC voltage source is replaced by resistance load. The drive sequences of rectifier mode in the positive half cycle ($v_g > 0$ and $i_o < 0$) are shown in Fig. 7. The pulses of SPWM v_{gs1} ~ v_{gs4} are generated by comparing the modulation waves v_{m1} and v_{m2} with the carrier wave v_{c1}. The drive pule of the auxiliary switch v_{gsa} is generated by delaying the falling edge of v_{gs3} and v_{gs1}. The short-circuit pulse v_{sc} is synchronized to the rising edge of gate-drive pulses v_{gs2} and v_{gs4}. The pulse width of v_{gsa} and v_{sc} are determined by the ZVS condition analyzed in the next section.

The filter inductors L_1 & L_2 are supposed to be large enough so the grid current i_o could be treated as constant when the DC voltage of switch bridge v_r is charging and discharging. The grid and the filter inductors L_1 & L_2 are replaced by the sinusoidal current source i_o. The switching devices are supposed to be ideal switches. The analysis is based on the steady operation state in the positive half cycle ($v_g > 0$ and $i_o < 0$). The operation circuits in one switching cycle are shown in Fig. 8.

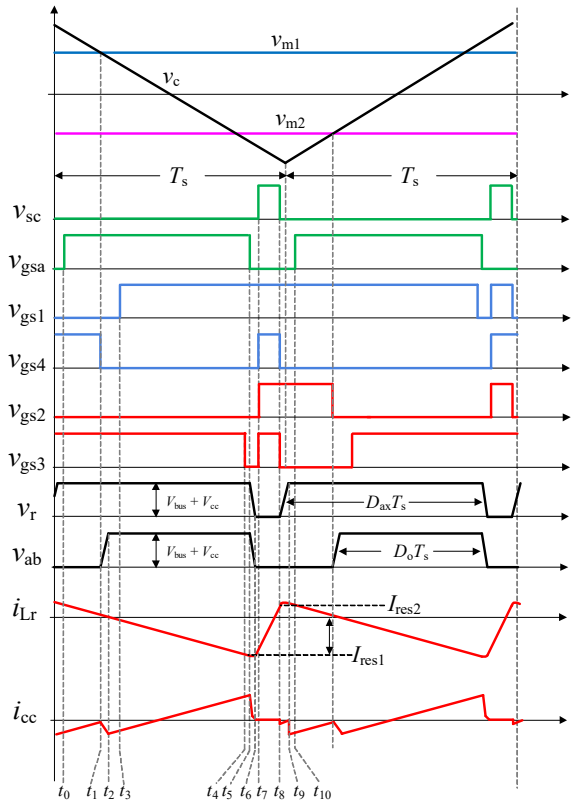

Fig. 7 Drive sequences and switching waveform of one switching cycle in rectifier mode

Stage 1 (t_0-t_1): the direction of grid current i_o is negative and freewheeling through S_3 and S_4. The auxiliary switch S_a is conducting and the resonant inductor current i_{Lr} is discharged with the slope of $-V_{cc}/L_r$.

Stage 2 (t_1-t_2): S_4 is turned off at t_1 by SPWM. The voltage of resonant capacitor C_{r4} is charged and the voltage of resonant capacitor C_{r1} is discharged by the grid current i_o. At t_2 the voltage of capacitor C_{r1} is discharged to zero.

Stage 3 (t_2-t_3): the body-diode D_1 of S_1 turns on at t_2. S_1 is ZVS turned on by SPWM at t_3. The duration of stage 2 and stage 3 (t_1~ t_3) is the dead-time of SPWM.

Stage 4 (t_3-t_4): the grid power is delivered to the DC load R through the switch bridge and the auxiliary resonant branch. The duration of stage 4 is determined by the SPWM strategy.

Stage 5 (t_4-t_5): S_3 is turned off at t_4 by SPWM and the grid current i_o is freewheeling in the body-diode D_3.

Stage 6 (t_5-t_6): the auxiliary switch S_a is turned off at t_5 by ZVS-SPWM. The resonant capacitors C_{r2} and C_{r4} are discharged while C_{ra} is charged by the resonant inductor L_r. The initial resonant current i_{Lr} at t_5 is defined as I_{res1}. Stage 6 ends when the voltage of capacitors C_{r2} and C_{r4} is discharged to zero at t_6.

Stage 7 (t_6-t_7): After the switch bridge voltage v_r resonates to zero at t_6, the body-diodes D_2 and D_4 turn on. The voltage of switch bridge is clamped to zero and the main switches S_2 can be ZVS turned on. The resonant inductor current i_{Lr} is charged with the slope of V_{bus}/L_r.

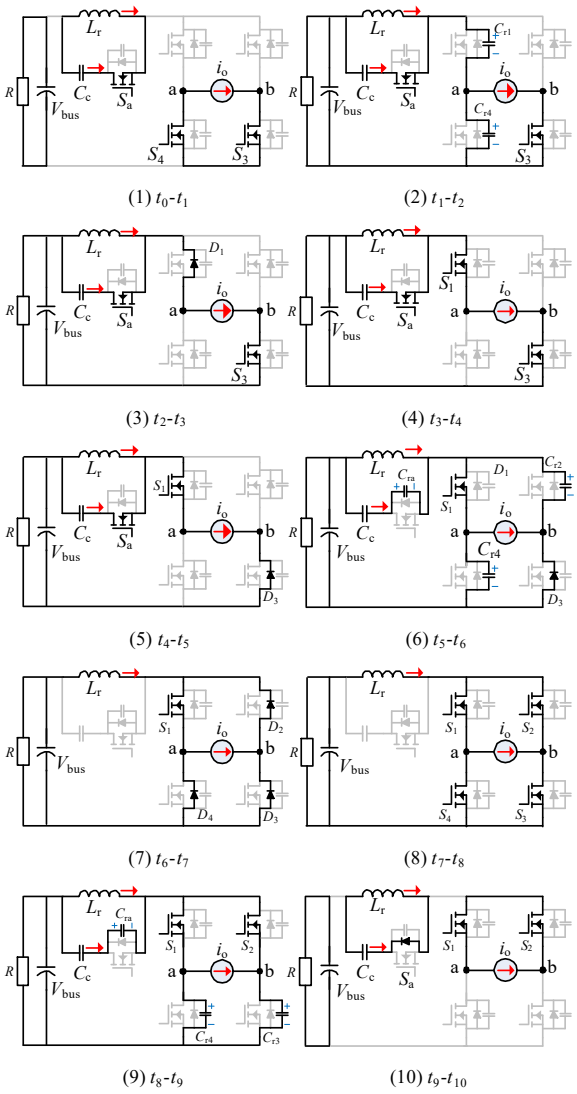

Fig. 8 Rectifier operation stages of one witching cycle, $i_o < 0$

Stage 8 (t_7-t_8): Main switches S_2, S_3 and S_4 are ZVS turned on by the short-circuit pulse v_{sc} at t_7, holding the switch bridge voltage v_r to zero to charge the resonant inductor current i_{Lr} from negative to positive. The body-diodes D_2, D_3 and D_4 are bypassed because of the low on resistance of MOSFET's drain-source channel and the reverse recovery is relieved. At t_8, the current i_{Lr} is charged to I_{res2}.

Stage 9 (t_8-t_9): At t_8, the short-circuit pulse v_{sc} is removed from all the main switches. S_1 and S_2 keep turning on by the high level drive pulse of SPWM. S_3 and S_4 are turned off without the short-circuit pulse v_{sc}. The resonant capacitors C_{r3} and C_{r4} are charged while C_{ra} is discharged by the resonant inductor current i_{Lr}. Stage 9 ends when the voltage of capacitor C_{ra} is discharged to zero at t_9.

Stage 10 (t_9-t_{10}): the body-diode D_a turns on at t_9 and the voltage of switch bridge v_r is charged back and clamped to V_{bus}+V_{cc}. At t_{10} S_a is ZVS turned on.

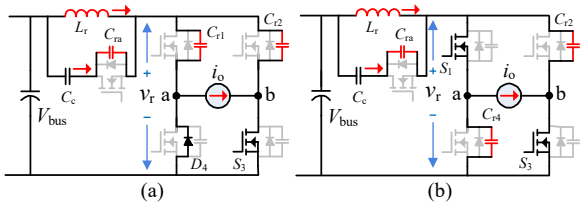

Fig. 9 Resonant circuits in inverter mode, $i_o > 0$ (a) v_r fall (b) v_r rise

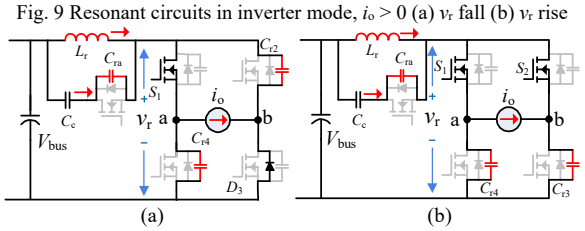

Fig. 10 Resonant circuits in rectifier mode, $i_o < 0$ (a) v_r fall (b) v_r rise

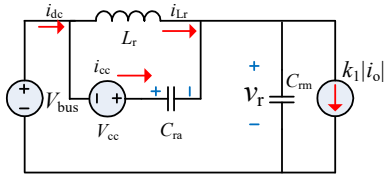

Fig. 11 Equivalent resonant model

Table II VALUE OF EQUIVALENT CONTROLLED CURRENT SOURCE

Mode	1st Resonance, v_r fall	2nd Resonance, v_r rise
Rectifier	$k_1 = -1$	$k_1 = 0$
Inverter	$k_1 = 0$	$k_1 = 1$

It can be concluded that stage 1 to 5 and stage 10 are the SPWM phases, which take up 90% of a switching cycle. Stage 6 to 9 are the resonant processes and short-circuit stage of the switch bridge, during which the grid power can not be transferred to the DC load.

IV. UNIFIED RESONANT EQUATIONS

The resonant circuits in inverter mode and rectifier mode are given in Fig. 9 and Fig. 10 respectively. The grid current i_o is positive in inverter mode and it only takes part in the resonant process of charging the switch bridge voltage v_r from zero to V_{bus}+V_{cc}, as shown in Fig. 9(b). On the contrary, the grid current i_o is negative in rectifier mode and it only takes part in the resonant process of discharging the switch bridge voltage v_r to zero, as shown in Fig. 10(a).

All the resonant circuits in Fig. 9 and Fig. 10 can be simplified to the equivalent circuit in Fig. 11. The DC bus capacitor and clamping capacitor C_c are replaced by the DC voltage source V_{bus} and V_{cc} considering their capacitance is large enough. C_{rm} represents the sum of two resonant capacitors paralleled with main switches. The value of equivalent controlled current source $k_1|i_o|$ depends on the operation mode, the value of k_1 is given in Table II.

The resonant processes and ZVS condition of inverter mode have been analyzed in [8]. In this paper the resonant equations are adapted for the situation in rectifier mode. Equation (1)

represents the first resonant process of discharging the switch bridge voltage v_r to zero in both inverter and rectifier mode:

$$\begin{cases} v_r(t) = V_{bus} - \sqrt{V_{cc}^2 + (k_1|i_o| - I_{res1})^2 Z_r^2}\sin(\omega t - \varphi_1) \\ i_{Lr}(t) = -\dfrac{1}{Z_r}\sqrt{V_{cc}^2 + (k_1|i_o| - I_{res1})^2 Z_r^2}\cos(\omega t - \varphi_1) + k_1|i_o| \end{cases} \quad (1)$$

$$\omega = \frac{1}{\sqrt{L_r(2C_{rm} + C_{ra})}},\ Z_r = \sqrt{\frac{L_r}{2C_{rm} + C_{ra}}},\ \varphi_1 = \tan^{-1}\left(\frac{V_{cc}}{(k_1|i_o| - I_{res1})Z_r}\right) \quad (2)$$

Equation (3) represents the second resonant process of charging the switch bridge voltage v_r back to V_{bus}+V_{cc} in both inverter and rectifier mode:

$$\begin{cases} v_{Cra}(t) = V_{cc} - \sqrt{V_{bus}^2 + (I_{res2} - k_1|i_o|)^2 Z_r^2}\sin(\omega t - \varphi_2) \\ i_{Lr}(t) = \dfrac{1}{Z_r}\sqrt{V_{bus}^2 + (I_{res2} - k_1|i_o|)^2 Z_r^2}\cos(\omega t - \varphi_2) + k_1|i_o| \\ \varphi_2 = \tan^{-1}\left(V_{bus}/\left((I_{res2} - k_1|i_o|)Z_r\right)\right) \end{cases} \quad (3)$$

Where v_{Cra} is the voltage of resonant capacitor C_{ra}. The minimum value of switch bridge voltage v_r in (1) and resonant capacitor voltage v_{Cra} in (2) should be smaller than zero to guarantee the ZVS condition. The required I_{res1} and I_{res2} in rectifier mode are derived to (4) and (5) according to the previous conditions. That means the resonant inductor current i_{Lr} should be charged to certain level at t_5 and t_8 to ensure the switch bridge voltage v_r can bounce between V_{bus}+V_{cc} and zero.

$$\begin{cases} 2D_o/D_{ax} \ge 1 \\ I_{res1\_rec} = -\sqrt{\left(\left(\dfrac{2D_o}{D_{ax}} - 1\right)|i_o| + \dfrac{V_{dc} - V_{cc}}{Z_r}\right)\left(\left(\dfrac{2D_o}{D_{ax}} - 1\right)|i_o| + \dfrac{V_{dc} + V_{cc}}{Z_r}\right)} - |i_o| \\ I_{res2\_rec} = 0 \end{cases} \quad (4)$$

$$\begin{cases} 2D_o/D_{ax} < 1 \\ I_{res1\_rec} = -|i_o| - \sqrt{V_{bus}^2 - V_{cc}^2}/Z_r \\ I_{res2\_rec} = \sqrt{|i_o|\cdot\left(\dfrac{2D_o}{D_{ax}} - 1\right)\left(|i_o|\cdot\left(\dfrac{2D_o}{D_{ax}} - 1\right) - \dfrac{2V_{dc}}{Z_r}\right)} \end{cases} \quad (5)$$

where D_{ax} is the duty ratio of the auxiliary switch S_a and D_o is the duty cycle of the SPWM, as shown in Fig. 7.

In the previous analysis the clamping capacitor C_c is supposed to be large enough, however the ampere-second balance of C_c should also be satisfied in practice. Therefore, the switching cycle average current of C_c (i_{cc}) is zero. Obviously, the DC side current i_{dc} equals to the sum of i_{cc} and i_{Lr} in Fig. 11. Their relationship can be obtained in (6):

$$\int_{t_0}^{t_{10}} i_{dc}dt = \int_{t_0}^{t_{10}} i_{Lr}dt \quad (6)$$

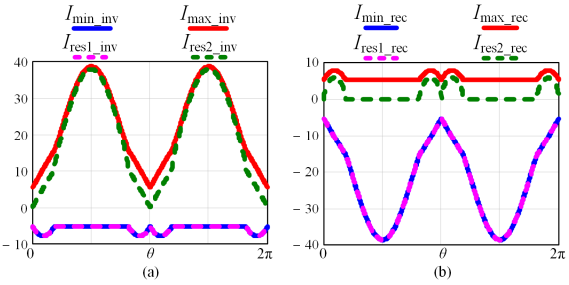

Fig. 12 ZVS condition: initial resonant inductor current and peak resonant inductor current in (a) inverter mode (b) rectifier mode with 3kW power

The DC side current i_{dc} equals to the resonant inductor current i_{Lr} when the switch bridge is short-circuited (t_6-t_8), so equation (6) can be simplified to (7):

$$\int_{t_0}^{t_6} i_{dc}dt + \int_{t_8}^{t_{10}} i_{dc}dt = \int_{t_0}^{t_6} i_{Lr}dt + \int_{t_8}^{t_{10}} i_{Lr}dt \quad (7)$$

The DC side current i_{dc} equals to zero when the grid current i_o is freewheeling from t_0 to t_1 and t_9 to t_{10}, while it equals to i_o from t_1 to t_6. Therefore the left part of (7) is adapted to (8):

$$\int_{t_0}^{t_6} i_{dc}dt + \int_{t_8}^{t_{10}} i_{dc}dt = \int_{t_1}^{t_6} -|i_o|dt = -D_o T_s|i_o| \quad (8)$$

If the resonant inductor current i_{Lr} changes a little during the resonant processes, it can be approximately regarded as a triangular wave with the peak amplitude of I_{max} and I_{min}. Then the right part of (7) can be changed to (9):

$$\int_{t_0}^{t_6} i_{Lr}dt + \int_{t_8}^{t_{10}} i_{Lr}dt = D_{ax}T_s(I_{max} + I_{min})/2 \quad (9)$$

Then the relationship between resonant inductor current i_{Lr} and grid current i_o is derivated:

$$(I_{max} + I_{min})/2 = k_2|i_o|D_o/D_{ax} \quad (10)$$

k_2 is -1 in rectifier mode and 1 in inverter mode. The expressions of the peak amplitude of i_{Lr} in rectifier mode and inverter mode are given in (11) and (12) respectively. Obviously, they are antithetic:

$$\begin{aligned} i_{min\_rec} &= -i_{max\_inv} \\ i_{max\_rec} &= -i_{min\_inv} \end{aligned} \quad (13)$$

I_{res1}, I_{res2}, I_{max} and I_{min} with 3kW output power are plotted in Fig. 12. The difference between the initial value and the peak value (I_{max}-I_{res1}, I_{min}-I_{res1}) during the resonant processes is small. The polarity of resonant inductor current i_{Lr} is opposite between inverter mode and rectifier mode while the amplitude is almost equal. It can be concluded that the amplitude of resonant

$$i_{min\_rec} = \begin{cases} -V_{bus}/Z_r - 2|i_o|D_o/D_{ax}, & 2D_o/D_{ax} \ge 1 \\ -V_{bus}/Z_r - |i_o|, & 2D_o/D_{ax} < 1 \end{cases}, \quad i_{max\_rec} = \begin{cases} V_{bus}/Z_r, & 2D_o/D_{ax} \ge 1 \\ V_{bus}/Z_r + |i_o|\cdot(1 - 2D_o/D_{ax}), & 2D_o/D_{ax} < 1 \end{cases} \quad (11)$$

$$i_{min\_inv} = \begin{cases} -V_{bus}/Z_r, & 2D_o/D_{ax} \ge 1 \\ -V_{bus}/Z_r - |i_o|\cdot(1 - 2D_o/D_{ax}), & 2D_o/D_{ax} < 1 \end{cases}, \quad i_{max\_inv} = \begin{cases} V_{bus}/Z_r + 2|i_o|D_o/D_{ax}, & 2D_o/D_{ax} \ge 1 \\ V_{bus}/Z_r + |i_o|, & 2D_o/D_{ax} < 1 \end{cases} \quad (12)$$

inductor current i_{Lr} is determined by the ZVS condition while its average value is mainly decided by the grid current i_o.

According to (11), the time sequence of ZVS-SPWM in Fig. 7 can be designed by (14) and (15):

$$t_9 - t_5 \approx L_r\left(I_{max} - I_{min}\right)/V_{bus} \tag{14}$$

$$t_5 - t_0 + t_{10} - t_9 \approx L_r\left(I_{max} - I_{min}\right)/V_{cc} \tag{15}$$

V. Loss Analysis

The specifications of semiconductor and passive components are given in Table III for loss evaluation. The losses of ZVS single-phase inverter include nine parts: conducting loss of main switches P_{cm}, turn-off loss of main switches P_{offm}, conducting loss of auxiliary switch P_{ca}, turn-off loss of auxiliary switch P_{offa}, core loss of resonant inductor P_{Lr_Fe}, winding loss of resonant inductor P_{Lr_Cu}, ESR loss of resonant capacitors P_{esr}, core loss of filter inductors P_{L12_Fe} and winding loss P_{L12_Cu}.

The loss evaluation in rectifier mode is presented in Fig. 13. The maximum part of loss are the conducting losss of MOSFETs (P_{cm}, P_{ca}). The turn-on losses are eliminated with ZVS and the turn-off losses (P_{offm}, P_{offa}) are reduced less than 0.05% of total power due to the nonlinear output capacitance of super-junction MOSFET [11]. While the trade-off is the additional losses of auxiliary switch, resonant inductor and capacitors (P_{Lr_Fe}, P_{Lr_Cu} and P_{esr}). The efficiency evaluation at rated 3kW power is 98.4%. It can be found from Fig. 13 that the losses of auxiliary switch and resonant inductor (P_{ca}, P_{Lr_Fe} and P_{Lr_Cu}) take higher percentage with smaller power. The reason is that the amplitude of i_{Lr} is not proportional to the grid current i_o and "V_{bus}/Z_r" in (11) will not change with smaller power.

Table III Specificaions of Semiconductor and Passive Components

MOSFETs	FCH47N60F
Filter Inductors	super sendust toroid core 46.7/24.1/18mm AWG 12 wire×2P
Resonant Inductor	ferrite PQ32-30 Litz wire 0.05mm×1300×2P
Resonant Capacitors	MKP film capacitor

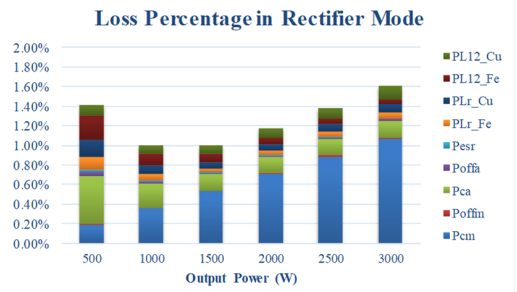

Fig. 13 Loss percentage of total output power in rectifier mode

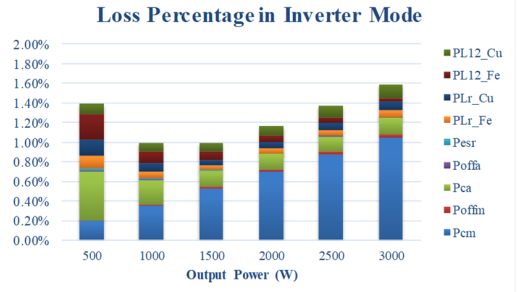

Fig. 14 Loss percentage of total output power in inverter mode

The loss distribution in inverter mode is illustrated in Fig. 14. The conducting loss of MOSFETs in both rectifier mode and inverter mode are same because of the reverse conducting capability of MOSFETs, which is different from IGBTs. The symmetrical resonant inductor currents in both modes also make the same magnetic loss. The difference between inverter and rectifier mode is that the turn-off loss of auxiliary switch P_{offa} is higher in rectifier mode. The turn-off current of S_a at t_5 in rectifier mode is $-I_{res1\_rec}$-$|i_o|$ while the turn-off current of S_a in inverter mode is $-I_{res1\_inv}$. As shown in Fig. 12, $-I_{res1\_rec}$-$|i_o|$ is much higher than $-I_{res1\_inv}$. Nevertheless, the percentage of P_{offa} is less than 0.046% in rectifier mode and less than 0.014% in inverter mode according to the loss evaluation, which is a small part of the total loss.

VI. Experimental Results

The control diagram of rectifier operation is shown in Fig. 15. The reference of DC bus voltage v_{bus_ref} is 360V and the output of controller PI2 is the reference of grid current i_{o_ref}. The DC bus voltage is charged to 325V firstly by a precharging circuit, which is not shown in Fig. 15.

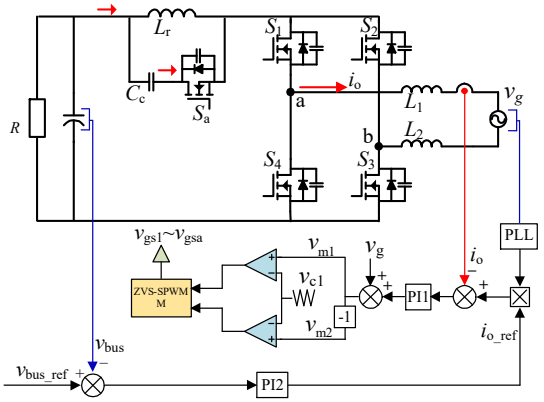

Fig. 15 Control diagram of rectifier operation

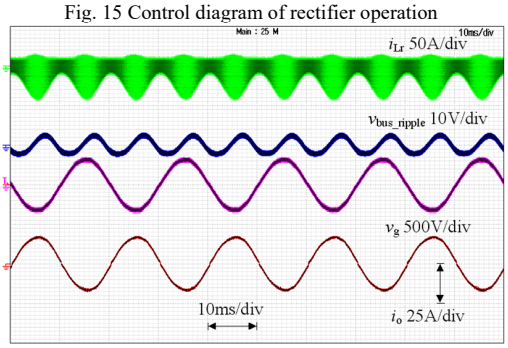

Fig. 16 Grid current i_o, resonant inductor current i_{Lr} and bus ripple voltage in rectifier mode, Po = 3kW

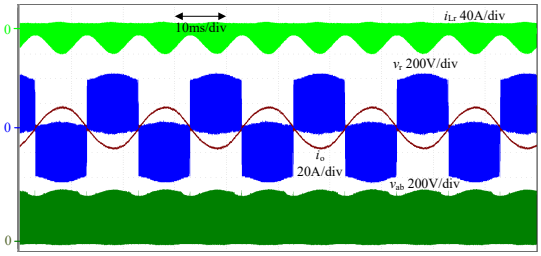

Fig. 17 The DC side voltage of switch bridge v_r, output voltage of switch bridge v_{ab}, resonant inductor current i_{Lr} and grid current i_o

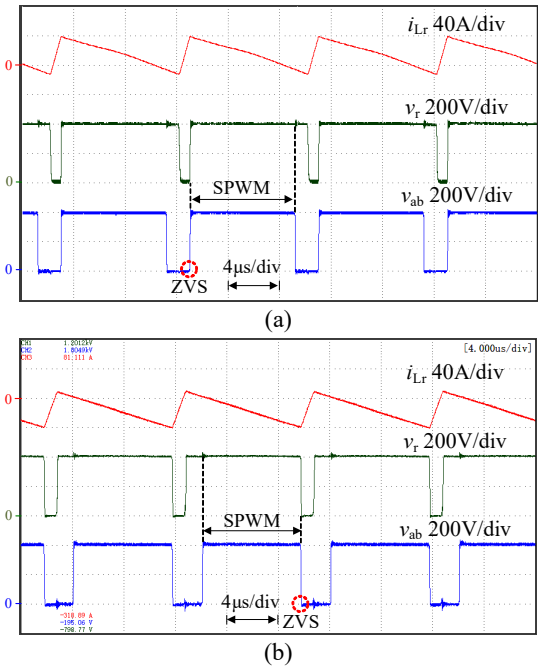

Fig. 18 The DC side voltage of switch bridge v_r, output voltage of switch bridge v_{ab} and resonant inductor current i_{Lr} in (a) inverter mode (b) rectifier mode, $P_o = 3\text{kW}$, $\theta = \pi/2$

Fig. 16 shows the grid current i_o, DC bus voltage ripple v_{bus_ripple} and resonant inductor current i_{Lr} in rectifier mode. The polarity of grid current i_o is opposite to the grid voltage v_g. The envelope curve of resonant inductor current i_{Lr} matches the mathematical calculation results in Fig. 12(b). The DC bus voltage is stable with 100Hz ripple, which is same with the grid AC power fluctuation.

Fig. 17 shows the DC side voltage of switch bridge v_r, output voltage of switch bridge v_{ab}, resonant inductor current i_{Lr} and grid current i_o in grid cycle. The amplitudes of v_r and v_{ab} change with the grid current i_o, which is caused by the voltage change of the clamping capacitor C_c. The resonant inductor needs higher current amplitudes when the grid current i_o is larger according to (11). That also increases the current in clamping capacitor and the voltage of the clamping capacitor C_c also rises with the charge accumulated cycle by cycle.

The DC side voltage of switch bridge v_r, output voltage of switch bridge v_{ab} and resonant inductor current i_{Lr} in switching cycle with output power of 3kW are plotted in Fig. 18. The DC side voltage of switch bridge v_r bounces between zero and

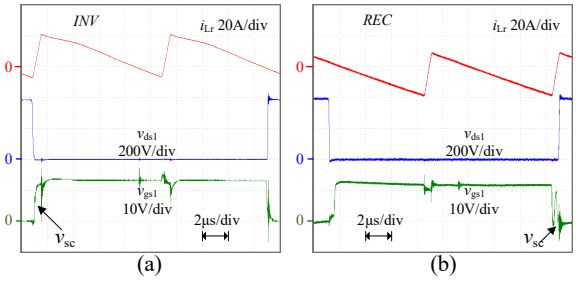

Fig. 19 The resonant inductor current i_{Lr}, drain-source voltage of S_1 and gate-source voltage of S_1 in (a) inverter mode (b) rectifier mode, $P_o = 3\text{kW}$, $\theta = \pi/3$

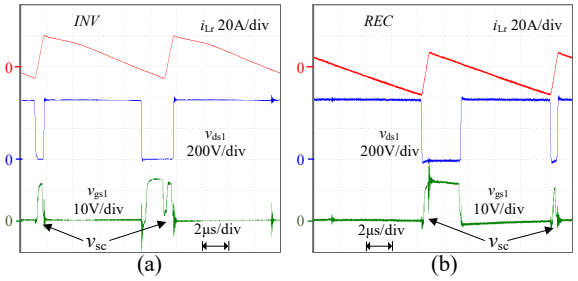

Fig. 20 The resonant inductor current i_{Lr}, drain-source voltage of S_1 and gate-source voltage of S_1 in (a) inverter mode (b) rectifier mode, $P_o = 3\text{kW}$, $\theta = -\pi/3$

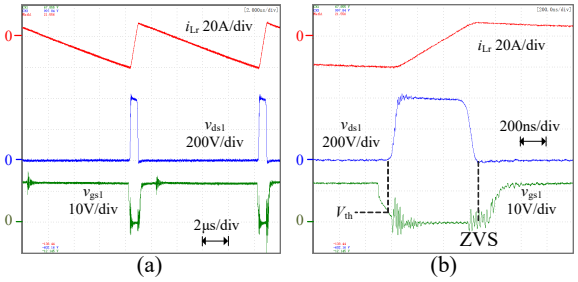

Fig. 21 The resonant inductor current i_{Lr}, drain-source voltage of S_a and gate-source voltage of S_a in rectifier mode (a) 2μs/div (b) 200ns/div, $P_o = 3\text{kW}$, $\theta = \pi/3$

$V_{bus}+V_{cc}$ at fixed frequency (100kHz) and the turn-off of body-diode is synchronized to the zero-voltage state of switch bridge (rising edge of v_{ab} in inverter mode and falling edge of v_{ab} in rectifier mode). The direction of resonant inductor currents i_{Lr} in the two modes are opposite while the amplitudes are equal.

Fig. 19 and Fig. 20 show the switching waveforms of main switch S_1. The drain-source voltage v_{ds1} falls to zero before the rising edge of gate-source voltage v_{gs1} in both inverter mode and rectifier mode, that means the ZVS is achieved. The difference between inverter mode and rectifier mode is the position of the short-circuit pulse, which is respectively controlled by the ZVS-SPWM in each mode.

The switching waveforms of auxiliary switch S_a are shown in Fig. 21. The switching cycle of S_a is 10μs and ZVS turn-on of S_a of is also realized. During the turn-off transient in Fig. 21(b), the gate-source voltage v_{gsa} falls to the threshold voltage V_{th} meanwhile the drain-source voltage v_{dsa} is still near zero level.

That means the turn-off loss of auxiliary switch S_a is also very small.

The efficiency of the ZVS single-phase DC-AC converter is shown as the curves in Fig. 22. The efficiency of inverter mode is slightly higher than rectifier mode due to higher turn-off loss of auxiliary switch. The efficiency test results are lower than the efficiency evaluation in Fig. 13 and Fig. 14. The distinction is about 0.5% with light load. The main reason is the minimum step of the short-circuit pulse generated by the digital controller is 11.11ns and the gate drive circuit can not transmit the drive pulse shorter than 33.33ns. That leads to surplus resonant inductor current and increases the loss of resonant inductor and auxiliary switch. While with higher power, the efficiency is mainly determined by the conducting loss of MOSFET and the difference between efficiency test and theoretical evaluation decreases to 0.2%. Another reason is the skin effect, proximity effect and harmonic loss of inductors are not included in the efficiency evaluation.

The harmonic analysis of the grid current i_o is given in Fig. 23. The total harmonic distortion (THD) of grid current is 2.99% with output power of 3kW. The third-order harmonic of grid current has the highest amplitude of 2.61%, which is mainly caused by the dead-time effect with the switching frequency of 100kHz. The harmonic spectrum of the grid voltage v_g is also given in Fig. 23 as a reference and the THD of v_g is 1.54%. The third-order harmonic percentage of the grid voltage is 0.71% and it also has the negative influence on the quality of grid current through the feed-forward loop of grid voltage in Fig. 15.

VII. Conclusions

The pulse-width modulation scheme for rectifier operation of a ZVS single-phase inverter is proposed. With the new ZVS modulation scheme the ZVS single-phase inverter can operate in rectifier mode with unity power factor and all switching devices are still ZVS turned-on. The unified resonant equations are derived for analyzing the ZVS single-phase inverter in both forward and reverse power flow. The similarities and differences of the resonant circuit between inverter mode and rectifier mode are discussed. The experiments of inverter operation and rectifier operation on a same ZVS single-phase inverter prototype verify the theoretical analysis and show the high efficiency and power quality.

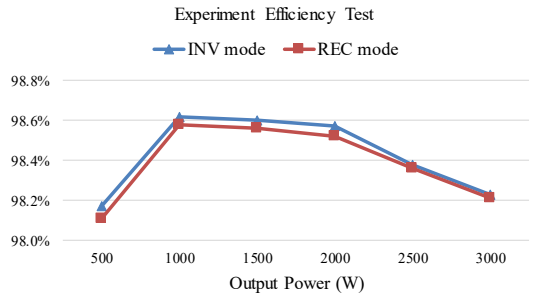

Fig. 22 Efficiency test results of inverter mode and rectifier mode

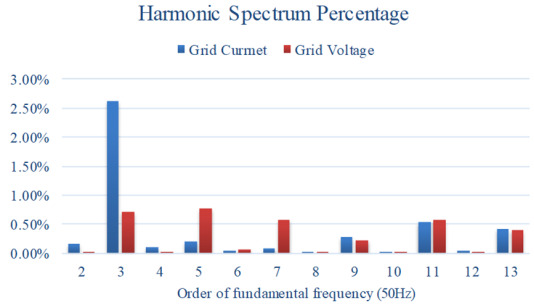

Fig. 23 The harmonic spectrum percentage of grid current i_o and grid voltage v_g in rectifier mode with 3kW power

References

[1] M. Bragard, N. Soltau, S. Thomas, and R. De Doncker, "The Balance of Renewable Sources and User Demands in Grids: Power Electronics for Modular Battery Energy Storage Systems," *IEEE Trans. Power Electron*., vol. 25, no. 12, pp. 3049–3056, Dec. 2010.

[2] H. Qian, J. Zhang, J. S. Lai, and W. Yu, "A High-Efficiency Grid-Tie Battery Energy Storage System," *IEEE Trans. Power Electron*., vol. 26, no. 3, pp. 886–896, Mar. 2011.

[3] L. Huber, J. Yungtaek, and M. M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers," *IEEE Trans. Power Electron*., vol. 23, no. 3, pp. 1381-1390, May 2008.

[4] C. Marxgut, F. Krismer, D. Bortis and J. W. Kolar, "Ultraflat Interleaved Triangular Current Mode (TCM) Single-Phase PFC Rectifier," *IEEE Trans. Power Electron*., vol. 29, no. 2, pp. 873-882, Feb. 2014.

[5] Z. Liu, F. C. Lee, Q. Li and Y. Yang, "Design of GaN-Based MHz Totem-Pole PFC Rectifier," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 799-807, Sept. 2016.

[6] B. Feng and D. Xu, "1-kW PFC Converter with Compound Active Clamping," *IEEE Trans. Power Electron*., vol. 20, pp. 324–331, Mar. 2005.

[7] Y. Chen, D. Xu, J. Xi, G. Hu, C. Du, Y. Li, and M. Chen, "A ZVS Grid-Connected Full-Bridge Inverter with a Novel ZVS SPWM Scheme," *IEEE Trans. Power Electron*., vol. 31, no. 5, pp.3626-3638, May 2016.

[8] R. Gurunathan and A. K. S. Bhat, "Zero-Voltage Switching DC Link Single-Phase Pulsewidth-Modulated Voltage Source Inverter," *IEEE Trans. Power Electron*., vol. 22, no. 5, pp. 1610-1618, Sep. 2007.

[9] M. Mezaroba, D. C. Martins and I. Barbi, "A ZVS PWM Full-Bridge Inverter with Active Clamping Technique using the Reverse Recovery Energy of the Diodes," in *Proc. IEEE IECON*, 2002, pp. 621-626.

[10] D. M. Divan, "The resonant DC link converter-a new concept in static power conversion," *IEEE Transactions on Industry Applications*, vol. 25, no. 2, pp. 317-325, Mar/Apr 1989.

[11] D. M. Divan and G. Skibinski, "Zero-Switching-Loss Inverters for High-Power Applications," *IEEE Transactions on Industry Applications*, vol. 25, no. 4, pp. 634-643, Jul/Aug 1989.

[12] M. Hartmann, H. Ertl and J. W. Kolar, "On the Tradeoff Between Input Current Quality and Efficiency of High Switching Frequency PWM Rectifiers," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp.3137-3149, July 2012.