An Enhanced PWM Method for Loss Balancing of Five Level T-Type Inverter in PV Systems

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***Abstract*—Multilevel inverters have attracted much industry and research concerns in photovoltaic (PV) applications. Although, it is demonstrated that power switching devices are subjected to unequal distribution of power losses and the reliability of multilevel inverters becomes low in accordance. Therefore, a new pulse width modulation (PWM) method is proposed in this paper for loss balancing in single phase five level inverters. The proposed method swaps the utilization of power components through the line period using the redundancy property between the switching states of T-type multilevel inverters. In addition, natural balance of voltages over DC link capacitors is achieved using the proposed method. The superiority of the proposed method is verified using simulation and experimental prototypes.**

Keywords—multilevel inverters; photovoltaic (PV); pulse width modulation (PWM); reliability

I. INTRODUCTION

Recently, improving the reliability of multilevel inverters has become of great importance with the increased penetration levels of photovoltaic (PV) sources in electrical grids [1]–[3]. The field operating statistics of installed PV systems have reported that power inverters possess the highest failure rates [4]–[6]. One main disadvantage of multilevel inverters is the power losses dissimilarity among power switching devices [7], [8]. These unequal power losses result in unbalanced junction temperatures in the switching devices. In addition, lifetime and power ratings of the whole converter are determined by the number of cycles to failure of the most stressed device [9].

The active neutral point clamped (ANPC) inverter has been developed to solve the unbalanced thermal stresses on power insulated gate bipolar transistors (IGBTs) devices in multilevel inverters [10]. In [11], the double frequency pulse width modulation (DFPWM) is applied to the ANPC inverter so as to balance power losses among power devices through utilizing the redundancy offered by the additional switches. The effective switching frequency of switching devices is doubled in DFPWM method. In [12], an adaptive type of DFPWM method is introduced to improve the conventional DFPWM method.

However, from the cost and size point of views, the T-type version of NPC inverters has become preferred in PV industry [13]–[15]. The T-type NPC leg has four IGBT switches compared to the six IGBTs in ANPC leg. Similar to other multilevel inverters, the problem of unbalanced power losses in power switching devices shortens the lifetime of the T-type inverter.

Stimulated by the abovementioned reliability problems in T-type inverters, this paper introduces a new PWM method for balancing the power losses in power IGBT devices. The proposed method swaps the utilization of power IGBTs during the line period so as to equalize the effective duty cycle and the root mean square (rms) currents through the IGBT switches.

The paper is organized as follows: Section II overviews the operation of single phase five level inverters and the conventional PWM methods. The proposed PWM method is presented in Section III. Simulation and experimental verifications of the proposed method are shown in Section IV to show the superiority of the proposed method. Lastly, the paper is concluded in Section V.

II. THE T-TYPE INVERTER AND CONVENTIONAL PWM METHOD

A. Five Level T-Type Inverter

Fig. 1 shows the circuit diagram of PV system integrated with single phase five level T-type inverter. The T-type inverter consists of four switches in the H-bridge part and each leg is connected to the neutral point (NP) O of the DC link capacitors through bidirectional switches. Each leg can generate three level, and the combination of the two legs can generate five levels at the output. Table I summarizes the different output levels and switch combinations to generate these levels and their effects on DC link capacitor voltages. It can be seen that there are some redundant switching states that can generate the same output voltage levels. The redundant switching states utilize different switches combinations and they have distinguished charging/discharging effects on the DC link capacitors.

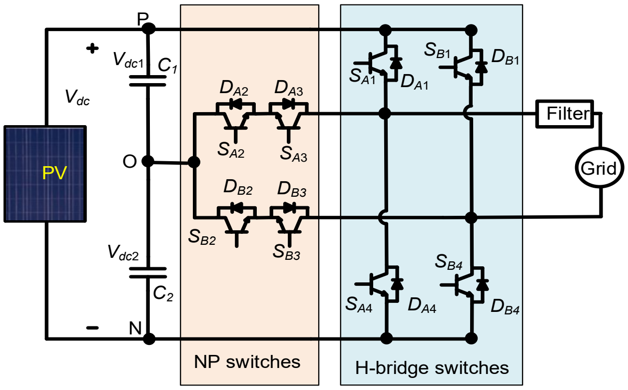


Fig. 1. PV system integrated with five level T-type inverter.

B. *Conventional PWM Method*

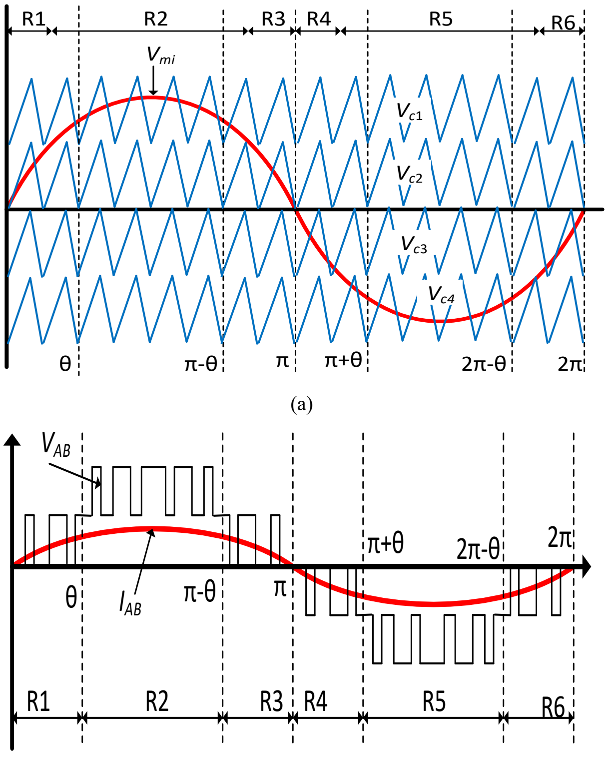
The basic operation of level shifted PWM of five level inverters and the corresponding output voltage V_{AB} and output current I_{AB} are shown in Fig. 2. It can be seen that the line period is divided into six regions R1-R6, wherein two levels are normally generated in each region. The corresponding effective duty cycles of conventional PWM methods for each of the H-bridge switches and NP switches are shown in Fig. 3.

From Fig. 3 (a), it is clear that the H-bridge switches of leg A (S_{A1}, and S_{A4}) have different effective duty cycles than that those of leg B (S_{B1} and S_{B4}). The same difference exist in the NP switches. Therefore, different values of rms currents flow in power IGBTs that result in mismatched power losses. Thence, mismatched junction temperatures and lifetime are existing as follows (1)-(3):

$$T_j = T_h + P_{loss}.\sum_{i=1}^{4} R_{th(i)} + P_{loss}.R_{th(c-h)} \tag{1}$$

$$N_f = A.(\Delta T_j)^{\alpha}.exp(\frac{E_a}{K_b T_j}) \tag{2}$$

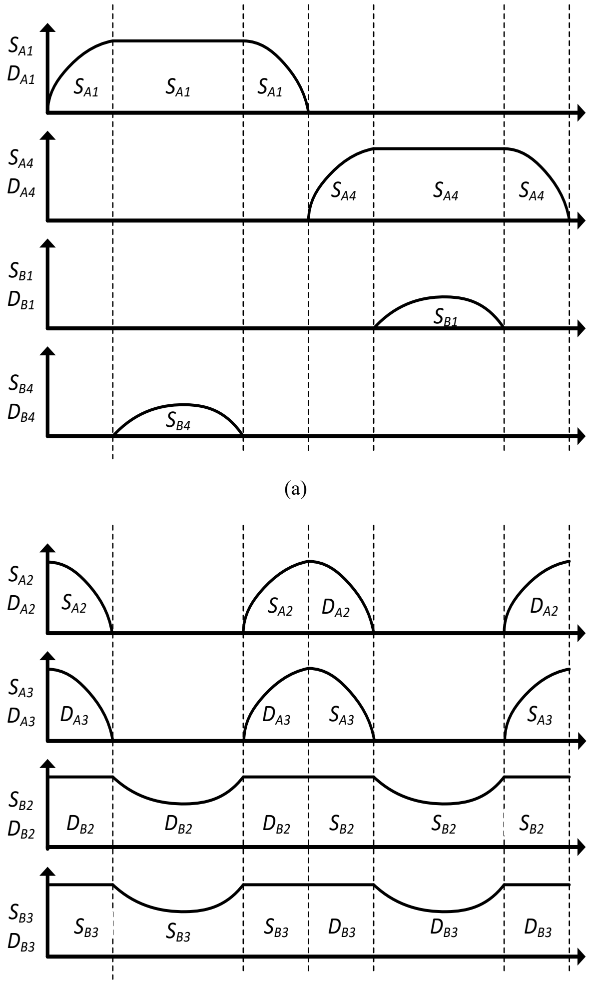
$$\Delta T_j = 2.P_{loss}.\sum_{i=1}^{4} R_{th(i)} \cdot \frac{(1-e^{-\frac{t_{on}}{\tau_{th(i)}}})^2}{1-e^{-\frac{t_e}{\tau_{th(i)}}}} \tag{3}$$



(a)

(a)

Fig. 2. PWM controlled five level inverter: (a) carrier based PWM, and (b) Output voltage and output current.



(a)

(b)

Fig. 3. Effective duty cycles of power IGBTS in conventional PWM method: (a) H-bridge switches, and (b) NP switches.

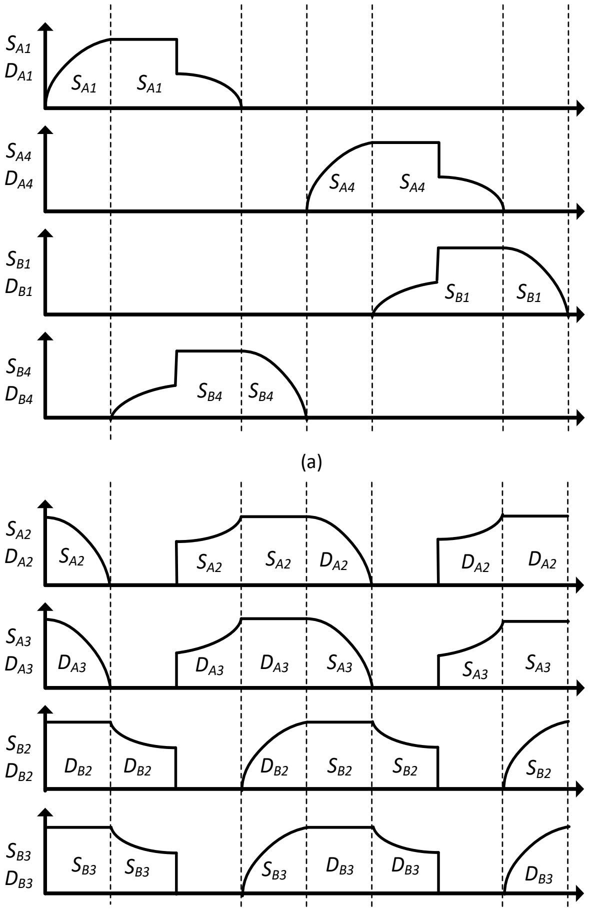
Table I. Output levels and switch combination of T-type inverter.

Amp.	**Seq.**	S_{A1}	S_{A2}	S_{A3}	S_{A4}	S_{B1}	S_{B2}	S_{B3}	S_{B4}	V_{dc1}	V_{dc2}
V_{dc}	V_{1_S1}	on	off	off	off	off	off	off	on	–	–
$0.5V_{dc}$	V_{2_S1}	on	off	off	off	off	on	on	off	↓	↑
	V_{2_S2}	off	on	on	off	off	off	off	on	↑	↓
0	V_{3_S1}	on	off	off	off	on	off	off	off	–	–
	V_{3_S2}	off	off	off	on	off	off	off	on		
	V_{3_S3}	off	on	on	off	off	on	on	off		
$-0.5V_{dc}$	V_{4_S1}	off	on	on	off	on	off	off	off	↓	↑
	V_{4_S2}	off	off	off	on	off	on	on	off	↑	↓
$-V_{dc}$	V_{5_S1}	off	off	off	on	on	off	off	off	–	–

III. THE PROPOSED METHOD

The proposed PWM method is based on using swapped gating pulses of IGBT switches within the line period so as to achieve balanced power losses through the IGBTs devices in T-type inverters. The main idea of the proposed PWM is utilizing the redundant switching states as in Table I through using each DC link capacitor for swapped π/4 period during the whole line cycle. Fig. 4 shows the effective duty cycles of the power switches under the proposed PWM method. It can be seen that balanced effective duty cycles are achieved in the power IGBTs and the freewheeling diodes as well. In addition, the system efficiency is kept the same under the proposed PWM. Thence, the proposed PWM method balances the rms currents of the IGBT switches and the thermal stresses are balanced in accordance. This is advantageous over the conventional PWM methods, which suffer from unequal distribution of thermal stresses among the power IGBT switches.

The proposed PWM swaps the H-bridge switches (S_{A1} and S_{A4}) of leg A with (S_{B1} and S_{B4}) in leg B to make the rms currents through the four switches identical and balanced power losses can be achieved in accordance. Thence, the most thermally stressed devices are alleviated using the proposed method and better lifetime expectancy can be achieved.



(a)

(b)

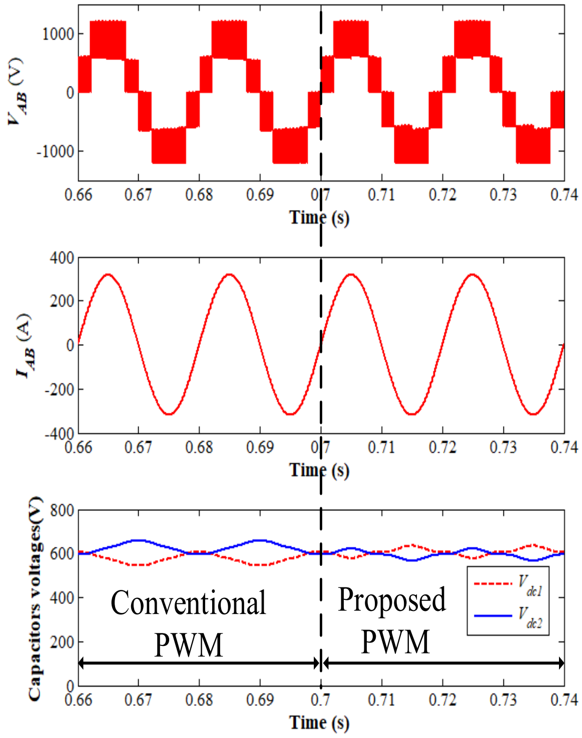
Fig. 4. Effective duty cycles of power IGBTS in the proposed PWM method: (a) H-bridge switches, and (b) NP switches.

IV. SIMULATION AND EXPERIMENTAL RESULTS

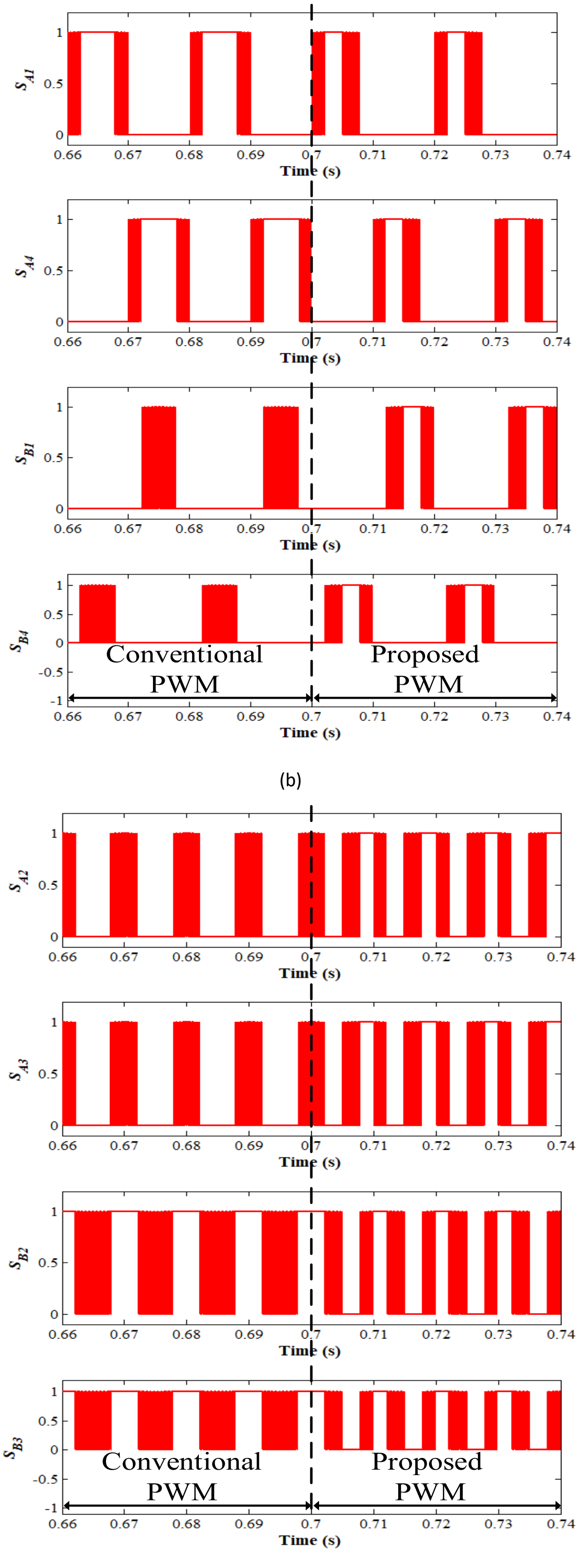
Table II shows the system parameters for simulation and experimental results. The FF225R17ME4 IGBT/Diode module is used for calculating the power losses and thermal behavior in simulation results [16]. The power losses are calculated based on numerical simulation using the selected power IGBT device datasheet and the power losses calculation method in [11].

The output voltage, output current and voltages over DC link capacitors are shown in Fig. 5 (a). The proposed PWM method maintains the same output power ratings. It can be seen that the output current is preserved the same under conventional and the proposed PWM method. In addition, the output voltage V_{AB} has the same number of output voltage levels under both of the conventional and the proposed PWM methods. Thence, the proposed PWM does not deteriorates the output performance nor the output ratings of the inverters. The voltage balance over DC link capacitors is highly needed for longer lifetime of DC link capacitors, and for enhanced performance of the output current and voltage waveforms. The voltages of DC link capacitors shown in Fig. 5 (a) are balanced under conventional and proposed PWM methods with small ripple as a result of swapping in part of line period.

The balancing of the effective gating pulses of H-bridge and NP power switches are shown in Fig. 5 (b), and (c), respectively. It is clear that there are unbalance between the power switches under the conventional PWM method. This in turn results in unequal distribution of power losses and thermal stresses among the power switches. In contrast, it can be seen from Fig. 5 (b) and (c) that the gating pulses of power switches are balanced under the proposed PWM method. Thence, balanced power losses and thermal stresses can be obtained.



(a)



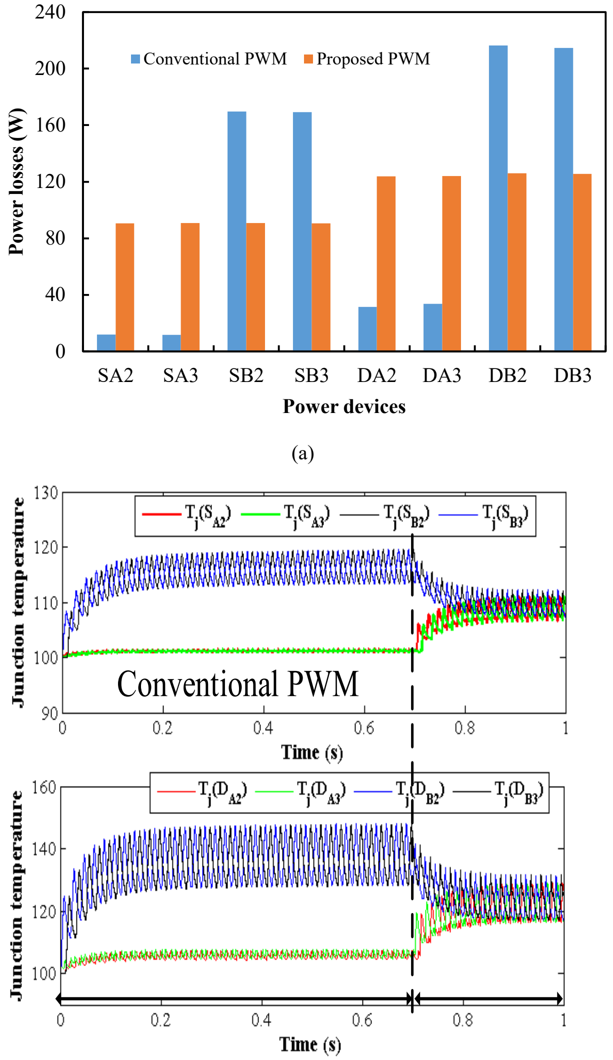
(b)

(c)

Fig. 5. Simulation results: (a) V_{AB}, I_{AB}, V_{dc1}, V_{dc2}, (b) Gating pulses of H-bridge switches, and (c) Gating pulses of NP switches.

Fig. 6 (a) shows the power losses of NP switches under conventional and proposed PWM methods. It can be seen that there are unbalanced power losses among the power switches under the conventional PWM method. The NP switches of leg B have higher power losses than NP switches in leg A. In addition, the NP diodes of leg B possess higher power losses than those of leg A. In contrast, it is clear that the proposed PWM method achieves balanced power losses among switches. The NP switches of leg A and leg B have the same power losses. Moreover, there are equal power losses among the diodes of both legs.

The junction temperature comparisons of NP switches are shown in Fig. 6 (b). Applying the proposed PWM method results in balancing the junction temperature of the switches of both legs. Thence, the feasibility of the proposed method to preserve longer lifetime of the power devices is clear as a result of lower thermal stresses on devices. A higher reliability of PV systems is obtained in accordance.



(a)

(b)

Fig. 6. Comparison of conventional and the proposed PWM: (a) Power losses, and (b) Junction temperatures

Moreover, a scaled down prototype is set in the lab. The parameters of the experimental setup are summarized in Table II. The output voltage, output current and DC link voltages are shown in Fig. 7 (a). It is clear that the proposed PWM method preserves the same output ratings and levels as in conventional PWM. In addition, no derating operation is required for the output currents of the inverter. The output voltage waveform has five levels in its output.

In addition, the voltages over DC link capacitors are balanced under the proposed PWM method. Thence, no additional voltage stresses exist under the proposed PWM method. The experimental results match the simulation results regarding the preservation of same output voltage, current, and balanced DC link capacitors' voltages with smaller ripples.

The gating pulsed under conventional and the proposed algorithm are shown in Fig. 7 (b) and (c) for H-bridge and NP switches, respectively. It can be seen that the conventional PWM method possesses unbalanced gating pulses for H-bridge devices of leg A and leg B. In addition, the gating pulses of NP switches have different switching patterns among leg A and leg B. From another side, the proposed PWM offers balanced gating pulses for the H-bridge switches. Thence, the same gating patterns are applied for the switches of leg A and leg B. The same benefit exists for the NP switches and diodes. Hence, redistribution of thermal stresses is obtained.

The proposed algorithm can effectively balance the effective gating pulsed of power switches. Therefore, thermal stresses can be reduced from the most stressed power semiconductor devices. In accordance, the reliability of the whole PV inverter system is improved and longer lifetime of the power components is achieved.

V. CONCLUSIONS

A new PWM method is proposed for loss balancing between IGBTs in five level T-type inverters in PV applications. The conventional PWM methods suffer from unequal distribution of thermal stresses between power IGBT devices. The proposed method utilizes the redundancy between switching states in multilevel inverters to swap the power devices equally during the line period. Thence, the proposed PWM method can balance the thermal stresses over the power switches in multilevel inverter. The simulation and experimental results verify the ability of proposed method to balance the power losses. A great improvements in thermal stresses reduction and lifetime extension have been obtained. Therefore, the reliability of the whole PV inverter system can be improved using the proposed PWM method.

Table II. Parameters for simulation and experimental results.

Parameter	Simulation	Experimental
DC-link voltage V_{dc}	1200 V	100 V
DC-link capacitance C_1, C_2	10 mF	1.5 mF
Output frequency f_l	50 Hz	50 Hz
Switching frequency f_s	5 kHz	5 kHz
Output load R, L	3 Ω, 1 mH	10 Ω, 3 mH

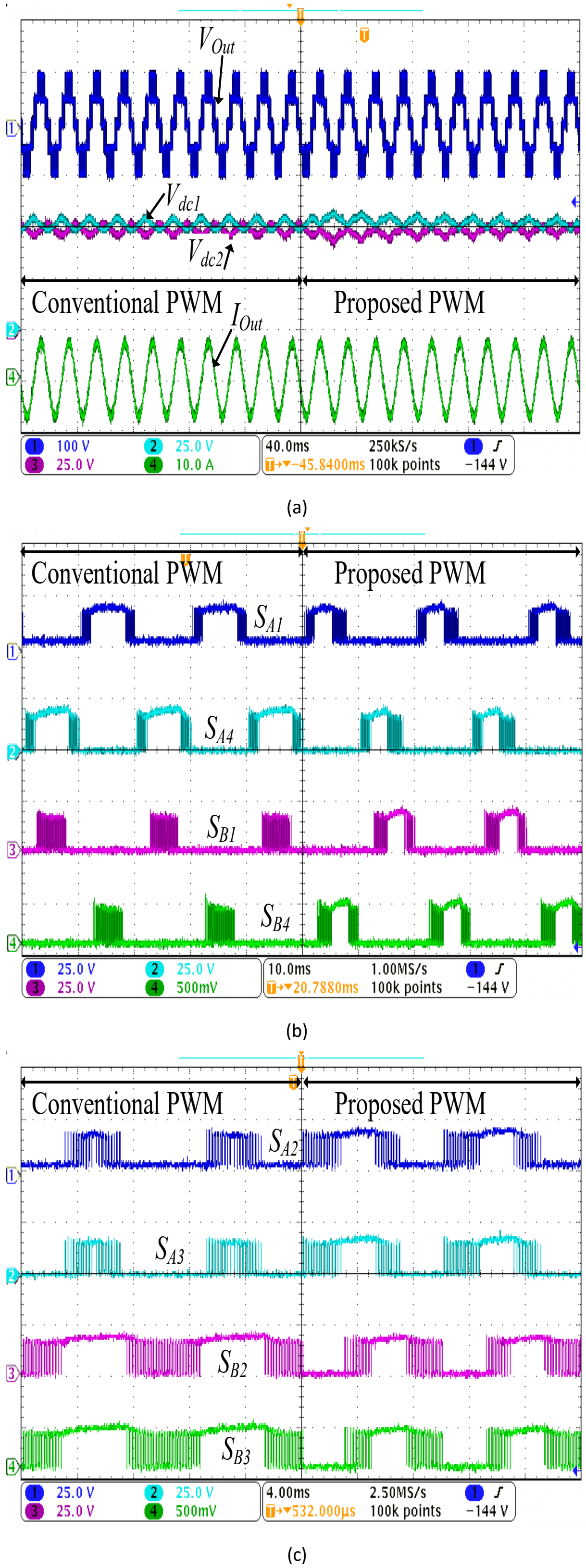


Fig. 7. Experimental results: (a) V_{AB}, I_{AB}, V_{dc1}, V_{dc2}, (b) Gating pulses of H-bridge switches, and (c) Gating pulses of NP switches.

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