# Carrier-based PWM Design of Multilevel ANPC-based Converter through Hierarchical Decomposition

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***Abstract*—Traditional PWM design of multilevel active-neutral-point-clamped (ANPC) based converter is complex and lack of scalability especially when the voltage level increases. This is particularly true when considering loss distribution, waveform quality and control modularity in the PWM process. This paper firstly proposes a general PWM design approach for multilevel ANPC-based converter through hierarchical decomposition. Modified from decomposition theory, the hierarchical decomposition is introduced in this work to facilitate identification of different operation patterns for an arbitrary ANPC-based topology. Based on the proposed approach, simplified PWM schemes for various patterns are designed modularly through carrier-based methods (i.e. level-shift and phase-shift PWM). Experiments of ANPC-based topologies show the universality of the proposed method.**

***Keywords—Carrier-based pulse-width modulation; active-neutral-point-clamped converter; multilevel pulse-width modulation; hierarchical decomposition***

## I. INTRODUCTION

Voltage source multilevel converters (MLCs) have been widely applied in industry due to the merits of high-quality output, reduced voltage stress on semiconductor devices, high equivalent switching frequency, low dv/dt, and so on [1].

Among various topologies, the active-neutral-point-clamped (ANPC) topology (e.g. three-level (3L) ANPC [2]) can easily achieve equal loss distribution compared to the conventional neutral-point-clamped (NPC) topology. In addition, various MLCs are proposed based on the multilevel ANPC topology, such as the five-level (5L) ANPC [3], Dual Flying Capacitor (DFC) ANPC [4], etc. Challenges of these ANPC-based topologies, such as circuit analysis [5], basic modulation schemes [6-7], fault-tolerant controls [8-9], have been studied for years. However, existing PWM methods mainly focus on 3L topologies and unfortunately lead to very complex modulation algorithm for higher-level ANPC (i.e. four-level (4L) or higher) due to the lack of systematic analysis, especially when considering the system loss distribution, waveform quality, and control modularity.

In this paper, a simplified systematic PWM design method is proposed for arbitrary ANPC converters through hierarchical decomposition method. Based on this method, an *N*-level ANPC-based topology can be decomposed into smaller sub-topologies (output level is lower than *N*), and then, different PWM patterns should be adopted for each sub-topology, which naturally simplifies the switching network into several decoupled parts, i.e. high switching frequency (**HSF**) parts with PWM operation and low switching frequency (**LSF**) parts. Thereafter, systematic PWM design procedure can be carried out for each part with corresponding topological features, which results in simplification of various modulation strategies.

## II. HIERARCHICAL DECOMPOSITION

Here are several concepts that will be used in this paper: (1) A *switch group* (**SG**) is a column of switches in an ANPC topology as labeled by red dotted box in **Fig. 1(a)~(h)**. (2) A *switch cell* (**SC**) is a pair of two series-connected switches with complementary states (also known as half-bridge) in an SG (in **Fig. 1(a)**, $SG_1$ has two SCs, while $SG_2$ has one SC). (3) A *simplified representation* is the figure of ANPC topology with only labels of SGs and SCs and colors indicating operation patterns (red is for **HSF** parts, blue is for **LSF** parts) as shown in **Fig. 1(i)~(p)**.

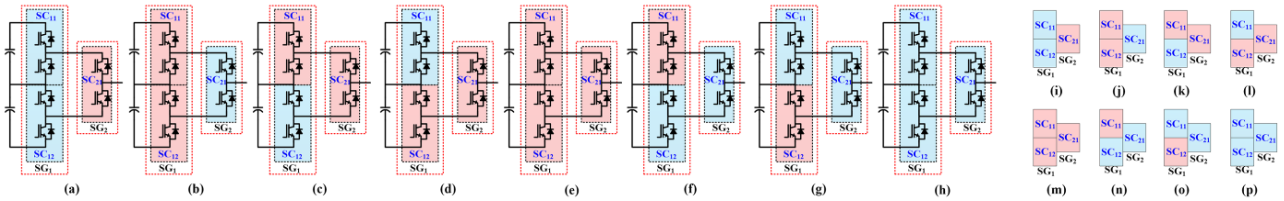


Fig. 1: All possible PWM patterns of 3L ANPC (a) 3L-PWM-1, (b) 3L-PWM-2, (c) 3L-PWM-3, (d) 3L-PWM-4, (e) 3L-PWM-5, (f) 3L-PWM-6, (g) 3L-PWM-7, (h) 3L-PWM-8, simplified representations of corresponding PWM patterns (i)~(p).

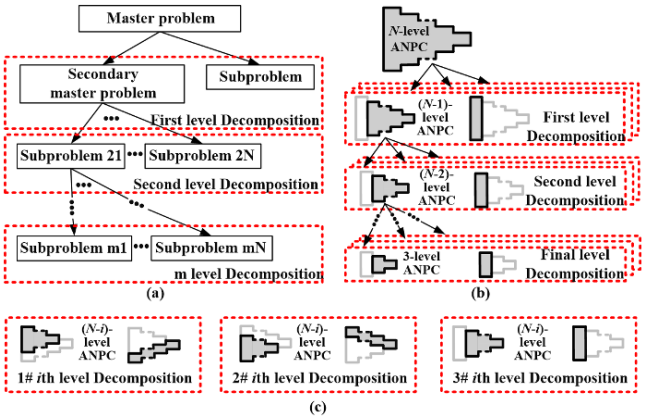


Fig. 2: hierarchical decomposition (a) for network utility maximization, (b) for ANPC-based topology, (c) three possible results for *i*th level decomposition.

Decomposition theory was proposed for the design of modularized and distributed control of wired and wireless networks [10], especially for solving the network utility maximization (**NUM**) problem. The basic idea of decomposition for NUM is to decompose the original large optimal problem into subproblems (see **Fig. 2(a)**). Primal decomposition, dual decomposition, and hierarchical decomposition methods were introduced in literature [11-12]. Due to the similarity between information network and switch network, this analytical approach to NUM problems can be modified for topology analysis and modulation design. Therefore, the basic idea of decomposition for ANPC-based converters is to hierarchically decompose the original large complex circuit into several down-scale circuits (see **Fig. 2(b)**).

Here the First Level Decomposition (**1st-D**) is to split an *N*-level ANPC topology into two sub-topologies, and one of them is an (*N*-1)-level ANPC topology. Then the (*N*-1)-level ANPC topology obtained in **1st-D** can be further split into two sub-topologies, and one of them is (*N*-2)-level ANPC topology during the process of the second level decomposition (**2nd-D**). For an *N*-level ANPC topology, the Final Level Decomposition (or it can be called **(*N*-3)th-D**) is expected to obtain 3L ANPC topology and another sub-topology. The maximum number of $i^{th}$ level decomposition is always three as shown in **Fig. 2(c)**. Therefore, for an *N*-level ANPC topology, there should be $3^{N-3}$ decompositions (*N* is an integer, *N*>3). For a 4L-ANPC converter, there are three 1st-Ds as shown in **Fig. 3**. In such way, an arbitrary ANPC topology can always be considered as an iterative representation based on 3L ANPC cells regardless of whatever potential PWM operation principles are applied. For a 3L ANPC topology, there are five PWM patterns that can guarantee effective operation of whole voltage output ranges with pulse-width modulated process as shown in **Fig. 1(a)~(e)** [6, 13] (detailed discussion will be provided in PWM design section).

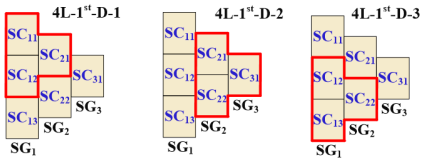


Fig. 3: Three first level decompositions of 4L ANPC topology.

## III. The General PWM Design Procedure for ANPC-based Converters

Although different modulation methods were proposed in literature, most of them are designed for an ANPC with specific level (e.g. 3L ANPC topology, 5L ANPC-based topology) [2, 6, 7, 13-14]. These conventional design methods normally face difficulties of scalability for high-level ANPC topologies. In fact, considering all the redundant switching states of an ANPC topology, each SG/SC of the topology may operate at **HSF** based on a certain modulation scheme, resulting in a large number of possible PWM patterns. However, only a small number of PWM patterns are considered in literature, leading to non-comprehensive and unfair conclusions. In [15], a specific PWM scheme is introduced by applying the virtual-vector concept for a 4L ANPC. In [16], another PWM pattern is proposed for a general *N*-level converter leg, changing the states of *N* switches between the transition of two adjacent switching states. More patterns are remained to be evaluated.

To demonstrate the count of possible patterns, a 5L ANPC topology is used as an example. Assuming that there are *k* SCs (the total number of SCs in 5L ANPC topology is 10, $0 \le k \le 10$) operating at **HSF**, the number of possible PWM patterns in this case can be calculated by [10*9*⋯*k/*k** (*k*-1) *⋯*2*1]. The total number of all possibilities is 1024 ($2^{10}$). For an *N*-level ANPC, this number can be calculated by $2^{N(N-1)/2}$.

A conventional method is to exhaustively search all the possibilities one by one and carry out PWM design process for each of them. However, not all patterns can realize proper PWM operation during the whole output regions. These ineffective patterns greatly increase the complexity of the PWM design process. To avoid this problem, a systematic PWM design procedure with three simple steps is proposed based on hierarchical decomposition as shown in **Fig. 4**. Firstly, the SG-based PWM patterns are derived to realize basic pulse-width modulated operation during the whole output regions. Secondly, effective PWM patterns can be designed based on step one and hierarchical decomposition process. Thirdly, the modularized modulation can be designed for each pattern by utilizing the carrier-based PWM with a modular evolution from low to high level ANPC converters. This three-step procedure is introduced in detail through following **Sections IV** and **V**.

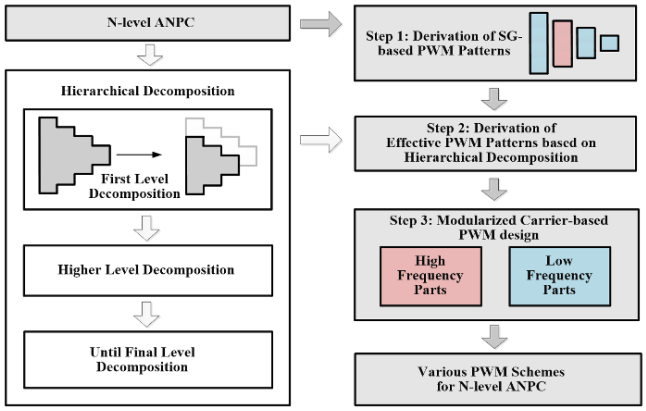


Fig. 4: The PWM design procedure based on hierarchical decomposition.

## IV. Derivation of PWM Patterns

### A. Switch-group-based PWM patterns

The first step of PWM design is to identify effective patterns of an ANPC topology based on all the potential operation patterns of its SGs, which is called SG-based PWM patterns. In fact, the similar concept, *Switching Pole* is introduced to describe each column of switches of an ANPC leg in [17]. Same as in [16], a specific pattern is presented to guarantee the proper PWM operation during the whole output regions, however, all the other patterns are neglected.

To derive all effective SG-based PWM patterns, the general $N$-level ANPC topology is shown in **Fig. 5(a)**. It is composed of $N$-1 SGs and a dc link using $N$-1 series-connected capacitors (or dc sources). Each SG may operate at **HSF**. Theoretically, for an $N$-level ANPC topology, there are $2^{N-1}$ kinds of SG-based PWM patterns. Since this paper is mainly focused on carrier-based PWM design, the one with all SGs at **LSF** is not considered. Therefore, a $N$-level ANPC topology has $(2^{N-1}$-1) effective SG-based PWM patterns.

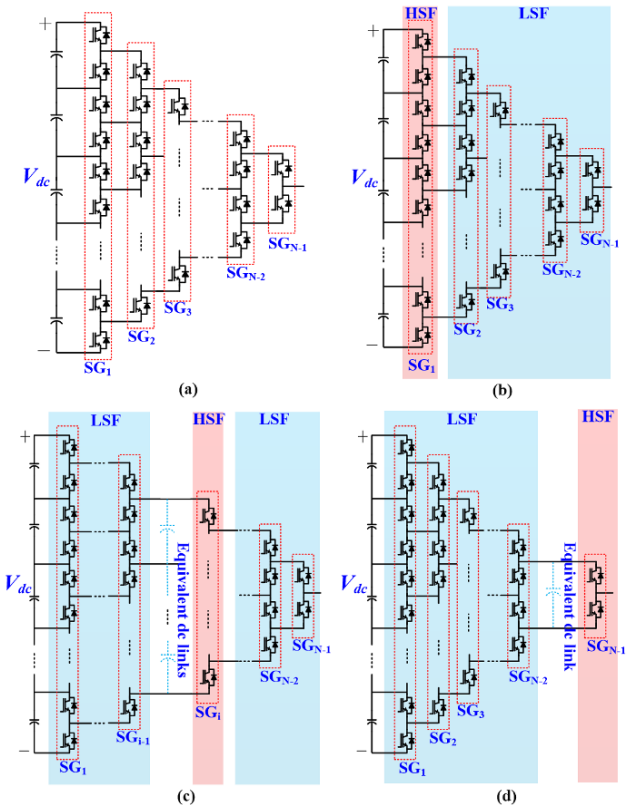


Fig. 5: (a) $N$-level ANPC Topology, (b) SG-a, (c) SG-b, (d) SG-c.

**Fig. 5(b)~(d)** shows three representative types as examples named SG-a (in **Fig. 5 (b)**), SG-b (in **Fig. 5 (c)**), SG-c (in **Fig. 5 (d)**). In **Fig. 5 (b)**, the converter operates with one **HSF** part (red region) and one **LSF** part (blue region). $SG_1$ (**HSF** part) is designed to operate at PWM frequency $f_{PWM}$, while $SG_2$~$SG_{N-1}$ can be basically controlled to generate staircase or step waveform by using fundamental frequency $f_0$. In **Fig. 5(c)**, the converter operates with two **LSF** parts and one **HSF** part. $SG_i$ ($i$ is an integer satisfying $2 \le i \le N-2$) is controlled at **HSF** (the rest at **LSF**). By manipulating the operation of $SG_1$~$SG_{i-1}$, the output port voltage of the $SG_{i-1}$ can be controlled at $f_0$ to form equivalent dc links as labeled in **Fig. 5(c)**. Then $SG_i$ should work at **HSF** through the modulation process to output modulated voltage pulses during the whole output regions. In **Fig. 5(d)**, the converter operates with one **LSF** part and one **HSF** part with $SG_{N-1}$ at **HSF** (the rest at **LSF**).

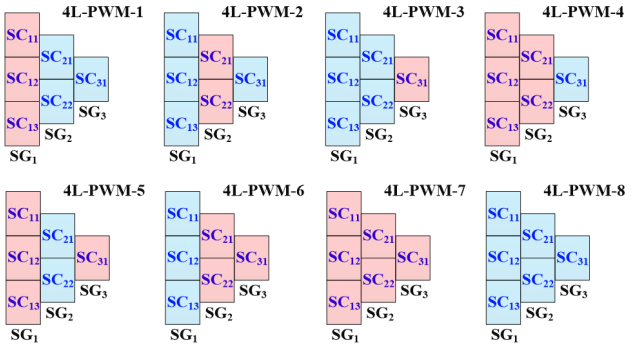


Fig. 6: Eight SG-based PWM patterns of 4L ANPC.

Take a 4L ANPC topology as an example. Eight SG-based PWM patterns of 4L-ANPC are derived as shown in **Fig. 6**. The first seven patterns are effective and can realize PWM output in full operation range. While the eighth one named 4L-PWM-8 has all SGs operating at **LSF**, and is out of scope.

### B. Derivation of effective PWM patterns through hierarchical decomposition

The second step of PWM design is to derive other PWM patterns of an ANPC topology through combinations of SG-based PWM patterns and hierarchical decomposition process. The unique combinations will be further extended considering all the PWM patterns of 3L ANPC as shown in **Fig. 1**, which results in various possible PWM patterns. For those SG-based patterns with **HSF** $SG_{N-1}$, all seven 3L patterns can be utilized. While for those without **HSF** $SG_{N-1}$, five effective 3L patterns can be utilized.

To easily obtain all the unique patterns, all results could be sorted according to their number of **HSF** SCs. Take a 4L ANPC as an example, its effective SG-based PWM patterns (see **Fig. 6**) and its hierarchical decompositions (see **Fig. 3**) are considered which results in 21 combinations. After utilizing all possible PWM patterns of 3L ANPC, 49 unique PWM patterns are derived as shown in **Table I**.

The **HSF** SCs are indicated as "1", while the **LSF** SCs are noted by "0". Systematic naming rules are based on the number of output levels, the level of topological decomposition, and the SG-based PWM pattern. For a 4L ANPC, the name of 1st-D-based PWM patterns can be determined by using format: 4L-PWM-$x_1x_2x_3$, where $x_1$ is referred as the SG-based PWM pattern of 4L ANPC, $x_2$ means one of 1st-Ds, $x_3$ shows one of the possible PWM patterns of 3L ANPC. The name of 1st-D-based 5L PWM patterns can be determined by using a similar format as 4L ANPC: 5L-PWM-$x_1x_2x_3$, where $x_1$ is referred as the SG-based PWM pattern of 5L ANPC, $x_2$ means one of 1st-Ds, $x_3$ shows one of the possible SG-based PWM patterns of 4L ANPC. Furthermore, the derivation process of PWM patterns of an arbitrary $N$-level ANPC can be carried out in a

similar way. Due to limited paper length, other patterns of higher-level ANPC are omitted here.

TABLE I
DIFFERENT PWM PATTERNS OF 4L ANPC

| No | 4L PWM Patterns | $SC_{11}$~ $SC_{13}$, $SC_{21}$~ $SC_{22}$, $SG_{31}$ | | | No | 4L PWM Patterns | $SC_{11}$~ $SC_{13}$, $SC_{21}$~ $SC_{22}$, $SG_{31}$ | | |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 4L-PWM-1 | 111 | 00 | 0 | 26 | 4L-PWM-331 | 011 | 00 | 1 |
| 2 | 4L-PWM-111 | 001 | 10 | 0 | 27 | 4L-PWM-333 | 010 | 01 | 1 |
| 3 | 4L-PWM-112 | 101 | 10 | 0 | 28 | 4L-PWM-334 | 001 | 01 | 1 |
| 4 | 4L-PWM-113 | 011 | 10 | 0 | 29 | 4L-PWM-335 | 011 | 01 | 1 |
| 5 | 4L-PWM-114 | 111 | 10 | 0 | 30 | 4L-PWM-336 | 010 | 00 | 1 |
| 6 | 4L-PWM-123 | 111 | 10 | 1 | 31 | 4L-PWM-337 | 001 | 00 | 1 |
| 7 | 4L-PWM-124 | 111 | 01 | 1 | 32 | 4L-PWM-4 | 111 | 11 | 0 |
| 8 | 4L-PWM-131 | 100 | 01 | 0 | 33 | 4L-PWM-413 | 101 | 11 | 0 |
| 9 | 4L-PWM-132 | 110 | 01 | 0 | 34 | 4L-PWM-5 | 111 | 00 | 1 |
| 10 | 4L-PWM-133 | 101 | 01 | 0 | 35 | 4L-PWM-511 | 001 | 10 | 1 |
| 11 | 4L-PWM-134 | 111 | 01 | 0 | 36 | 4L-PWM-512 | 101 | 10 | 1 |
| 12 | 4L-PWM-2 | 000 | 11 | 0 | 37 | 4L-PWM-513 | 011 | 10 | 1 |
| 13 | 4L-PWM-212 | 100 | 11 | 0 | 38 | 4L-PWM-516 | 101 | 00 | 1 |
| 14 | 4L-PWM-213 | 010 | 11 | 0 | 39 | 4L-PWM-531 | 100 | 01 | 1 |
| 15 | 4L-PWM-214 | 110 | 11 | 0 | 40 | 4L-PWM-532 | 110 | 01 | 1 |
| 16 | 4L-PWM-222 | 000 | 10 | 1 | 41 | 4L-PWM-533 | 101 | 01 | 1 |
| 17 | 4L-PWM-223 | 000 | 01 | 1 | 42 | 4L-PWM-6 | 000 | 11 | 1 |
| 18 | 4L-PWM-233 | 001 | 11 | 0 | 43 | 4L-PWM-612 | 100 | 11 | 1 |
| 19 | 4L-PWM-234 | 011 | 11 | 0 | 44 | 4L-PWM-613 | 010 | 11 | 1 |
| 20 | 4L-PWM-3 | 000 | 00 | 1 | 45 | 4L-PWM-614 | 100 | 11 | 1 |
| 21 | 4L-PWM-311 | 110 | 00 | 1 | 46 | 4L-PWM-633 | 001 | 11 | 1 |
| 22 | 4L-PWM-313 | 100 | 10 | 1 | 47 | 4L-PWM-634 | 011 | 11 | 1 |
| 23 | 4L-PWM-314 | 010 | 10 | 1 | 48 | 4L-PWM-7 | 111 | 11 | 1 |
| 24 | 4L-PWM-315 | 110 | 10 | 1 | 49 | 4L-PWM-713 | 101 | 11 | 1 |
| 25 | 4L-PWM-316 | 100 | 00 | 1 | | | | | |

Note: '1' means **HSF**, '0' means **LSF**

## V. DESIGN AND IMPLEMETATION OF CARRIER-BASED PWM

Through the proposed process, various PWM patterns are systematically obtained. As a third step, the PWM design can be carried out.

For **HSF** SCs in one PWM pattern, pulse-width modulation schemes should be designed to produce the modulation reference. Compared to space-vector-based modulation, carrier-based modulation is more straightforward to be extended for high-level topologies, without increasing the complexity of the algorithm [18]. In [19], two types of multicarrier-based PWM are introduced, i.e. level-shift (**LS**) PWM, phase-shift (**PS**) PWM, respectively. In **Section V. B** and **C**, carrier-based PWM are introduced for **HSF** SCs in various PWM patterns. For **LSF** SCs in PWM patterns, modulation processes should assist the operation of **HSF** parts and maintain the appropriate device voltages. In **Section V. D**, modulation at fundamental switching frequency during full output range is designed for **LSF** SCs to reduce the switching actions as much as possible.

### A. *Device utilization patterns*

To design proper carrier-based PWM for a certain pattern, the general principles of SCs operation during whole output ranges should be investigated first. For an arbitrary *N*-level ANPC, two output adjacent levels are normally produced during a certain period to achieve better voltage quality and low dv/dt, e.g. *i*-level and (*i*-1)-level, $i \leqslant N$. To systematically indicate the SCs that participate in two output adjacent levels, *device utilization patterns* are identified accordingly. For 4L ANPC topology, there are four levels named as 4L, 3L, 2L, 1L. To output two adjacent levels, the participated SCs follows three device utilization patterns named as 4L-DUP-1 (**Fig. 7(a)**), 4L-DUP-2 (**Fig. 7(b)**), 4L-DUP-3 (**Fig. 7(c)**). To output [1L, 2L], at least one of the following cells $SC_{13}$, $SC_{22}$, $SC_{31}$ (highlighted by yellow) must be utilized, while $SC_{12}$ and $SC_{21}$ (in light grey) could be utilized as shown in **Fig. 7(a)**. The dark grey $SC_{11}$ has nothing to do with associated output region. To output [2L, 3L], at least one of the following cells $SC_{12}$, $SC_{21}$, $SC_{22}$, $SC_{31}$ (highlighted by yellow) must be utilized, while $SC_{11}$ and $SC_{13}$ (in light grey) could be utilized as shown in **Fig. 7(b)**. To output [3L, 4L], at least one of $SC_{11}$, $SC_{21}$, $SC_{31}$ (highlighted by yellow) must be utilized in the current paths. At the same time, $SC_{12}$, $SC_{22}$ (highlighted by light grey) could also be utilized. The $SC_{13}$ (highlighted by dark grey) cannot affect this output region.

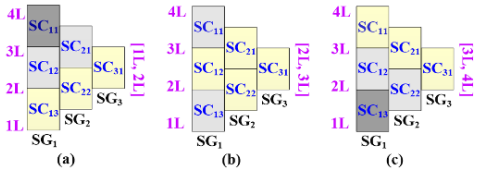


Fig. 7: Three device utilization patterns of 4L ANPC: (a) 4L-DUP-1, (b) 4L-DUP-2, (c) 4L-DUP-3.

### B. *Carrier-based PWM for 3L ANPC*

#### (1) Level-shift PWM

For 3L ANPC, there are two SG-based PWM patterns of which the LS PWM can be easily applied as shown in **Fig. 1 (a)~(b)**. In [6], these two PWM schemes are referred as modulation 1 (**Fig. 8(a)**), modulation 2 (**Fig. 8(b)**), and are analyzed in detail.

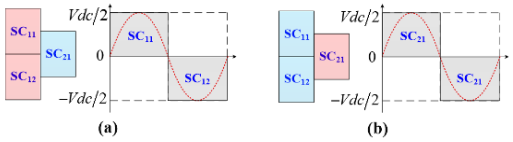


Fig. 8: Level-shift PWM for 3L ANPC under: (a) 3L-PWM-1 in Fig. 1(a), (b) 3L-PWM-2 in Fig. 1(b).

#### (2) Phase-shift PWM

PS-PWM can be applied for three PWM patterns shown in **Fig. 1(c)~(e)**. For the pattern 3L-PWM-3 in **Fig. 1(c)**, a modified PS-PWM is introduced. The gate signals are shown in **Fig. 9(a)**. There are two carriers, the first one (black line) is compared with the voltage reference (red), the second one (green) is compared with a tunable proportion (blue) which influences the number of switching actions of $SC_{11}$ and $SC_{21}$. The rotation of the conducting SC occurs when the proportion

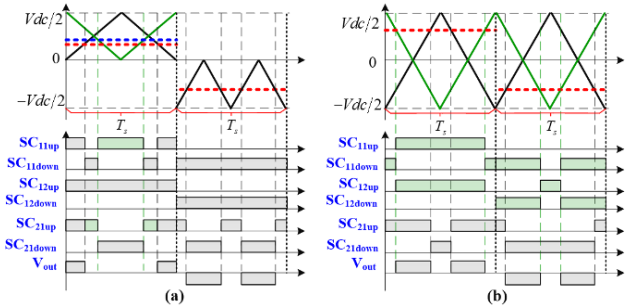


Fig. 9: Phase-shift PWM for 3L ANPC under: (a) 3L-PWM-3 in Fig. 1(c), (b) 3L-PWM-5 in Fig. 1(e).

is bigger/smaller than the second carrier. Similar scheme can be designed for 3L-PWM-4 in **Fig. 1(d)**.

In [13], PS PWM named doubled frequency PWM can be applied for pattern 3L-PWM-5 (see **Fig. 1(e)**) to achieve a better loss distribution compared with modulation 1 (**Fig. 1(a)**) and modulation 2 (**Fig. 1(b)**). While it can also be considered as a mixture of the modulation 1 and modulation 2 in one carrier period [20]. The gate signals are shown in **Fig. 9(b)**. The SC with subscript "up" means the ON/OFF state of the upper switch in a SC, while the subscript "down" means the lower switch. All three SCs operate in PWM frequency, and share the loss evenly. And the equivalent switching frequency is doubled by this method.

### *C. PWM design for **LSF** SCs of ANPC (>3L)*

In **Fig. 10**, fundamental switching frequency PWM schemes are developed for **LSF** part of three basic SG-based patterns: 4L-PWM-1 (**Fig. 10(a)**), 4L-PWM-2 (**Fig. 10(b)**), 4L-PWM-3 (**Fig. 10(c)**). In 4L-PWM-1, $SG_1$ is operating at **HSF**, while $SG_2$ and $SG_3$ are at **LSF** which results in four states. Three **LSF** modulation schemes can be obtained based on four fundamental switching frequency states named "11", "10", "01", "00", where the first number is for the leftmost **LSF** SG, while the second number is for the rightmost **LSF** SG. The value "1" or "0" denotes the "ON" or "OFF" state of the associated SGs. Note that for SG-based PWM, all SCs in same SG operate based on same gate signals. In scheme 1, $SG_2$ is ON during [2L, 4L], while $SG_3$ is ON during [3L, 4L]. In scheme 2, $SG_2$ is ON during [3L, 4L], while $SG_3$ is ON during [2L, 4L]. In scheme 3, $SG_2$ is ON when the signal is larger than zero, while $SG_3$ is ON during [3L, 4L] and [2L, 2.5L]. To achieve fundamental switching frequency, scheme 1, scheme 2 or their combination can be applied. For **LSF** parts of 4L-PWM-2 and 4L-PWM-3, the similar PWM can be applied with the simple substitution of associated **LSF** SGs as shown in **Fig. 10(b)** and **Fig. 10(c)**.

For $N$-level SG-based patterns, PWM for $N$-1 **LSF** SGs ($SG_1$~$SG_{N-2}$) can be directly designed based on similar schemes. The signals of associated **LSF** SGs are assigned based on the $N$-2 bits binary number (total number of possibilities is $2^{N-2}$. In fact, to realize fundamental switching frequency modulation, the number of selected states should be three continuous Gray Code (only one binary number is different between any two adjacent codes). If $N$=5 (5L topology), there will be $2^3$ states (i.e. "000", "001", "011", "010", "110", "111", "101", "100"), leading to various fundamental switching frequency schemes, such as a scheme utilizing "111" during [4L, 5L], "110" during [3L, 4L], "100" during [2L, 3L], "000" during [1L, 2L] for $SG_1$~$SG_3$ if they are at **LSF**. For other patterns derived through step two, the similar schemes can be applied for **LSF** SCs. Take 4L-PWM-111 as an example, three states, "11" during [3L, 4L], "01" during [2L, 3L], "00" during [1L, 2L], can be applied for **LSF** SCs. The first number of selected states is for $SC_{11}$, $SC_{12}$, $SC_{22}$, while the second number is for $SC_{31}$.

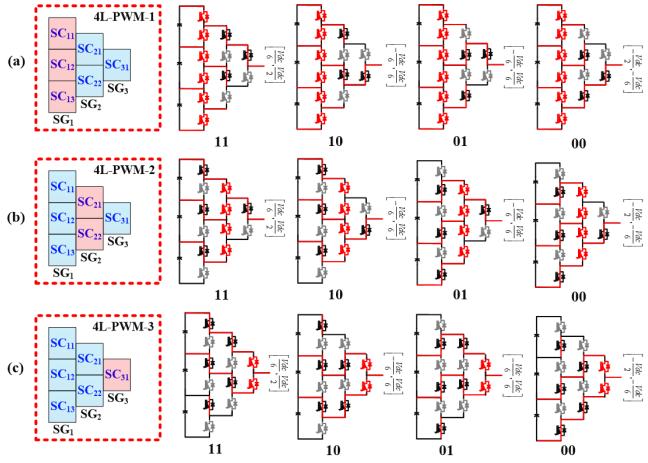

Fig. 10: Fundamental frequency switching PWM under (a) 4L-PWM-1, (b) 4L-PWM-2, (c) 4L-PWM-3.

### *D. PWM design for **HSF** SCs of ANPC (>3L)*

For those PWM patterns with all **HSF** SCs belonging to same SGs under any device utilization patterns, LS PWM can be easily applied. In the simplest case, LS PWM can be applied for the SG-based PWM patterns with only one **HSF** SG. In **Fig. 11**, there are three patterns named as 4L-PWM-1, 4L-PWM-2, 4L-PWM-3, with associated LS PWM. For 4L-PWM-1~3, the SCs within same SGs are assigned the same gate signals. In 4L-PWM-1, the LS PWM is applied for $SG_1$. In 4L-PWM-2, the LS PWM is applied for $SG_2$, and the LS PWM is applied for $SG_3$ in 4L-PWM-3. Note that, for 4L-PWM-2, the possible assignment of $SG_2$ is determined by the **LSF** SCs.

The designed LS PWM can also be implemented for other 4L SG-based patterns with only minor modifications. For 4L-PWM-4, the designed PWM signals of $SG_1$ in 4L-PWM-1 (see **Fig. 11(a)**) and the designed PWM signals of $SG_2$ in 4L-PWM-2 (see **Fig. 11(b)**) can be directly applied for $SG_1$ and $SG_2$ in 4L-PWM-4. While the **LSF** $SC_{31}$ in 4L-PWM-1 and 2 should operate based on the same modulation signals to guarantee proper output. For other patterns derived through design step two, the LS PWM can be designed based on device utilization patterns. Same LS PWM signals are assigned for at least one of the **HSF** SCs that participate in two output adjacent levels.

Moreover, for higher $N$-level ANPC, PWM patterns can be derived through the combination of available ($N$-1)-level ANPC PWM pattern and new PWM for the additional **HSF** SCs in the $N$-level converter. For example, for 4L ANPC, in

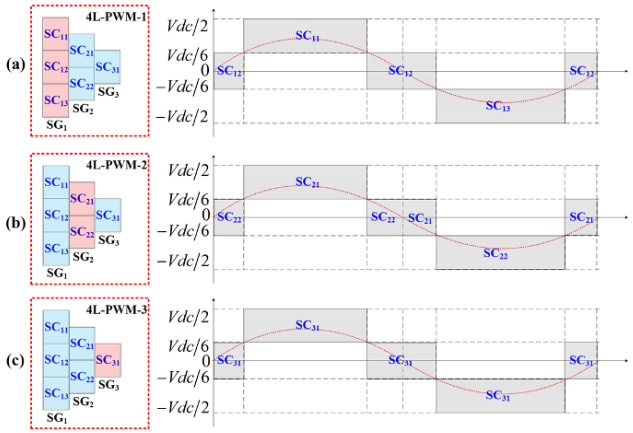

Fig. 11: LS-PWM under (a) 4L-PWM-1, (b) 4L-PWM-2, (c) 4L-PWM-3.

step two, different combinations of 3L ANPC and new **HSF** SCs will be generated. While the 4L PWM patterns can be realized by combining the 3L ANPC PWM patterns (including the PS PWM patterns) with the new **HSF** SCs in the 4L topology. The new PWM for additional **HSF** SCs can be obtained based on device utilization patterns, similar to the design process of SG-based patterns described earlier.

### *E. Demonstration examples of proposed methods*

To further demonstrate the proposed method, the PWM design examples for 4L and 5L ANPC are shown below.

In **Fig. 12**, the derivation process of pattern 4L-PWM-214 is shown based on the decomposition 4-1st-D-2. Three device utilization patterns of 4L ANPC (see **Fig. 7**) are used to determine the specific PWM scheme of 4L-PWM-214. The gating signals of designed carrier-based PWM is shown in **Fig. 13**. The modular PWM is achieved through a combination of PS PWM for 3L ANPC and LS PWM for 4L ANPC. To output [$-V_{dc}/6$, $V_{dc}/2$], PS-PWM is designed for **HSF** SCs ($SC_{11}$, $SC_{12}$, $SC_{21}$) based on an equivalent pattern 3L-PWM-5. To output [$-V_{dc}/2$, $-V_{dc}/6$], LS PWM is designed for **HSF** $SC_{31}$. To realize the same equivalent switching frequency during the whole operation ranges, the carrier frequency for PS PWM is designed to be half of the LS PWM.

In **Fig. 14**, the derivation process of pattern 5L-PWM-335 is shown, which is based on the decomposition 5-1st-D-3. Considering all the device utilization patterns of 5L ANPC, the gating signals of designed carrier-based PWM is shown in **Fig. 15**. The modular PWM is achieved through a combination of PS-PWM for 4L ANPC and LS PWM for 5L ANPC. To output [$V_{dc}/4$, $V_{dc}/2$], LS PWM is designed for **HSC** $SC_{31}$. To output [$-V_{dc}/2$, $V_{dc}/4$], PS PWM is designed for **HSC** SCs ($SC_{22}$, $SC_{23}$, $SC_{32}$) based on an equivalent 4L ANPC with pattern 4L-PWM-6 (see **Table I**). Similarly, the carrier frequency for PS PWM is designed to be half of the LS PWM to realize the same equivalent switching frequency during the whole operation ranges.

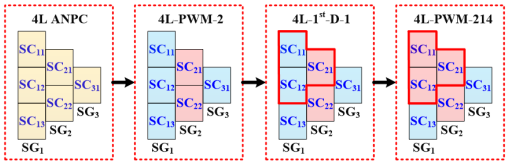


Fig. 12: Derivation of PWM pattern 4L-PWM-214.

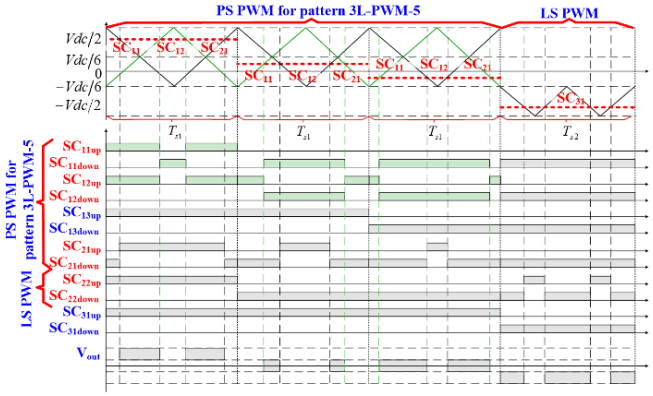


Fig. 13: Modular PWM for 4L ANPC under pattern 4L-PWM-214.

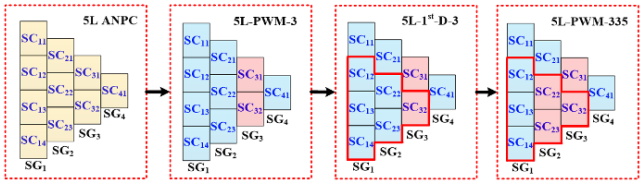


Fig. 14: Identification of PWM pattern 5L-PWM-335.

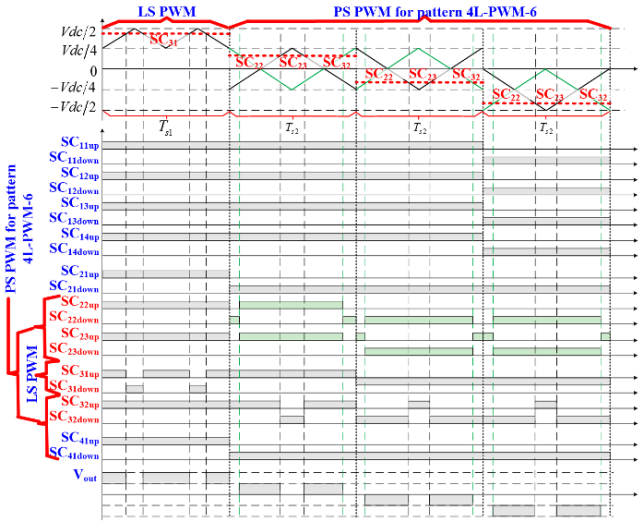


Fig. 15: Modular PWM for 5L ANPC under pattern 5L-PWM-335.

## VI. Experimental Verification

To verify the proposed PWM design method, one phase leg of the 4L ANPC (see **Fig. 16**) is built in the lab, the associated parameters are listed in **Table II**.

TABLE. II
EXPERIMENT PARAMETERS

| Parameters | Experiment | |
|---|---|---|
| | SI | p.u |
| Rated Line voltage | 82 V | 1.0 |
| Rated Power (3 phase) | 0.5 kVA | 1.0 |
| DC-link Voltage | 120 V | -- |
| DC link Capacitors $C_{dc}$ | 4000 uF | 11 |
| Equivalent switching frequency | 960Hz | 16 |
| Carrier frequency for LS-PWM of 4L-PWM-1~3 (case 1~3) | $f_{s1}$: 960Hz | 16 |
| Carrier frequency for modular PWM of 4L-PWM-214 (case 4) | $f_{s1}$: 480Hz<br>$f_{s2}$: 960Hz | 8<br>16 |

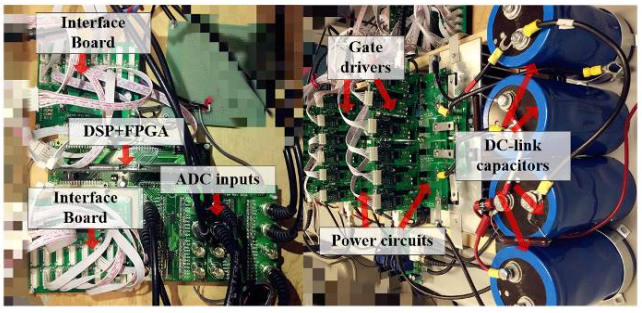


Fig. 16: Single-phase 4L ANPC prototype.

Experiments of four cases (case 1: 4L-PWM-1, case 2: 4L-PWM-2, case 3: 4L-PWM-3, case 4: 4L-PWM-214) are carried out respectively. Based on the proposed method, carrier-based

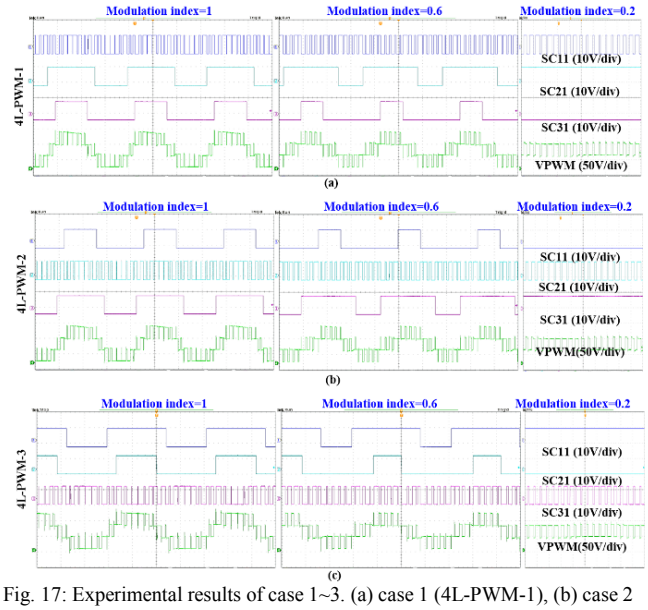


Fig. 17: Experimental results of case 1~3. (a) case 1 (4L-PWM-1), (b) case 2 (4L-PWM-2), (c) case 3 (4L-PWM-3).

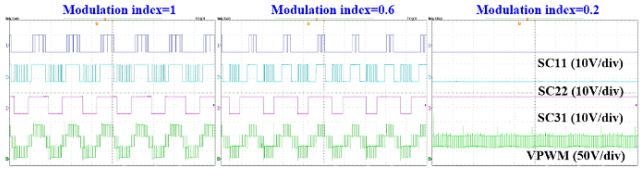


Fig. 18: Experimental results of case 4 (4L-PWM-214).

PWM with fundamental switching frequency PWM can be easily designed for 4L-ANPC based on **Section V. C** and **D**.

For 4L-PWM-1~3, the SCs within same SGs are assigned the same gate signals. In case 1 (4L-PWM-1), the LS-PWM is applied for $SG_1$, while fundamental switching frequency scheme 1 (three states "11", "10", "00" are used as shown in **Fig. 10(a)**) are applied for $SG_2$ and $SG_3$. In case 2 (4L-PWM-2), the LS-PWM is applied for $SG_2$, while fundamental switching frequency scheme 2 (three states "11", "01", "00" are used as shown in **Fig. 10(b)**) are applied for $SG_1$ and $SG_3$. In case 3 (4L-PWM-2), the LS-PWM is applied for $SG_3$, while fundamental switching frequency scheme 1 (three states "11", "10", "00" are used as shown in **Fig. 10(c)**) are applied for $SG_1$ and $SG_2$.

For each case, three modulation indexes (from high to low: 1, 0.6, 0.2) are applied to demonstrate the PWM can guarantee the proper output modulated voltages. As shown in **Fig. 17**, despite of the different assignment of **HSF** SCs and **LSF** SCs, the designed PWM schemes for three PWM patterns have the identical output waveforms during the full operation ranges. For the experiment results of 4L-PWM-214 (see **Fig. 18**), the doubling of equivalent switching frequency can be observed in during output region [$-V_{dc}/6$, $V_{dc}/2$], while designed LS PWM and associated fundamental switching frequency modulation are achieved in the rest region. Due to the modularity of these schemes, simplification of PWM design process and easiness of optimization through PWM combination/rotation can be expected in practical applications.

## VII. Conclusions

This paper proposes a systematic PWM design method for *N*-level ANPC-based converter through hierarchical decomposition and reveals the relationship between topological structures and modulation strategies. Based on the proposed method, modulation strategies for ANPC-based topology with simplified modular PWM, e.g. level-shift PWM, phase-shift PWM and fundamental frequency switching PWM can be systematically realized in a straightforward way. To validate the proposed method, the conventional ANPC converters are hierarchically decomposed into sub-topologies which leads to various PWM patterns. Thereafter, the carrier-based PWM schemes are designed modularly for specific PWM patterns of both 4L and 5L ANPC converters. The experimental results verify the universality of proposed approach.

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