An EMI-Less Full-Bridge Inverter for High Speed SiC Switching Devices

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***Abstract*—To improve the efficiency of inverters used in hybrid cars and electric vehicles (EVs), SiC-MOSFET transistors are used to minimize the switching losses by high-speed switching. However, as the speed increases, surges and ringing occur in the output voltage, and these can cause electromagnetic interference (EMI). In this paper, we study how this issue can be addressed by using a full bridge inverter to suppress common-mode voltages and cancel ringings currents with opposite phase that are generated when driving at high speed. In most cases, one should assume that transistors that are driven simultaneously have slightly different I-V characteristics. Due to this variation, the ringing cannot be completely canceled, resulting in a common-mode voltage. Although this is liable to cause EMI, we also found that if the two transistors are operated close to the point where the maximum switching current occurs, the common-mode voltage fluctuation can be sufficiently suppressed at any current. We analyzed these characteristics in a simulation using a SiC-MOSFET transistor model, and experimentally verified its behavior in a prototype inverter.**

Keywords—EMI; SiC; Inverter; Full-bridge; Common-mode

I. INTRODUCTION

The practical implementation of SiC-MOSFET transistors has made it possible to switch high voltages at high speed. However, since it is impossible to produce electrical circuits with zero parasitic inductance and transistor components with zero parasitic capacitance, steps must be taken to ensure that the EMI noise caused by parasitic resonance is kept within standard tolerances. To this end several methods were proposed [1][2][3] to suppress common-mode voltages, mostly by adding special circuits to cancel them. In this study, we investigated a method that enables high-speed switching while suppressing EMI. Specifically, this method involves using a full bridge inverter to perform switching simultaneously in the positive and negative directions so as to cancel ringing with opposite phases generated in the load. When applied to EVs and hybrid cars, this method should make it possible to simplify or eliminate EMI suppression shielding. Although it requires more inverters than a half bridge inverter, the common-mode voltage that becomes the basis of the EMI can be set to a sufficiently low level so that the total equipment cost including the shield can be reduced.

For this purpose, it is important to use a suitable inverter design so that switching occurs simultaneously and the resulting waveforms are vertically symmetrical. In this paper, we clarify the resonance mechanism in full bridge inverters and show the necessary conditions for the creation of symmetric waveforms, and we present the results of measuring the EMI suppression effect.

II. RESONANCE DUE TO PARASITIC ELEMENTS IN THE INVERTER

A. Prototype full bridge inverter

Fig. 1 shows a schematic diagram in which a two-phase induction motor is connected to our system as a load. Full-bridge inverters are used for purposes such as generating alternating current from a single DC power supply or controlling the directions of drive currents, but are generally not designed to have low EMI emissions. In this study, by making the two constituent half-bridge parts of a full-bridge inverted as electrically symmetrical as possible, we were able to suppress EMI by canceling out the ringing with opposite phases. Fig. 2 shows a prototype designed based on this concept. To reduce the parasitic inductance of the wiring, we used tin-plated copper plate with a thickness of 1.5 mm. For the switching elements, we used SiC transistors (Cree CMF20120D).

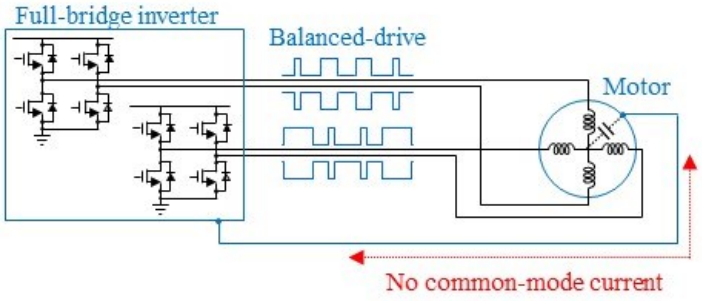


Fig. 1. Balanced-drive inverter system.

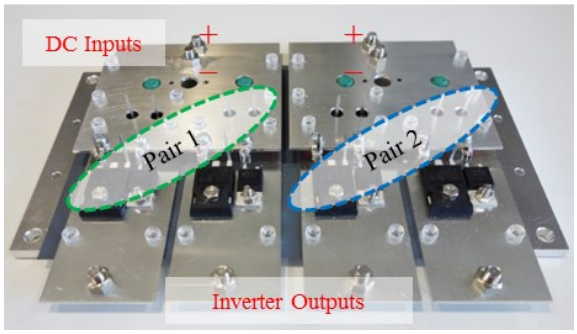


Fig. 2. Prototype inverter with SiC transistors.

Fig. 3 shows the main parasitic components of the prototype inverter. A 1-μF multilayer-stacked ceramic capacitor is inserted between the power supply plates as a snubber to suppress as much as possible the surge currents produced when switching currents flow in parasitic inductors L_P and L_N of the wiring from the power supply to the inverter. One of the causes of parasitic resonance is the drain-source capacitance of the switching transistors (e.g., C_3) and the parasitic inductance caused by the series-connected transistors and diodes, which resonates with the inductance occurring in the snubber capacitor wiring (L_{P2}+L_{3T}+L_{4D}+ L_{N2}+L_S). In our test equipment, this had a resonant frequency of about 40 MHz. Another cause is resonance of the snubber capacitor (C_S) and power supply wiring (L_S+L_P+L_N), which had a frequency of about 250 kHz.

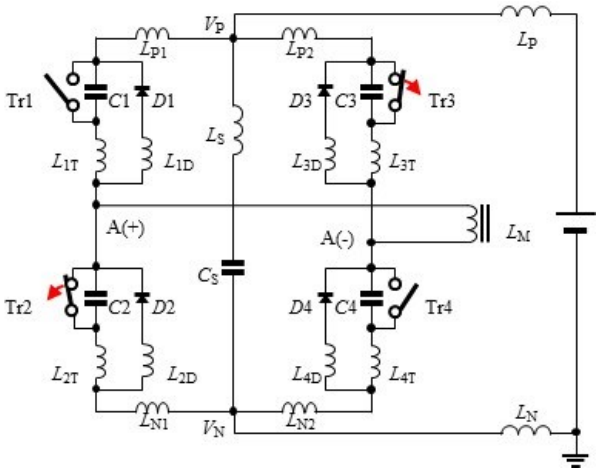


Fig. 3. Full-bridge inverter circuit and parasitic components.

B. *Parasitic resonance measurement result*

Two transistors Tr2 and Tr3 (situated at opposite corners in Fig. 3 were driven at the same time to measure the "off" current I_D and drain-to-source voltage V_{DS} of each transistor, and to observe the difference between the two V_{DS} values in order to measure the common-mode voltage fluctuations shown in Fig. 4. In Fig. 2, Pair 1 is a pair of transistors with matched switching characteristics whose output waveforms are lined up so that the common-mode voltage hardly fluctuates at all (as shown by the red waveform trace in Fig. 4. As a result, there is no danger of EMI occurring. On the other hand, Pair 2 consists of transistors whose characteristics are not matched. In this case, as shown in Fig. 5, there is a discrepancy between the "off" timings of the transistors, and the ringing phases are not mutually opposing. It could be said that the difference in transistor characteristics causes switching to start at different timings, resulting in a change in the shape of the output waveform.

Fig. 4. Inverter output waveforms with good symmetry (Pair 1).

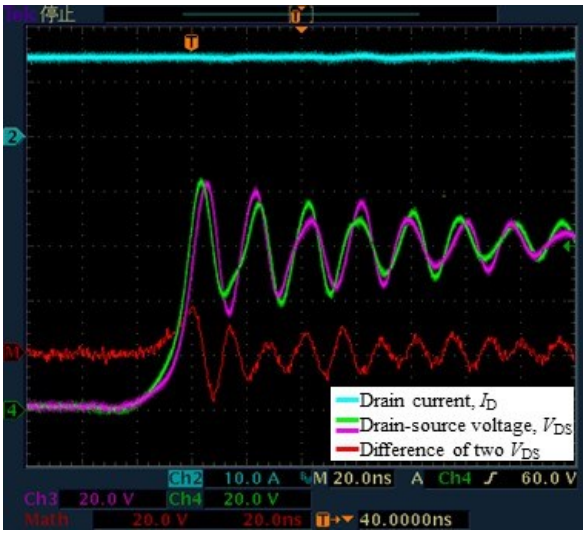


Fig. 5. Inverter output waveforms with poor symmetry (Pair 2).

III. FULL-BRIDGE INVERTER DESIGN GUIDELINES

A. *Effect of parasitic inductance in snubber wiring*

In the ringing caused by parasitic resonance, the components at lower frequencies (here, 250 kHz) have symmetrical output waveforms because only one loop is resonating in contrast to two for high frequencies. On the other hand, for high frequency resonance driven by the drain-source capacitance of the transistors, this period is smaller (about 29 ns), so a discrepancy of a few nanoseconds can have a large effect on the output waveform. Since the prototype inverter uses copper plate to connect the power supply and is built with a sandwich structure including a snubber capacitor, these leads have very low inductance and appear as a short circuit between the power supplies at high frequencies of the order of 40 MHz, resulting in two independent resonance circuits as shown in Fig. 6. However, by matching up the timings at which switching starts, it is possible to create resonance with opposing phases in these two resonance circuits, resulting in the suppression of EMI.

In this case, the snubber capacitor is connected directly in the middle of the left and right legs of the inverter, and the total inductance of the left and right legs must be set to the same value as seen from both ends of the snubber capacitor. This is because if the snubber capacitor is connected at a position offset towards either of the two legs, then the sizes of L_R and L_L in Fig. 6 will be different, and the two resonant frequencies will be different.

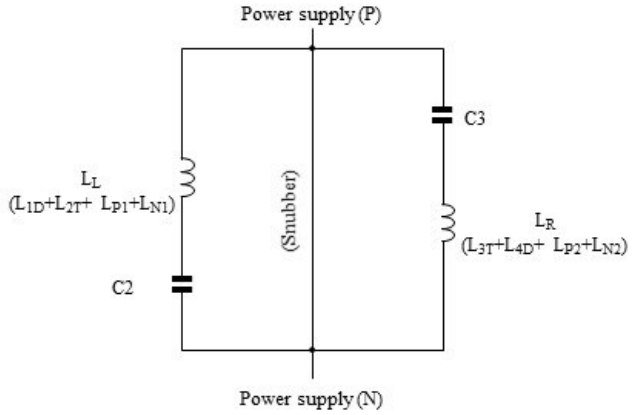


Fig. 6. Equivalent circuit when the parasitic inductance of snubber capacitor is very small.

B. *Effect of gate wiring inductance*

In the simplified circuit of Fig. 6, the parasitic inductance L_G of the gate wiring is unrelated to the resonant frequency, but we have found that it has a large effect on the amplitude of ringing. Fig. 7 shows the output surge voltage amplitude obtained in simulations where L_G was varied from 10 nH to 200 nH. The variation of surge voltage amplitude with L_G is due to the back EMF(electromotive force) produced by L_G. Fig. 9 shows the results of simulations performed to analyze the variation of gate-source voltage V_{GS} with L_G equal to 10 nH and 80 nH. Since we are using discrete SiC-MOSFET transistors, the voltage V_{GS}_Outside acting on the external package leads is not the same as the voltage V_{GS_Inside} acting on the actual transistor chip inside the package (Fig.8). To turn the transistor off, the current that draws away the transistor's input capacitance is about 1 A. With a small inductance of L_G = 10 nH, this back EMF is hardly generated at all, but with a relatively large inductance of L_G = 80 nH, $V_{GS\_Outside}$ instantaneously has a negative voltage due to the back EMF of L_G. As a result, it is thought that the current drawing away the gate charge becomes larger, and the time for which the mirror capacitance formed by drain-gate capacitance C_{DG} is charged becomes shorter so that the transistor turns off faster, resulting in a steeper V_{DS} gradient and a larger surge voltage amplitude. In other words, we found that it was necessary to design the circuit so that transistors driven simultaneously have the same L_G.

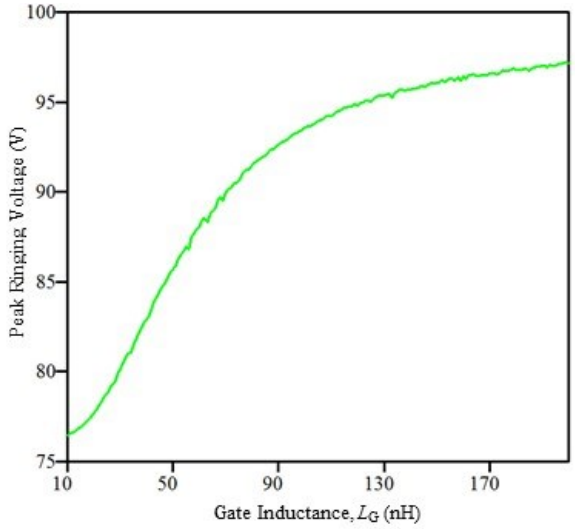


Fig. 7. Relationship between gate inductance and peak ringing voltage.

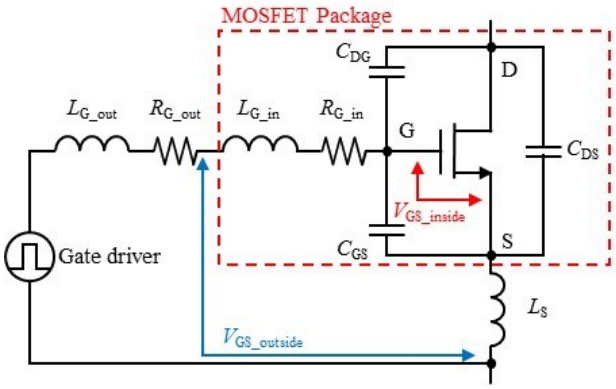
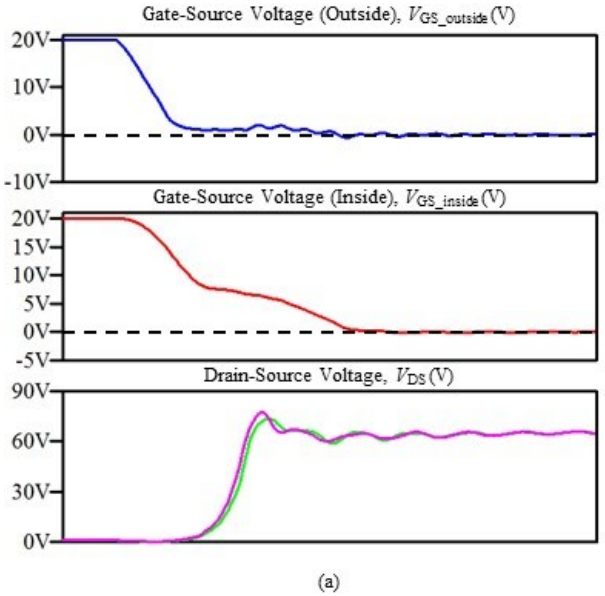
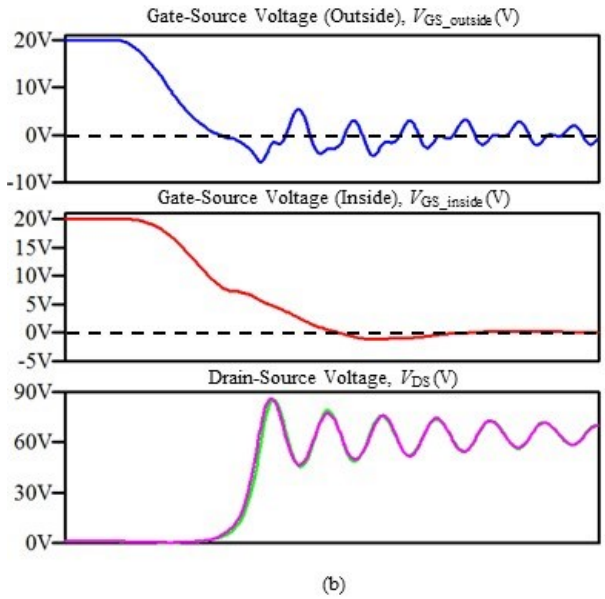


Fig. 8. Parasitic components of gate wiring.



(a)



(b)

Fig. 9. Relationship between gate inductance and surge voltage amplitude, showing (a) Gate inductance L_G is 10nH, (b) Gate inductance L_G is 80nH.

IV. Relationship between Switching Current and Common-mode Voltage

Using a simple Shockley gradual channel approximation to model the relationship between the transistor gate-source voltage and drain current, the transistor turns off at the boundary when the drain current during switching becomes saturated, and is thus expressed as follows:

$$I_D = G\,(\,V_{GS} - V_{th}\,)^2 \tag{1}$$

where G is the transistor's gain factor, V_{GS} is the gate-source voltage, and V_{th} is the threshold voltage. The actual characteristic deviates from this quadratic formula, but this can be used as an approximation.

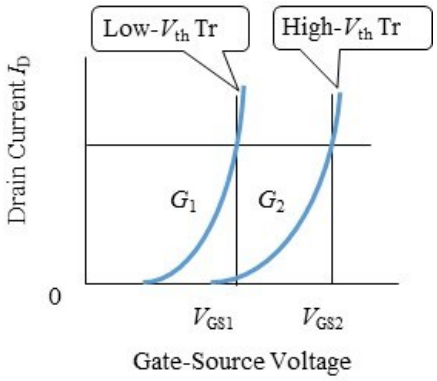


Fig. 10. Drain currents and gate-source voltage.

On the other hand, when the switching characteristics of the two transistors are different, the abovementioned parameters G and V_{th} are different, as are the gate-source voltages V_{GS1} and V_{GS2} needed to achieve the same switching current (Fig. 10).

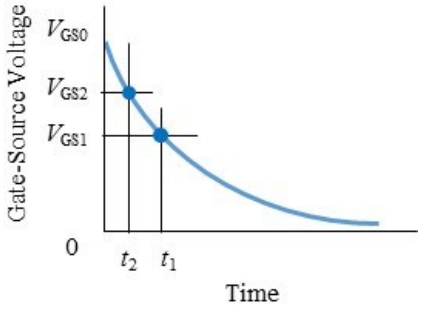


Fig. 11. Gate-source voltage transition and switching timing.

The gate-source voltage, which was V_{GS0} in the "on" state, is attenuated exponentially as shown in Fig. 11 until time t_1 and t_2 when a gate plateau occurs due to the gate-source voltage being driven to the "off" state. If we assume that the gate driver starts driving at time zero, the two transistors with different threshold values start switching at times t_1 and t_2, which are given by the following equations:

$$t_1 = -\,C_{iss} R_G \mathrm{LN}\left(\frac{V_{GS1}}{V_{GS0}}\right) = -\,C_{iss} R_G \mathrm{LN}\left(\frac{\sqrt{\frac{I_D}{G_1}} + V_{th1}}{V_{GS0}}\right) \tag{2}$$

$$t_2 = -\,C_{iss} R_G \mathrm{LN}\left(\frac{V_{GS2}}{V_{GS0}}\right) = -\,C_{iss} R_G \mathrm{LN}\left(\frac{\sqrt{\frac{I_D}{G_2}} + V_{th2}}{V_{GS0}}\right) \tag{3}$$

where C_{iss} is the gate input capacitance, and R_G is the gate resistance. Since the transistors have different characteristics, they switch at different timings separated by the interval Δt_a. Thus,

$$\Delta t = t_1 - t_2 = C_{iss} R_G \mathrm{LN}\left(\frac{\sqrt{\frac{I_D}{G_2} + V_{th2}}}{\sqrt{\frac{I_D}{G_1} + V_{th1}}}\right) \tag{4}$$

The problem here is that even if the timing is adjusted by shifting the gate drive timing by Δt_{set} as shown in Fig. 12, the optimal timing shift changes when the drain current I_D changes.

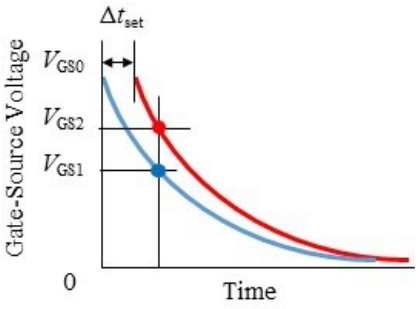


Fig. 12. Switching timing alignment by shifting the start timing.

However, it would be too complicated to control the variation of timing shifts for every switching current value, which is liable to change from one moment to the next. Therefore, by matching the timing when a large current flows, a slight deviation with smaller currents may be tolerated. Given a timing difference of Δt_{set} at a switching current $I_D = I_{set}$, if the same timing difference Δt_{set} is set for all other currents I_D, then the following timing error $\Delta t - \Delta t_{set}$ occurs.

$$\Delta t - \Delta t_{set} = C_{iss} R_G \mathrm{LN}\left(\frac{\sqrt{\left(\frac{I_D}{G_2} + V_{th2}\right)\left(\frac{I_{set}}{G_1} + V_{th1}\right)}}{\sqrt{\left(\frac{I_D}{G_1} + V_{th1}\right)\left(\frac{I_{set}}{G_2} + V_{th2}\right)}}\right) \tag{5}$$

By fitting this formula to our Cree CMF20120D SiC-MOSFET transistors, which typically have a large threshold voltage, we obtained the following values: $G_1 = 2.15 \times 10^{-1}$, $G_2 = 1.70 \times 10^{-1}$, $V_{th1} = 4.1$, and $V_{th2} = 5.1$. Fig. 13 shows the results of calculating the timing error $\Delta t - \Delta t_{set}$ based on these values.

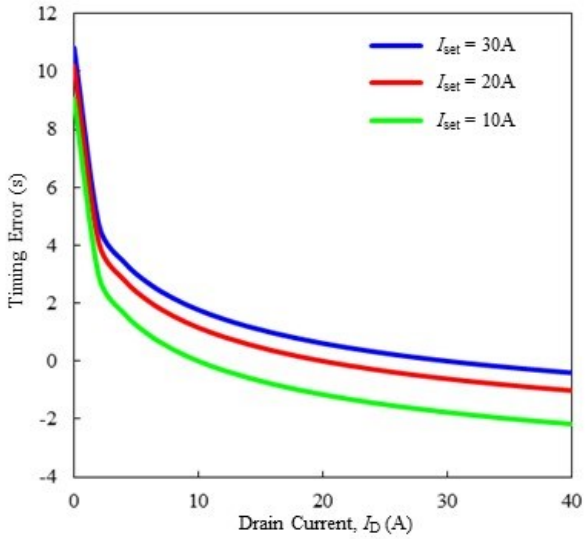


Fig. 13. Relationship between switching current I_D and timing errors.

When the ringing caused by switching the inverter has a period of T, the phase offset between the two ringings is equal to

$$\theta = \frac{2\pi(\Delta t - \Delta t_{set})}{T} \tag{6}$$

where it is assumed that the voltage amplitude of the ringing is proportional to the switching current. This is because when the current is commutated to the diode side, the back EMF generated by the inductance in the resonant loop is proportional to the change of current with time, so if the switching time is always constant, then the back EMF is proportional to the current. If so, when a current whose phase is offset by θ from the current $I_D \sin(2\pi t/T)$ is synthesized, the resulting common-mode voltage V_C is obtained by normalizing I_N as follows:

$$V_c = \frac{I_D}{I_N}\left\{\sin\left(\frac{2\pi t}{T} + \theta\right) - \sin\left(\frac{2\pi t}{T}\right)\right\} \tag{7}$$

The RMS value of this voltage is obtained by squaring and integrating over the period T:

$$V_{CRMS} = \sqrt{\frac{1}{T}\int_0^T V_c^2 \, dt} = \frac{I_D}{I_N}\sqrt{1 - \cos\theta} \tag{8}$$

Fig. 14 shows the results of calculating the RMS value of the common-mode voltage using (6).

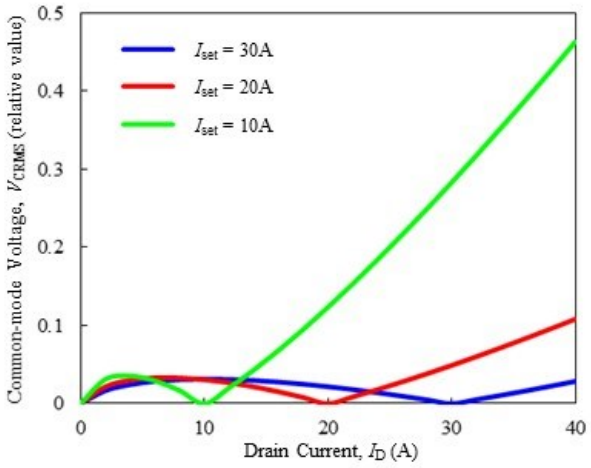


Fig. 14. Relationship between switching current I_D and common-mode voltages.

As this graph shows, when the switching timing is adjusted for a specific current, the calculated common-mode voltage becomes zero at that point, but as the current decreases, some common-mode voltage is generated due to timing errors. However, if the current is reduced, the voltage also decreases automatically, resulting in an upward curve. On the other hand, it can be seen that the common-mode voltage increases sharply when switching currents larger than the timing-adjusted currents.

V. MEASUREMENT RESULTS

A. *Balancing waveforms by timing correction*

Fig. 15 shows the results of measurements made using our prototype inverter to adjust the gate drivers to match the switching timings when driving a 30 A current. The left and right parts of this Figure show the output current waveforms for each current before and after timing adjustment, respectively. With a 60 V supply voltage, the output current is adjusted by performing measurements with a 1.8 mH load coil and by adjusting the on-time of the transistors accordingly. As these results show, we were able to confirm that fluctuation of the common-mode voltage can be suppressed by adjusting the maximum current timing, even when other currents are present.

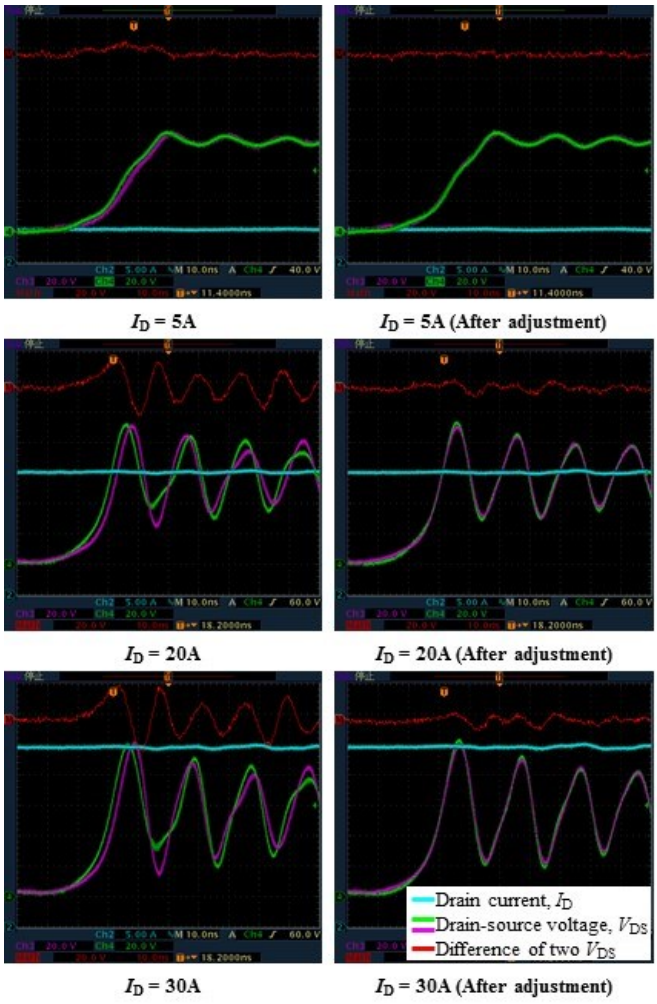


Fig. 15. Experimental comparison of common-mode voltages, showing .

B. *EMI measurements*

We performed EMI measurements by using a 1.8 mH load coil to simulate a motor. The output cables were passed through an anechoic chamber, and measurements were made by setting a probe directly above the cables. For comparison, we performed the same measurements using a half bridge inverter with the same coil load connected between the drain terminal of the inverter's low side transistor and the power supply. As shown in Fig. 16, we confirmed that the proposed full bridge inverter can reduce EMI emissions compared with a half bridge inverter without the common-mode cancellation mechanism.

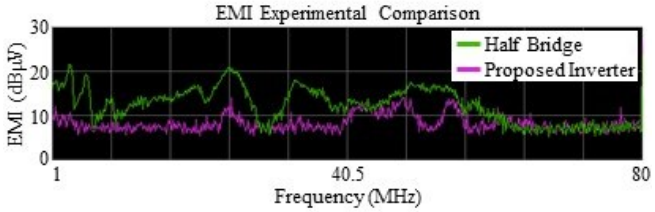


Fig. 16. EMI spectrum comparison for a typical half-bridge inverter and our full-bridge inverter.

VI. CONCLUSIONS

Using a prototype full-bridge inverter, we were able to demonstrate a common-mode voltage cancellation method that cancels out mutually opposite ringings that occur even when driven at high speed. To put this method into practice, we found that it is necessary to design a full bridge inverter that equalizes the inductance of the left and right legs of the inverter. We confirmed that if this inverter is properly designed, then it can suppress common-mode voltage fluctuations by correcting the switching start offset times when switching large currents (even when using transistors with different switching characteristics) so as to match up the output voltage waveforms.

We also clarified that the oscillation waveforms produced during switching also depend on the parasitic inductance of the gate drive circuit. By adjusting the drive timings if the transistor characteristics are mismatched, the switching waveforms can be made symmetrical so that they can be suppressed by common-mode voltage rejection. However, mismatched parasitic inductance in the gate drive circuit wiring can cause different ringing amplitudes at the complementary output terminals of the full-bridge circuit that could not be resolved by timing adjustments. It is therefore important to pay attention to the arrangement and wiring of gate drive circuitry at the design stage.

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