Comparative Investigation of PWM Current-Source Inverters for Future Machine Drives Using High-Frequency Wide-Bandgap Power Switches

Hang Dai and Thomas M. Jahns
Department of Electrical and Computer Engineering
University of Wisconsin-Madison
Madison, WI, USA
Email: hdai23@wisc.edu, jahns@engr.wisc.edu

***Abstract*—Pulse-width-modulated (PWM) current-source inverters (CSIs) in machine drives have received limited research attention since the 1980s because they are generally considered to be inferior to PWM voltage-source inverters (VSIs) in terms of several performance metrics. However, in view of the special features of wide-bandgap (WBG) power semiconductors that distinguish them from today's silicon devices, this paper uses simulation to reexamine the PWM-CSI's key performance metrics including efficiency, electromagnetic interference (EMI), and machine over-voltage at high switching frequencies (e.g., 200kHz) compared with two-level WBG-enabled VSIs under similar operating conditions. Advantages of the CSI compared to the baseline VSI topology are revealed for each of these three performance features. Reverse-voltage-blocking switches based on gallium nitride (GaN) High Electron Mobility Transistors (HEMTs) that are key to the operation of PWM-CSIs are discussed and experimentally evaluated.**

Keywords — Current-source inverter; voltage-source inverter; motor drive; wide bandgap semiconductors; electromagnetic interference

I. INTRODUCTION

Three-phase current-source inverters (CSIs) played a critical role during the early days of solid-state power electronics. During the 1960s and 1970s, thyristor-based CSIs dominated the available power converters, primarily in the forms of load-commutated inverters (LCIs) [1] and auto-sequentially commutated inverters (ASCIs) [2]. The development of MOS-gated power semiconductors during the 1980s including IGBTs and power MOSFETs made it possible to reach much higher PWM switching frequencies. However, unlike thyristors, the MOS-gated power devices cannot block reverse voltage, making them more suitable candidates for voltage-source inverters (VSIs) than the CSIs that dominated motor drives at that time (Fig. 1). As the performance characteristics of IGBTs and power MOSFETs improved, CSIs eventually lost their competition with VSIs for machine drive applications at all power levels less than several MWs [3].

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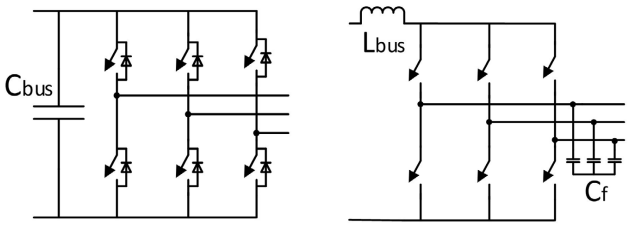

Fig. 1. Basic inverter topologies of three-phase inverters: a) VSI; b) CSI

Today, more than 30 years later, new wide bandgap (WBG) power semiconductors fabricated using both silicon carbide (SiC) and gallium nitride (GaN) are becoming available that can switch more than 10 times faster than their silicon-based counterparts. However, when attempts are made to use these WBG devices as drop-in replacements for silicon-IGBTs in VSI machine drives with PWM switching frequencies higher than dozens of kHz, vexing problems caused by their much higher switching frequency and *dv/dt* values have emerged, including machine terminal over-voltages and significantly elevated electromagnetic interference (EMI) levels [4][5].

The purpose of this paper is to investigate the application of WBG power switches to PWM-CSIs for machine drive applications, and to compare their performance metrics to PWM-VSIs that also use WBG power switches. Key performance metrics of WBG-enabled PWM-CSIs operating at 200kHz are evaluated and compared to those of WBG-enabled PWM-VSIs at 200kHz both with and without inverter output filters. Suitable GaN-based power switch configurations that can block reverse voltage are identified and experimentally evaluated.

II. PERFORMANCE COMPARISONS BETWEEN CSI AND VSI

A. Design of CSI and VSI for 200kHz Operation

For comparing the performance metrics of the CSI and VSI, it is assumed that they are both designed to excite the same wye-connected 3 kW ac machine at its rated operating point: 230 Vrms line-to-line and 7.6 Arms phase current.

As shown in Fig. 1, the VSI has a dc-link capacitor for voltage stabilization and anti-parallel diodes (either intrinsic or extrinsic) across each power switch to provide paths for reactive and regenerative current. In contrast, the CSI has a dc-link inductor to provide stiff inductor current. The 6 CSI switches conduct current unidirectionally and are required to block reverse voltages. The CSI's three output filter capacitors C_f are needed to provide a buffer between the inductances in the dc link and motor phases, in addition to providing a filtering function at the inverter's output terminals [6]. This section discusses some of the key component design features that are essential for the CSI and VSI, respectively.

The CSI's dc-link inductor must be designed to deliver dc current to the inverter input with low current ripple to enable the inverter's PWM algorithm to accurately regulate the amplitude and the waveforms of the three phase currents. Based on [7], an approximate expression for the required dc link inductance L_{bus} is presented as

$$L_{bus} = \frac{\sqrt{3}U_{ph}}{4f_{sw}\Delta i_{dc\text{-}pp}} \tag{1}$$

where U_{ph} and $\Delta i_{\text{dc-pp}}$ are the phase voltage and maximum allowed current ripple (designed to be around 10% of the rated phase current), respectively, and f_{sw} is the switching frequency.

In addition to the current ripple constraint, the dc-link inductor should be able to suppress the overshoot current during sudden load change conditions. With a command feedforward method implemented, the worst-case overshoot current for inductor-sizing purposes occurs when the converter is operating at rated current and the inverter-side dc-link is short-circuited. The corresponding minimum value of dc link inductor L_{bus} can be expressed as [7]

$$L_{bus} = \frac{1.5U_{ph}}{f_{sw}(I_{dc\text{-}max} - I_{dc\text{-}rated})} \tag{2}$$

where $I_{dc\text{-}max}$ is the peak allowable dc link current following the short-circuit application, and $I_{dc\text{-}rated}$ is the rated dc link current assumed to be flowing prior to the short circuit event.

A general guideline for designing the CSI's output filter capacitors C_f is to limit the line-to-line voltage ripple to not exceed 5% of the machine's rated line-to-line voltage. The resulting expression for the minimum value of C_f is

$$C_f = \frac{I_{dc\text{-}rated}}{4f_{sw}\Delta V_{cf}} \tag{3}$$

where ΔV_{cf} is the maximum allowable voltage ripple across the capacitor[7].

As can be seen in (1) - (3), the passive component values decrease inversely as the switching frequency is increased. This is an important characteristic of the PWM-CSI when operated at high switching frequencies. To clearly illustrate this trend, the passive component values are plotted as function of the PWM switching frequency f_{sw} in Fig. 2. As shown, the required dc-link inductance drops significantly as the switching frequency is increased. When f_{sw} is 10kHz or less, which is typical for silicon IGBTs in motor drives, the required inductances are typically bulky and lossy. However, if the

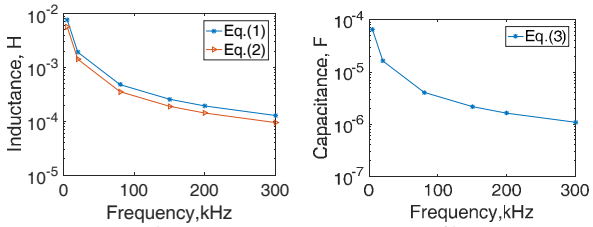

Fig 2. CSI passive components' variations to switching frequency a) dc-link inductor; b) output capacitor filter (U_{ph}=132Vrms, $I_{dc\text{-}rated}$=12.2A , $\Delta i_{dc\text{-}pp}$=1.5A , $I_{dc\text{-}max}$=22A , ΔV_{cf}=12V)

switching frequency is increased to 200kHz by introducing wide bandgap power switches, the required dc link inductance and filter capacitance values drop by a factor of 20, resulting in inductors and capacitors that are much more compact with lower losses. These mass, volume, and loss reductions for L_{bus} and C_f are critical to designing PWM-CSIs that achieve both high efficiency and high power density.

For the VSI in Fig. 1a, the only passive component in the core inverter that needs to be designed is the dc-bus capacitor C_{bus}. One requirement for this capacitor similar to the CSI's dc-link inductor is to provide nearly constant voltage (i.e., low voltage ripple) at the inverter input terminals to make it simpler for the PWM algorithm to produce high-quality output voltage waveforms. In [8], the C_{bus} capacitor is designed to meet the voltage ripple limitation, leading to the conclusion that the required capacitance ideally decreases inversely with switching frequency increases, similar to the relationship discussed previously for L_{bus} in the CSI. However, in many cases, the ripple current that must be handled by the dc link capacitor stays nearly constant despite increases in f_{sw}. When electrolytic capacitors are chosen for C_{bus}, it is often the case that the ripple current handling requirements dominate the capacitance value selection, partly or completely offsetting the advantages of increasing f_{sw} [9].

In addition to controlling the voltage ripple, the bus capacitor serves several other important roles including energy buffering, PWM ripple current filtering, transient peak load support, and input current harmonic bypassing [10]. As a result, it is typically necessary to design these capacitors on a case-by-case basis using combinations of closed-form analysis, simulations and experiments [11]. Since an optimized VSI dc-bus capacitor design is not the focus of this paper, interested readers are referred elsewhere for more information such as [12] which presents a sizing method based on consideration of both the voltage and current ripple limitations.

In some applications, there are dc bus ride-through requirements for the dc bus that make it possible for the inverter to continue operating many fundamental cycles after loss of the inverter's power supply. Ride-through requirements can dominate the sizing of the dc bus components in some cases, causing their values to be governed by the fundamental frequency instead of the switching frequency. This important issue is beyond the scope of this paper.

For the switches, a SiC power device has been selected for both the CSI and VSI in this comparative study. This choice

TABLE I. SUMMARY OF THE DESIGNED CSI AND VSI

Description	WBG-CSI	WBG-VSI
3-phase load ratings	3-phase balanced, 3 kW, 230 Vrms l-l, 7.6 Arms	
Fundamental frequency	150 Hz	
Switching frequency	200 kHz	
Rated dc bus voltage	N/A	325 Vdc
Rated dc bus current	12.2 Adc	N/A
Switches	SiC FET, 1200 V, 90 A C2M0025120D (Cree) (2/sw., common-source)	SiC FET, 1200 V, 90 A C2M0025120D (Cree)
Filter capacitor	1.628 uF, ceramic	N/A
DC bus	250 µH MPP-cored inductor	15 µF film capacitor
Modulation method	Current SVPWM	Voltage SVPWM

was influenced by the lack of suitable GaN-HEMT device models that are used later for the efficiency simulations. Since the CSI requires power switches that can block reverse voltage, and the SiC devices do not provide this capability, two SiC devices are connected in a common-source configuration for each inverter switch to provide this feature. A more detailed discussion of the CSI switch is presented in Section III.

TABLE I summarizes the resulting designs of the 3 kW CSI and VSI used in the following comparisons.

B. EMI Comparison

With increased switching frequency of motor drives, the effects of parasitic inductances and capacitances existing in WBG-based motor drive systems become more pronounced than they are in conventional silicon-based motor drives. The high switching frequency combined with the parasitics leads to increased EMI levels for VSIs, as explored in [5][13].

Schematic diagrams identifying the dominant parasitic components in VSIs and CSIs are shown in Fig. 3, which is similar to schematics found in previous literature such as [5]. The parameters of the cable are obtained from the high-frequency cable equivalent circuit presented in [14], and the motor model has been obtained from [5] and [15].

EMI is usually classified as conducted EMI or radiated EMI. Since radiated EMI can be easily suppressed by shielded

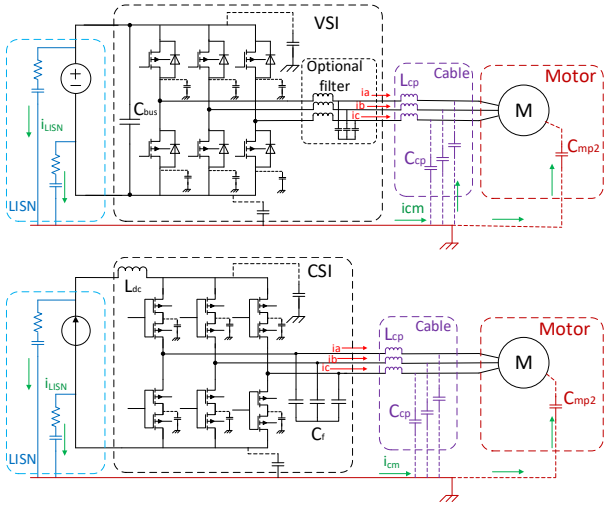

Fig. 3. EMI and efficiency simulation circuits for VSI and CSI including machine drives parasitic inductances and capacitances.

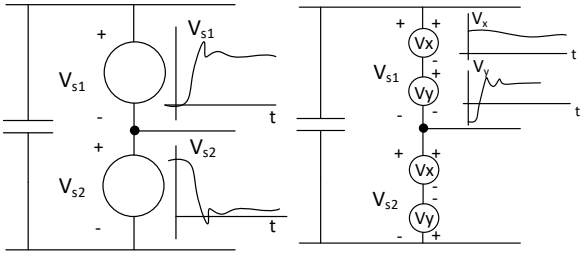

Fig. 4. Conducted EMI voltage generation during switching transient for 2-level VSI, with switch voltages V_{s1} and V_{s2} in left circuit segregated into differential-mode (V_x) and common-mode (V_y) components in right circuit.

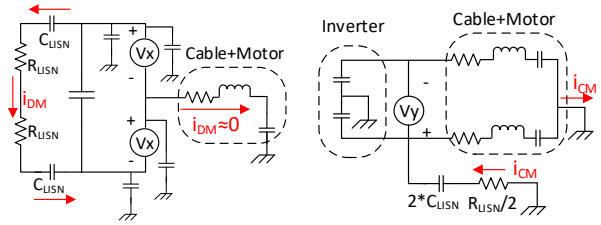

Fig. 5. VSI equivalent circuit identifying the current path for differential-mode (DM) EMI current (left) and common-mode (CM) EMI current (right)

cables and housings in the motor drive system, conducted EMI is the primary focus in this paper. Within the conducted EMI class, there is conducted common-mode EMI (CM EMI) and differential-mode EMI (DM EMI). Simple schematics highlighting the generation of CM and DM EMI in the VSI topology presented in Fig. 3 are illustrated in Fig. 4 and 5. As seen in Fig. 4, the voltage across the upper switch during the switching transient is rising to the dc bus level, while the lower switch's voltage is reducing to zero volt. According to the definition of DM (V_x) and CM (V_y) voltages in (4) and (5), an equivalent circuit can be drawn in Fig. 5.

$$V_x = \frac{(V_{s1}+V_{s2})}{2} \quad (4) \qquad V_y = \frac{(V_{s1}-V_{s2})}{2} \quad (5)$$

As can be observed in Fig. 5a, the resulting DM EMI current i_{DM} flowing into the motor is nearly zero. In contrast, the CM voltage combined with the motor and cable's parasitics can generate significant CM current that flows into the motor. Therefore, conducted CM current plays a dominant part in VSI motor drives' EMI frequency spectrum, as verified in [13]. In addition, since CM conducted current is more dependent on the parasitics of the motor drive system, it can cause other serious issues including ground leakage current and motor bearing failure. For the CSI, a similar equivalent circuit analysis reveals similar conducting current paths for CM and DM currents . Therefore, this paper will focus on conducted CM EMI as the basis for a comparison between the VSI and CSI.

The generic CM EMI equivalent circuit for both the CSI and VSI is shown in Fig. 6. Since the line impedance stabilization network (LISN) is effectively a series connection of a coupling capacitor and a resistor, and the CM EMI is mainly achieved via parasitic capacitors, the impedances shown in Fig. 6 are capacitive. Thus, because the coupling capacitances of the inverter to ground are much smaller than

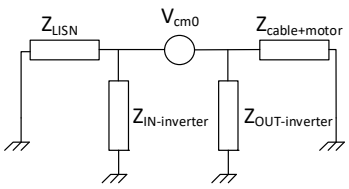

Fig. 6. Simplified equivalent circuit for motor drive conducted CM EMI.

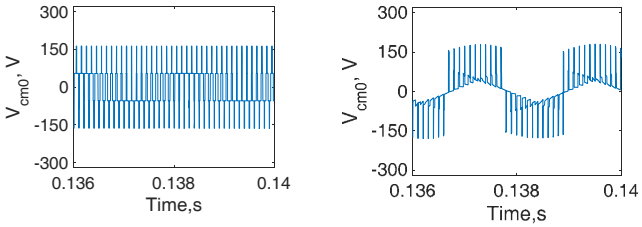

Fig. 7. Simulated common-mode voltage source (V_{cm0}) generation of VSI (left) and CSI (right) at 10 kHz switching frequency.

those of the LISN, cables, and motor, the $Z_{IN\text{-}inverter}$ and $Z_{OUT\text{-}inverter}$ impedances can be ignored in the simulation.

In Fig. 6, V_{cm0} is the CM EMI voltage source generated by the switching transient identified in Fig. 4, which is different from the CM EMI voltage (CMV) measured across the LISN resistor in Fig. 5 that is used for comparisons among different inverter topologies. Fig. 7 shows the simulation results for V_{cm0} in the VSI and CSI. It can be observed that the VSI's V_{cm0} switches between $V_{dc}/2$ and $-V_{dc}/2$ continuously, while the CSI's V_{cm0} switches between 0 and $V_{dc}/2$ for 1/6th of the fundamental cycle, and between 0 and $-V_{dc}/2$ during the next 1/6th of the fundamental cycle. According to the equivalent circuit, a higher V_{cm0} will likely result in a higher CM EMI level. Therefore, the CSI has a more benign CM source compared to the VSI due to its lower source voltage amplitude. For clearer observation, a 10 kHz switching frequency was chosen for the waveforms in Fig. 7. The basic charac-teristics remain the same at higher switching frequencies.

The CMV can be measured experimentally using a CM/DM separation circuit after measuring the voltage across the LISN resistor. In simulations, that CMV can be easily calculated using (6) and (7).

$$I_{cm} = \frac{I_a + I_b + I_c}{3} \tag{6}$$

$$CMV = I_{cm} \cdot R_{LISN}/2 \tag{7}$$

Fig. 8 shows simulation results comparing the conducted CM EMI (CMV) frequency spectra of the CSI and VSI (with and without an output filter) for a switching frequency of 200 kHz. The 150kHz to 30 MHz frequency range in Fig. 8 corresponds to the regulated range for EMI standard CISPR 11 [16]. The CSI generates significantly lower conducted CM EMI compared to the VSI without an output filter, particularly at high frequencies. In addition to the reduced V_{cm0} discussed above, the dc-link inductor L_{bus} serves as a low-pass filter that acts to suppress the CM EMI current. The higher the CM current's frequency, the more effective the inductor filter is for minimizing the corresponding current amplitude.

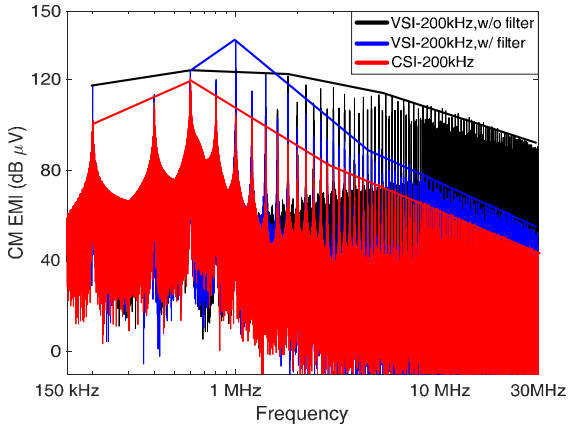

Fig. 8. Simulated comparison of conducted common-mode EMI (CMV) for CSI and VSI with/without optional output *LC* filter (see Fig. 3) for f_{sw}=200 kHz.

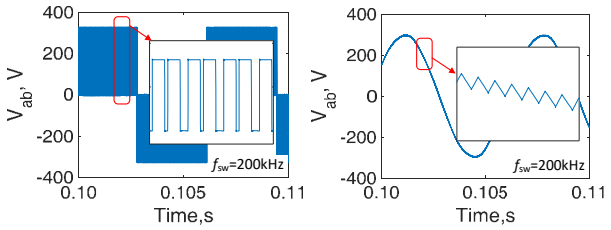

Fig. 9. Simulated output line-line voltage of VSI (left) and CSI (right).

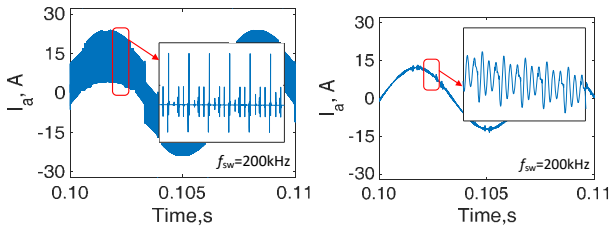

Fig. 10. Simulated output phase current of VSI (left) and CSI (right).

C. *Efficiency Simulation*

One promising aspect of WBG devices is their low switching and conduction losses that open opportunities for designing power converters with higher efficiencies compared to those based on Si devices. There are published papers that document successful applications of WBG devices in dc/dc power converters that have resulted in efficiency increases at high switching frequencies [17]. However, VSI-based motor drive systems differ from dc/dc converters because they typically require long multi-phase cables that apply ac waveforms to electric machines consisting of high-frequency PWM voltage pulses, in contrast to the dc voltage output of dc/dc converters.

As shown in Fig. 9, the line-to-line output voltage of a VSI (without output filter) consists of a series of voltage pulses rising from 0 to the positive or negative dc bus levels, while the CSI's output line-to-line voltage is nearly sinusoidal with minimal ripple voltage due to the filtering effect of L_{bus} and C_f discussed above. Due to capacitive parasitic coupling, the impedance of the motor winding decreases as the excitation frequency increases, and the motor load behaves effectively as an *LCR* network that is exposed to large numbers of switching

transients with very fast rise and fall times [18]. Because of the very high *dv/dt* values generated by WBG switch devices as well as their inherent low output C_{oss} , high-amplitude lightly-damped parasitic ringing commonly occurs. In addition, if the cable length between the drive unit and the motor system is increased beyond several meters, there will be even higher capacitive parasitic coupling that further aggravates the ringing. The combined effects of these features can result in higher switching losses for WBG-based VSIs when they are implemented in motor drives than expected based on the loss data extracted from double-pulse tests [18].

Fig. 10 provides the simulated phase current waveforms for the VSI (without output filters) and the CSI based on the equivalent circuits shown in Fig. 3 that include the major parasitic capacitances and inductances. PLECS loss simulation is employed where the loss data of switching devices are obtained from device manufacture's experiments and stored in a look up table. Reflecting the impact of the circuit parasitics in the absence of an output filter, the VSI's terminal phase current waveforms exhibit many current spikes that accompany the regulated fundamental component. This phenomenon has been observed in experimental VSI units, as shown in [19][20]. Closer examination of the simulation results confirms that these current spikes are attributable to the parasitic capacitances. Since they are aligned with the device switching events, they can induce significant additional inverter losses that increase with f_{sw}.

In contrast, the CSI's simulated terminal phase current does not exhibit any current spikes because of the C_f output capacitors. In fact, the phase current waveform is high quality with minimal PWM ripple because of the high value of f_{sw} (200 kHz). The phase current and voltage waveforms at the VSI output terminals can be improved to nearly match those of the CSI if *LC* filters are added at each output terminal, provided that the extra mass, volume, and cost of these filters is acceptable. Due to space limitations, the results for VSI with output filters are not shown here.

Fig. 11 presents the calculated efficiencies of the CSI and VSI (with and without output filter) using the simulation results. These results predict that the efficiency of the VSI without output filter drops significantly because of the increased switching losses caused by the interaction of the extremely fast voltage switching transients and the parasitic components. In contrast, the predicted inverter efficiencies for the CSI and VSI with output filter are close to each other and significantly higher, exceeding 98%. It is recognized that the accuracy of these predicted efficiency values depends heavily on the quality and fidelity of the simulation model. Work is under way to experimentally verify these predicted values.

D. Overvoltage Issue

The risk of creating high over-voltages at machine terminals due to fast voltage switching transients has been recognized for many years since the introduction of silicon IGBTs and power MOSFETs [21]. Since the machine cables and the machine itself exhibit transmission line characteristics when exposed to fast *dv/dt* values, substantial line-to-line over-voltages exceeding the VSI bus voltage can be developed at the machine terminals due to well-known reflection phenomena. The risk of these overvoltages is known to increase as the machine cable length increases.

A simplified schematic helpful for explaining the impact of PWM voltage pulses on the machine and its cables is shown in Fig. 12. As explained by [4], the reflected overvoltage can be roughly calculated under two cable length conditions. An important parameter named critical cable length l_c is defined in (8), where t_r is the PWM voltage pulses' rise time and c is the speed of light. If motor drive's cable length (l) is lower than the critical cable length, the maximum overvoltage is calculated by (9) [21]. On the other hand, if the cable length is longer than the critical cable length, then according to transmission line theory, the overvoltage is calculated based on impedance matching in (10) and (11).

$$l_c = \frac{\lambda}{4} = \frac{c \cdot \pi \cdot t_r}{4} \tag{8}$$

$$V_{\text{motor-end pu}} = 1 + \sin\left(\frac{l}{l_c} \cdot \frac{\pi}{2}\right) \tag{9}$$

$$V_{\text{motor-end pu}} = (1 + \Gamma) \cdot V_{\text{incident}} \tag{10}$$

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{11}$$

The overvoltage calculated by the above two cases only considers one-time reflection of the PWM voltage pulses. If the time duration between two voltage pulses is less than the oscillation period for reflected waves, the second pulse's effect will add to the first one. As a result, the combined voltage peak can be 3 to 4 times higher than the dc bus voltage. This phenomenon is described as "double-pulsing" [4].

Ringing of the drive system due to resonances of the parasitic components can further exacerbate the overvoltage peak values. More specifically, this ringing is typically attributable to the inductance and capacitance of the cable. The interaction of the machine, cables, and inverter generates resonant circuits that can cause the voltage pulse edges to be

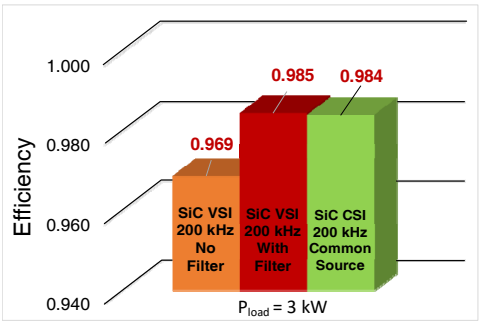

Fig. 11. Calculated efficiencies of CSI and VSI (with and without output filters) based on simulation using Fig. 3 equivalent circuits with f_{sw} = 200 kHz.

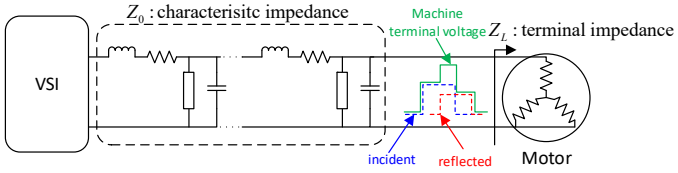

Fig. 12. Simplified machine drive equivalent circuit to explore over-voltages.

amplified, creating underdamped ringing voltage waveforms.

A technical report published by ABB in 1997 shows that the voltage pulses from the VSI and its resultant overvoltage can lead to significant reduction of motor winding's insulation life [22]. According to this report, increasing the switching frequency from 3kHz to 12kHz can lead to approx. 10x reduction of insulation life.

The introduction of WBG devices in place of the silicon switches can aggravate these undesirable voltage stress issues due to the combined effects of increased switching frequency and lower rise/fall times of voltage pulses. For example, the critical cable length can be significantly reduced due to reduced voltage rise/fall times t_r , making it possible to generate serious over-voltages with much shorter cables. The high switching frequency of WBG-based VSIs is also typically accompanied by reductions in the minimum time spacing between adjacent pulses, increasing the risk that the "double-pulsing" phenomenon can occur more frequently.

As noted during the preceding EMI and efficiency discussion, addition of VSI output filters can prevent the sharp voltage edges from reaching the machine cables, thereby suppressing the over-voltage risk. However, the same trade-offs with filter mass, volume, and cost must be evaluated. The EMI, efficiency, and overvoltage issues highlight the natural advantages that the CSI topology provides for WBG-based machine drives with high switching frequencies.

III. Development of Reverse-Voltage-Blocking Switches Based on GaN-HEMT WBG Devices

A. Semiconductor Switch Requirement for CSI and VSI

As noted in the introduction, the basic features of silicon MOS-gated power switches played a key role in shifting the motor drive industry from CSIs to VSIs which continue to dominate today's motor drive market. Fig. 13 shows simulation results for the voltage and current waveforms across each switch in both VSIs and CSIs. A lower switching frequency of 10kHz has been chosen to make the PWM details more visible. As can be seen, the voltage across VSI's switch is unidirectional while the current must be able to flow bi-

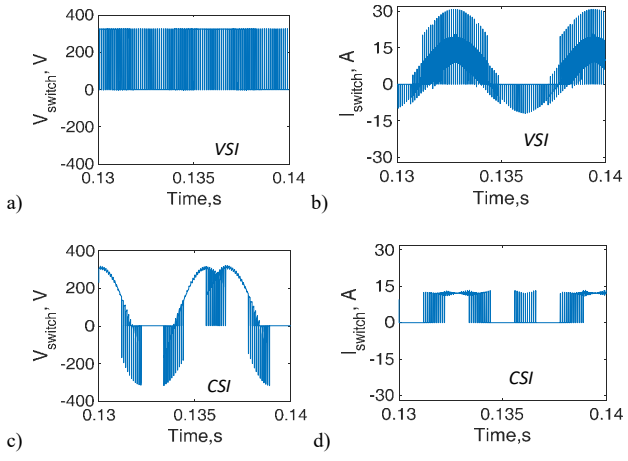

Fig. 13. Simulation results showing typical waveforms for the VSI switch's: a) voltage; and b) current; and CSI switch's: c) voltage; and d) current.

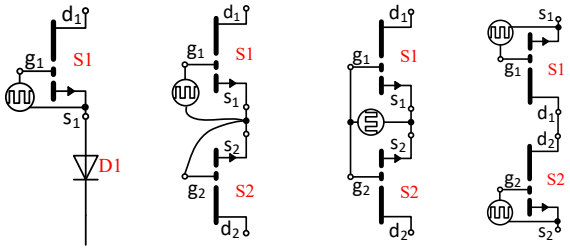

Fig. 14. Alternative discrete switch configurations using GaN-HEMTs to achieve reverse-voltage-blocking capability required by PWM-CSI

directionally. In contrast, the duality features of the CSI reverse the switch requirements to be bidirectional voltage blocking and unidirectional current for each CSI switch.

Power switches in the thyristor family can be designed to block voltages in both polarities, but, with the exception of the low-power triacs, they conduct current only in one direction. These features make them natural candidates for CSIs that dominated motor drives in the early days of solid-state power electronics, and they continue to survive today in some high-power (>1 MW) motor drives today. In contrast, silicon IGBT (with anti-parallel diode) and MOSFET can conduct current bidirectionally while only can block voltage in the forward direction. These features make them well-suited for VSI applications. Their much faster switching speeds were far superior to those achievable with thyristors for use in PWM-based inverters, causing the market to eventually abandon CSIs in nearly all motor drive applications in favor of VSIs.

The emergence of new WBG devices makes it important for researchers to ask which inverter topologies are best suited to their natural features. As discussed in Section II, applying WBG switches as drop-in replacements in conventional VSIs raises some significant complications in the areas of EMI, efficiency, and over-voltage. In contrast, the CSI topology appears to offer some appealing advantages in each of these categories. However, because of the dominance of VSIs for the past three decades, switch development for CSIs has received very little attention. As a result, there are very few commercially-available monolithic power semiconductor devices that provide the required combination of reverse-voltage blocking, fast switching speeds, and low conduction loss capabilities that are required for competitive CSIs. Therefore, this section examines alternative approaches for using commercially-available WBG switches that are suitable for use in high-performance CSIs.

B. Reverse-Voltage-Blocking Switch Configurations

Since there are no monolithic reverse-voltage-blocking

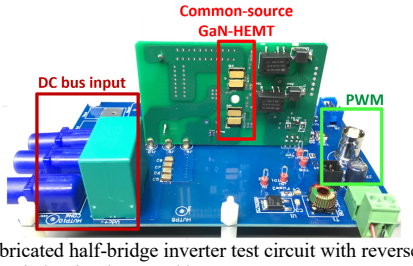

Fig. 15. Fabricated half-bridge inverter test circuit with reverse-voltage-blocking switches implemented by common-source-connected GaN-HEMTs.

(RVB) switches that have comparable switching performance as new WBG devices or even state-of-the-art silicon MOSFETs and IGBTs, available discrete WBG devices were investigated as the basis for implementing these switches. Due to space limits, attention is focused on using GaN-HEMT devices as the building blocks for the RVB switch. Four possible configurations are identified in Fig. 14. In Fig. 14a, the GaN-HEMT is in series with a diode and it solely depends on the diode to block the entire reverse voltage. This configuration is simple and effective, and has already been used in some previously documented PWM-CSI units [7][23]. However, the conduction loss of the series diode is significant, reducing its attractiveness for high-performance CSIs.

For the configuration in Fig. 14b, the lower GaN-HEMT's gate is shorted to its source in order to simplify the gate drive design. The motivation for this is to take advantage of GaN-HEMT that it will behave like a diode when V_{gs} equals 0 and the current is flowing from its source to drain. This characteristic has been used in many GaN-HEMT-based VSI topologies to provide a reverse-conducting channel during the deadtime [24]. However, experiments have revealed significant voltage drops and troublesome oscillation issues in this configuration [25].

The configuration in Fig. 14c uses one gate drive to control two source-connected GaN-HEMTs simultaneously. When forward conducting, the voltage drop of the two switches will be nearly the same due to the GaN-HEMT's symmetric conducting channels for both current polarities when $V_{gs}>V_{th}$. When the gate voltage is zero, the lower switch will block any reverse voltage up to its voltage rating. This configuration has previously been examined in [26] to configure switches that are suitable for bidirectional switching.

The last configuration shown in Fig. 14d has two GaN-HEMTs connected in common-drain configuration and needs two gate drives be synchronized with each other. One benefit of this configuration is that if it is converted into a monolithic RVB devices, the two connected drains correspond to a single shared drift region in the monolithic version. Therefore, the on-state resistance of the monolithic common-drain switch in Fig. 14d can be smaller than that of Fig. 14c when achieving the same reverse-voltage blocking capability.

C. Simulation and Experiment Results

To simplify the gate drive design as well as to provide low

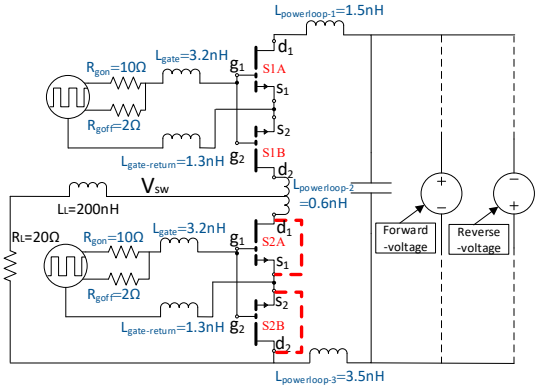

Fig. 16. Half-bridge inverter equivalent test circuit including parasitics.

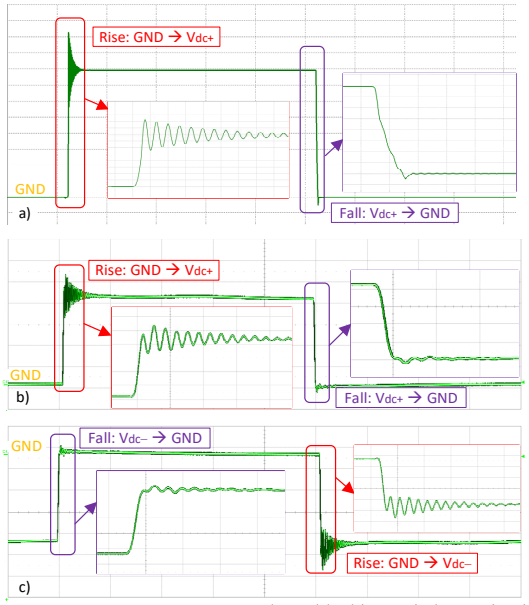

Fig. 17. Common-source reverse-voltage-blocking switch test circuit's waveforms (V_{SW}): a) simulation with V_{dc}=80V; experimental results with: b) V_{dc}=80V and c) V_{dc}= −80V.

conduction losses, it was decided to choose the common-source configuration in Fig. 14c for the initial experimental tests. A printed circuit board (PCB) for the common-source GaN-HEMT RVB switches has been fabricated as shown in Fig. 15. For this PCB, the 650V, 30A GS66508T GaN-HEMT (GaN Systems) was selected due to its double gate drive pad design that can achieve very compact gate drive connections when two devices are connected in series [27].

During the design process, ANSYS Q3D and LTSpice were used for simulation, and the equivalent circuit identifying important parasitic components is shown in Fig. 16. Reverse-voltage-blocking capability has been tested by reversing the dc bus voltage polarity. Figs. 17b and 17c show the experimental results of the voltage across the resistor load (V_{SW}) for both forward- and reverse-voltage-blocking conditions. It can be observed that the switching performances for the two conditions are symmetrical, so that the voltage rise transients from the GND reference to either the positive or negative dc bus rails are almost identical. The same is true for the voltage fall transients from either dc bus rail to GND. Due to the existence of parasitic inductance in the resistive load, during the deadtime when the upper switch S1A/S1B is off, the reactive current in the load needs to have low impedance flowing path to avoid overshoot. Therefore, either S2B or S2A is bypassed for forward- or reverse-voltage-blocking test condition and the reactive current will flow from S2A's source

TABLE II. SUMMARY OF THE DESIGNED REVERSE-VOLTAGE-BLOCKING SWITCH TEST CIRCUIT'S PERFORMANCE

Condition (V_{dc} = 80V, I_{switch} = 4A)	**Rise time, ns**	**Fall time, ns**	**Turn-on overshoot, V**	**Turn-off overshoot, V**
Experiment forward-blocking	10.7	14.9	20.7	7.1
Experiment reverse-blocking	10.8	14.3	23.5	7.5
Simulated forward-blocking	7.2	16.7	22.5	4.7

to drain or S2B's source to drain respectively due to GaN-HEMT's characteristics [24]. The simulation results for the forward-voltage blocking condition is presented in Fig. 17a for comparison. The simulation results match well with the experimental results, which builds confidence in the effectiveness of the simulations for use in future designs. TABLE II summarizes performance metrics of the designed RVB switch test circuit's waveforms shown in Fig. 17.

IV. CONCLUSION

This paper has used simulations to evaluate the impact of WBG power switches on the comparative performance of PWM-CSI and -VSI topologies for machine drive applications with a focus on EMI, efficiency, and over-voltage characteristics. The simulation results demonstrate that the PWM-CSI topology offers valuable performance advantages in each of these categories when the special demands imposed by high-frequency WBG power switches are considered. The combined filtering effect of the CSI's bus inductor and output capacitors on the delivered voltage and current waveforms lies at the heart of these advantages.

In addition, four alternative WBG power switch configurations have been discussed as candidates for providing the reverse-voltage-blocking capability required by CSI switches. The configuration with two series-connected GaN-HEMTs in a common-source configuration has been simulated and experimentally evaluated at 200kHz, with promising results. Work is now under way to apply this switch configuration to build a complete next-generation CSI that will be used to experimentally verify all key simulation results.

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