Comparative Performance Evaluation of Common Mode Voltage Reduction Three-Phase Inverter Topologies

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***Abstract*— Common-mode (CM) voltage related issues such as ground current and EMI are widely known in the three-phase PWM inverter based systems. With the adoption of better semiconductor switching devices, especially silicon carbide and gallium nitride devices, the increased dv/dt and switching frequency further aggravate the situation. As a result, a number of novel inverter topologies have recently been proposed by the researchers to achieve CM voltage reduction or cancellation. In this paper, three CM reduced topologies--floated, balanced, and four-leg inverter topologies have been studied with their performance compared. Based on the analytical, simulation, and experimental results, pros and cons of each topology are summarized and discussed.**

Keywords—common mode (CM), electromagnetic interference (EMI), gallium nitride, inverter topologies.

I. INTRODUCTION

The pulse width modulation (PWM) of three-phase inverters generates continuously varying common mode voltages (CMV) [1]-[2], which result in multiple practical issues, such as ground current, conducted and radiated emissions, and bearing current if used to drive a motor [3]-[5]. When modern power switches, such as silicon carbide (SiC) and gallium nitride (GaN) based devices are used in the inverters, the significantly increased dv/dt and operating frequency of these devices will further aggravate the situation [6]-[8], which has to be taken care of in order to harvest the full benefits of these new devices. Hence, this paper evaluates and compares the performance of novel three-phase inverter topologies that help reduce the CMV generation.

In industry, the CM filters are the widely adopted to cope with the CM related issues, but they can be bulky, expensive, and lossy [13]-[14]. It has also been reported that the size and cost penalties of CM chokes will be further exacerbated as the inverter operating frequency increases [15]. As the alternative solutions, some researchers have also investigated into other creative methods for CMV mitigation, such as active filters [16], new modulation strategies [17], and novel inverter topologies [18]-[23], etc. Active filters typically involve the use of high-performance amplifier or complementary transistors, which are very difficult to be realized in applications rated for more than 100 V. CM reduced PWM techniques also comes with the expense of degradation in DM performance and significant computation overhead. Among all, three inverter topologies, floated, balanced, and four-leg inverter, present themselves as promising solutions, due to their effectiveness in CMV suppression and simplicity in implementation. However, each topology has its own strengths and weaknesses that have not been thoroughly discussed in the literature. As a consequence, the relative advantage of each topology remains unclear to the public and needs to be unveiled.

This paper investigates and compares three CM reduced topologies--floated, balanced, and four-leg inverter as the solutions to the CMV-related issues in three-phase PWM inverter systems. Specifically, the operation principles of three topologies are first explained with key differences highlighted. Several performance metrics, such as efficiency, ground current amplitude, and CM EMI emission, are examined for each topology through simulation and experiments. Based on the data obtained, pros and cons of each topology are thoroughly discussed to provide guidance for topology selection.

II. OPERATING PRINCIPLES OF CMV REDUCED TOPOLOGIES

A. Conventional Three-Phase Inverter and CMV

The circuit schematic of a conventional B6 inverter is shown in Fig. 1a. It consists of three phase-legs, each of which is a series connection of two semiconductor switches. During normal operation, the output potential of each phase leg with respect to ground (i.e. v_{ag}, v_{bg}, and v_{cg}) is continuously switched between the positive and the negative DC bus potential ($+V_{dc}/2$ and $-V_{dc}/2$ if referring to the mid-point of DC bus as ground) due to the PWM of the switches. In consequence, the CMV generated by the inverter,

$$v_{CM0} = (v_{ag} + v_{bg} + v_{cg})/3, \quad (1)$$

also varies with the switching states. The CMV waveform of the B6 inverter in one switching cycle is illustrated in Fig. 2 by blue curve. The varying CMV will induce high amplitude current pulses in the parasitic grounding capacitances in the

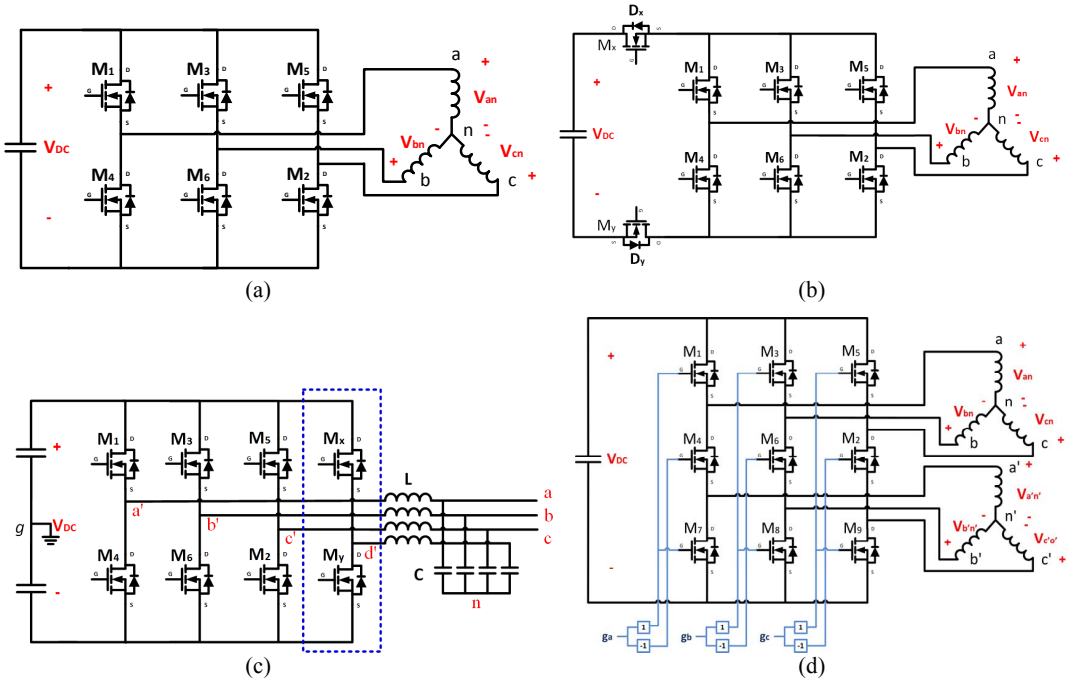

Fig. 1. (a) Conventional B6 inverter; (b) floated inverter; (c) four-leg inverter; (d) balanced inverter.

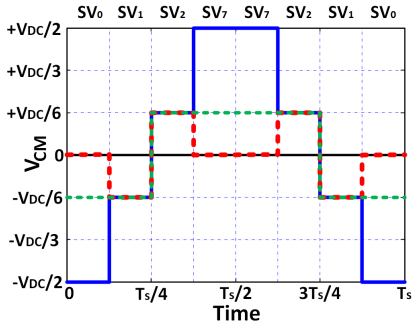

Fig. 2. CMV generated by B6 inverter (blue) and floated inverter (red or green)

CM path, resulting in ground current and CM EMI. CMV also couples to the machine rotor and leads to shaft voltage and bearing current in motor drive applications.

B. *Floated Inverter*

The floated inverter topology is shown in Fig. 1b. It was first introduced by the authors in [19]. It adds two auxiliary switches between the DC bus and three phase-legs. The six main switches operate in the same manner as in a B6 inverter. The two extra switches remain on during active switching states while turn-off during the zero states in order to "float" the load from DC bus. Depending on the gating timing of the two extra switches, the CMV waveforms can be either one of the red or green curves in Fig. 2. It can be seen, the CMV during zero states has been reduced.

C. *Four-Leg Inverter*

The four-leg inverter topology is shown in Fig. 1c, as introduced in [20]. In addition to the conventional six-switch configuration, an auxiliary leg has been added. A four-phase second order filter is also required at the inverter output to interface the auxiliary leg to the three main legs. Note since the two auxiliary switches do not supply load current, they can be derated with respect to the main switches. In order to achieve the CMV reduction, the three main legs and the auxiliary leg have to be operated coordinately so that the following is always maintained,

$$v_{a'g} + v_{b'g} + v_{c'g} + v_{d'g} = 0. \quad (2)$$

The three-phase load and the LC filter can be viewed as an unbalanced four-phase system, whose neutral point voltage at *n* is largely canceled under the constraint of (2). As a result, the corresponding CMV on the three-phase load is also significantly reduced.

D. *Balanced Inverter*

The proposed balanced inverter is shown in Fig. 1d. It was first introduced by the authors in [23]. The balanced inverter has three switches in series for each phase leg. The upper and the lower switches of each phase leg turn on and off simultaneously and are rated at half the DC bus voltage. The middle switch operates complementarily with the other two. Due to the given operation strategy, the two output voltages on each phase-leg always cancel each other, so that the total CMV is almost zero. Two sets of symmetrical loads are also needed to achieve appropriate cancellation.

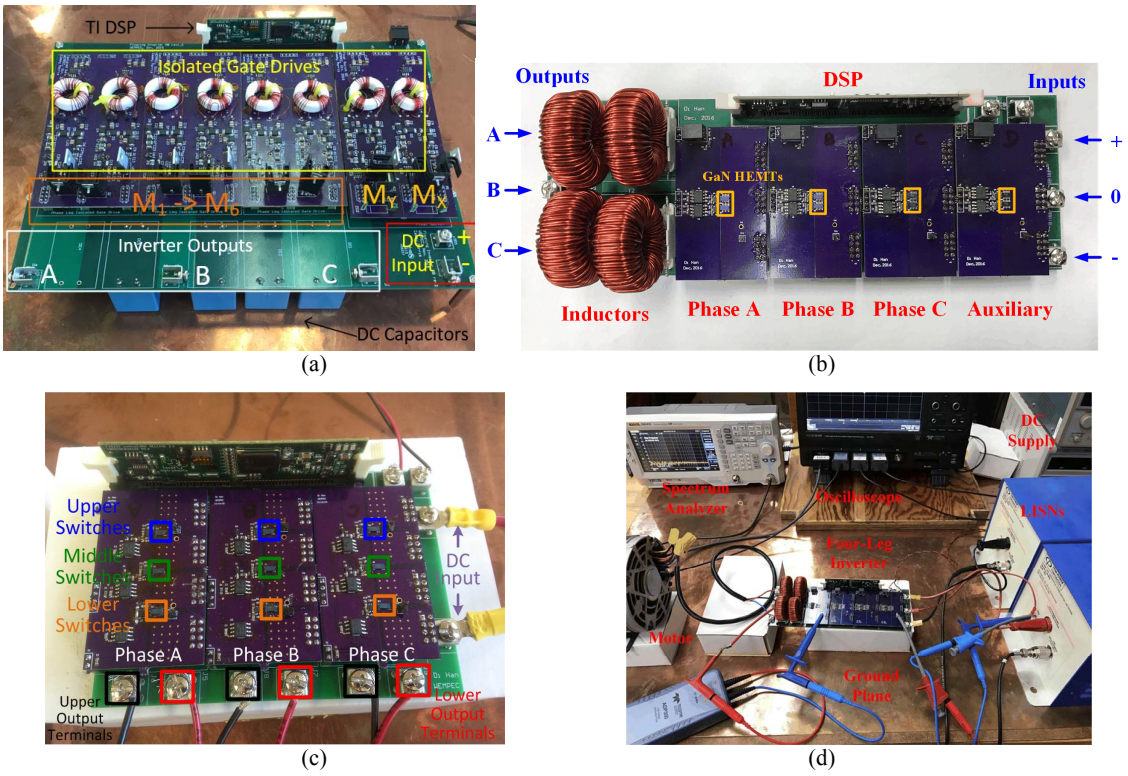

Fig. 3. (a) Floated inverter; (b) four-leg inverter; (c) balanced inverter; (d) test setup.

III. Comparison between Topologies

The three novel inverter topologies have been built in the lab using GaN HEMT EPC2010, as shown in Fig. 3. All of the three inverters can be easily reconfigured to a conventional B6 topology as a comparison baseline. They are used to drive an induction machine, the test conditions are summarized in Table I. The test bench is carefully configured to meet the requirements of typical EMI standards. The whole system is placed on top of a copper ground plane. The inverter prototype is connected to the DC power source through a pair of LISNs at the input. The load motor is also solidly grounded on the frame. The time-domain waveforms are measured with an oscilloscope while CM EMI spectrum is measured with a noise separator and a spectrum analyzer.

In this section, all four topologies studied will be compared regarding ground current, EMI spectra, and efficiency. The corresponding figures are plotted in Fig. 4a through Fig. 4c.

It can be seen from Fig. 4a that the balanced inverter achieves almost zero CM current, thus having the smallest CM current amplitude among all due to its perfect cancellation effect. The four-leg topology has the second smallest CM current. The floated inverter does not decrease the ground current amplitude compared to the conventional topology because the switching transitions still exist despite the reduced CMV amplitude.

From the noise spectra shown in Fig 4b, the floated inverter only achieves a few dB reduction with respect to the conventional topology. This is because the floated topology does not achieve CMV cancellation, but only manipulate the CMV during the zero states. On the other hand, the balanced and four-leg topologies have a very low emission level in the low-frequency range, achieving 40 dB reduction with respect to the conventional B6, due to the cancellation effect. Their EMI emissions gradually increase above 1 MHz and the balanced topology performs a little better than the four-leg topology at high-frequency range. The un-cancelled portion is due to the misalignment of the transition edges and the resonant points in the CM circuit path.

From the efficiency plot in Fig. 4c, it is clear that the balanced inverter has the best efficiency which has even lower loss than the conventional topology. This is due to the fact that replacing one full-voltage-rated device by two half-voltage-rated devices tends to reduce both the conduction and switching loss, as has been observed in multi-level topologies. On the other hand, both floated and four-leg inverter has lower efficiency than the B6 topology in most of the load range, mainly due to the extra losses generated on the additional two switches. Also note that the filter loss of the four-leg inverter is not accounted for in this figure, which otherwise renders the four-leg significantly worse than the others in terms of efficiency.

IV. Conclusion

This paper investigates and compares three CM reduced topologies--floated, balanced, and four-leg inverter as the solutions to the CMV-related issues in three-phase PWM

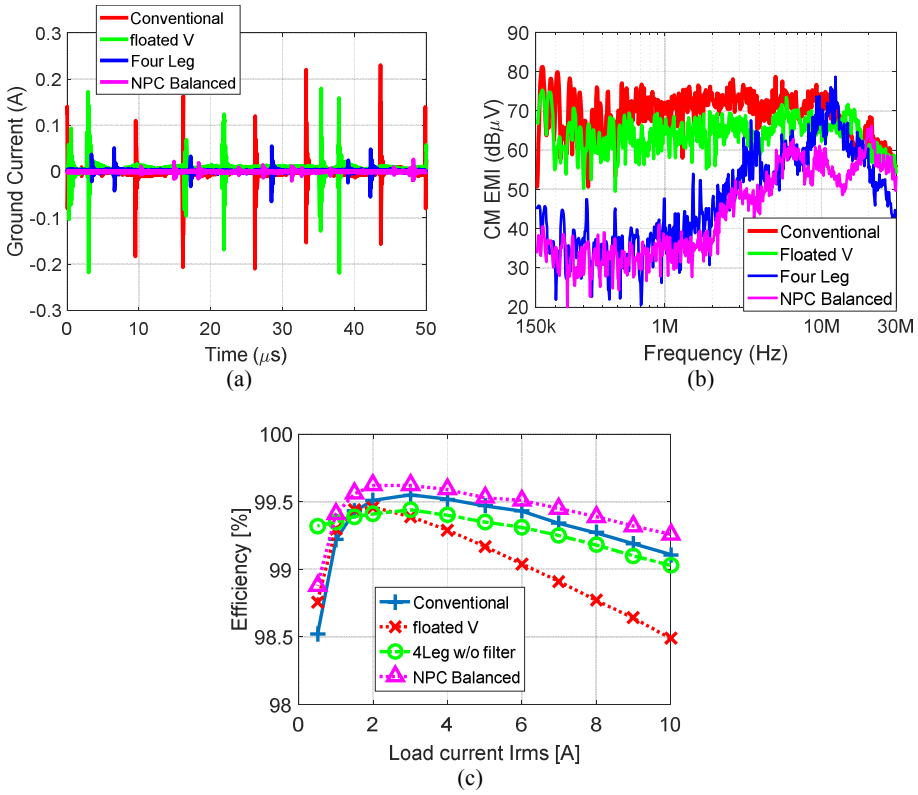

Fig. 4. Comparison of different topologies in terms of (a) CM current; (b) conducted CM EMI emission; (c) efficiency.

inverter systems. It is shown that all three topologies help reduce the CM voltage and CM EMI emission compared to the B6 inverter, but their principles are quite different. The floated inverter disconnects the inverter from DC bus during zero states, so that it only reduces the CMV during zero states. As a result, a few dB reduction in CM EMI is achievable through floated topology while limited influence on CM current is observed. The four-leg inverter adds a fourth leg and a second order filter to the system, and it utilizes a special PWM method to maintain total zero CMV. It significantly reduces the CM current and achieves 40 dB reduction in low-frequency emission. However, it does need DM filter which puts penalty on the size and loss. The balanced inverter generates two sets of output than cancel each other in terms of CMV. It has the minimum CM current and least EMI emission among all. However, it does need to drive two symmetrical loads, such as two sets of windings of a motor.

From the above discussion, the balanced inverter has the best performance among all and is most suitable for motor drive applications, especially when two sets of stator windings are readily available. The four-leg inverter is very attractive for grid connected applications when output DM filters are already in place. The floated inverter may be used in rest of the applications that does not fit the two above.

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