# Duo-Active-Neutral-Point-Clamped Multilevel Converter: An Exploration of the Fundamental Topology and Experimental Verification

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***Abstract*— For medium-voltage (MV) industrial applications such as the HVDC and adjustable-speed ac-motor drives, the multilevel voltage-source converters are deemed the predominant topologies. One of the promising derived-topologies from the neutral-point-clamped (NPC) configuration is the active NPC (ANPC) structure with an improved balanced loss-distribution performance. This paper introduces duo-ANPC (D-ANPC) converter topology, which is controlled with a new modulation technique. The suggested control method regulates the flying capacitor (FC) voltages naturally at their reference values and preserves the indispensable attribute of the natural balance in the FC-based ANPC inverters. The D-ANPC converter's phase leg is formed by equipping the classic ANPC converter with additional two low-frequency (LF) MV power switches, adding up to six in contrast to four LF power switches in the ANPC. The proposed D-ANPC converter has considerable advantages over the classic multilevel inverters that makes it a competitive topology for MV applications. The substantial reduction in the number of the high-frequency (HF) MV insulated-gate bipolar transistors (IGBTs) by 50% in comparison with the classic ANPC converter as well as a drastic abatement in the total voltage rating and the stored energy of the FCs are the main significant advantages offered by the D-ANPC multilevel converter over the flying-capacitor-based inverters. This study explores the fundamental circuitry of the proposed D-ANPC multilevel topology and provides an exhaustive comparison with classic FC-based inverters. The experimental results are presented to validate the proposed D-ANPC topology and its modulation.**

***Index Terms*- ANPC inverter, flying-capacitor voltage decrement, Duo-ANPC converter, IGBT abatement, natural balance, PSCPWM, stored energy reduction.**

## I. Introduction

The invention of the three-level neutral-point-clamped (NPC) converter marked the dawning of a new era in the topological field of the power electronic inverters recognized as "multilevel converters" [1], [2]. A decade later, the flying-capacitor multicell (FCM) was introduced by Meynard and Foch as a new multilevel converter topology [3], [4]. The sharp distinction between the FCM and NPC topology lies in the use of the flying-capacitors (FCs) as the voltage-clamping devices across the semiconductor power switches within the imbricated cells of the FCM converter, in contrast to the clamping diodes in the NPC topology. The three-level configuration of both converters reduced the blocking voltage of the semiconductor power switches by 50%. In other words, the employed insulated-gate bipolar transistors (IGBTs) are required to sustain and block half of the DC-link voltage, in contrast to the IGBT's full DC-link blocking-voltage rating in the traditional two-level converters [5], [6]. The cascaded multicell (CM) topology is considered as another multilevel breed that overcomes the voltage limitation complication concerning semiconductors employed in the two-level power converters which are incapable of sustaining the desired MV or higher DC-voltages. The solution lies in the cascaded connection of the several low-voltage H-bridge cells in which only a fraction of the main DC voltage is applied to each cell through isolating devices such as the multipulse transformers equipped with passive/active rectifiers or multiple isolated low-voltage DC inputs [7], [8]. Today, standard commercialized topologies of the multilevel converters include NPC, FCM, CM, and modular multilevel converters (MMCs) [9]. The innovative use of active power switches instead of

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passive clamping diodes in three-level NPC converters to balance the loss among the semiconductors is reported in [10]–[12]. Later, ABB introduced a new power conversion approach on the basis of the combining a single three-level NPC converter equipped with active switches and a single FCM multilevel converter together [13], [14]. The new hybrid power converter topology is referred to as active NPC (ANPC) multilevel converter which benefits of the robustness of the NPC along with the flexibility of the FCM converters [15]. The ANPC technology has now been matured into the ABB's ACS2000 MV motor drive series. Discerning the advantages of the ANPC topology and considering the escalating penetration of the multilevel inverters in the MV energy management market, this paper proposes a duo-ANPC (D-ANPC) topology which is controlled with a new modulation technique. The suggested control method regulates the flying capacitor (FC) voltages naturally at the reference values and preserves the indispensable attribute of the natural balance in the FC-based ANPC inverters. The experimental results are presented to validate the proposed D-ANPC topology and its suggested modulation method.

## II. Proposed Topology

The classic FC-based inverters including the FCM, the stacked multicell (SM), and the ANPC converters along with proposed D-ANPC converter are depicted in Figs. 1-2. The D-ANPC converter phase leg is formed by equipping the traditional ANPC with additional 2 low-frequency (LF) switches[1]. A fair comparison among the conventional FC-based multilevel converters and proposed D-ANPC converter for generating an identical output voltage (i.e., $4n+1$-level, $2E$ peak-to-peak, $4n$-p.u) is presented in Table I. This demonstrates that the proposed D-ANPC converter takes considerable advantages over the aforementioned inverters by reducing the number and voltage rating of the HF IGBTs as well as the capacitors, along with a drastic reduction in capacitor's stored energy. The total voltage ratings $\big(\mathcal{V}(n)\big)$ and stored energy $\big(\mathcal{E}(n)\big)$ of the DC-link capacitors and FCs in FCM, SM, ANPC, and D-ANPC converters are calculated in Eqs. 1-8 while their ratios are expressed in Eqs. 9-14.

$$\mathcal{E}(n)_{FCM} = \sum_{i=1}^{4n-1} \frac{C}{2}\left(i \times \frac{2E}{4n}\right)^2 + 2 \times \frac{C}{2}\big(E\big)^2 = \big(\frac{32n^2+1}{12n}\big)CE^2 \tag{1}$$

$$\mathcal{V}(n)_{FCM} = \sum_{i=1}^{4n-1}\left(i \times \frac{2E}{4n}\right) + 2 \times \big(E\big) = \big(4n+1\big)E \tag{2}$$

[1]Throughout this paper LF switches are deemed to be switching at line-frequency.

$$\mathcal{E}(n)_{SM} = 2 \times \sum_{i=1}^{2n} \frac{C}{2}\left(i \times \frac{E}{2n}\right)^2 = \big(\frac{8n^2+6n+1}{12n}\big)CE^2 \tag{3}$$

$$\mathcal{V}(n)_{SM} = 2 \times \sum_{i=1}^{2n}\left(i \times \frac{E}{2n}\right) = \big(2n+1\big)E \tag{4}$$

$$\mathcal{E}(n)_{ANPC} = \sum_{i=1}^{2n-1} \frac{C}{2}\left(i \times \frac{E}{2n}\right)^2 + 2 \times \frac{C}{2}\big(E\big)^2 = \big(\frac{8n^2+18n+1}{24n}\big)CE^2 \tag{5}$$

$$\mathcal{V}(n)_{ANPC} = \sum_{i=1}^{2n-1}\left(i \times \frac{E}{2n}\right) + 2 \times \big(E\big) = \big(n+1.5\big)E \tag{6}$$

$$\mathcal{E}(n)_{D-ANPC} = \sum_{i=1}^{n-1} \frac{C}{2}\left(i \times \frac{E}{2n}\right)^2 + 2 \times \frac{C}{2}\big(E/2\big)^2 = \big(\frac{2n^2+9n+1}{48n}\big)CE^2 \tag{7}$$

$$\mathcal{V}(n)_{D-ANPC} = \sum_{i=1}^{n-1}\left(i \times \frac{E}{2n}\right) + 2 \times \big(E/2\big) = \big(0.25n+0.75\big)E \tag{8}$$

$$\frac{\mathcal{E}(n)_{D-ANPC}}{\mathcal{E}(n)_{ANPC}} = \frac{1}{2} \times \frac{2n^2+9n+1}{8n^2+18n+1} \tag{9}$$

$$\frac{\mathcal{E}(n)_{D-ANPC}}{\mathcal{E}(n)_{SM}} = \frac{1}{4} \times \frac{2n^2+9n+1}{8n^2+6n+1} \tag{10}$$

$$\frac{\mathcal{E}(n)_{D-ANPC}}{\mathcal{E}(n)_{FCM}} = \frac{1}{4} \times \frac{2n^2+9n+1}{32n^2+1} \tag{11}$$

$$\frac{\mathcal{V}(n)_{D-ANPC}}{\mathcal{V}(n)_{ANPC}} = \frac{0.25n+0.75}{n+1.5} \tag{12}$$

$$\frac{\mathcal{V}(n)_{D-ANPC}}{\mathcal{V}(n)_{SM}} = \frac{0.25n+0.75}{2n+1} \tag{13}$$

$$\frac{\mathcal{V}(n)_{D-ANPC}}{\mathcal{V}(n)_{FCM}} = \frac{0.25n+0.75}{4n+1} \tag{14}$$

As an example, in order to generate a 17-level single-phase voltage with a peak-to-peak value of 16 p.u. the FCM converter would require a 16 p.u. DC-bus voltage, 16 HF-switching-cells, 32 HF-IGBTs with 1 p.u. voltage rating, 15 FCs with voltage ratings ranging from 1 p.u. to 15 p.u., and two DC-bus capacitors with voltage ratings of 8 p.u.. According to Eqs. 1-2 and Table I, the total voltage rating and stored energy of all the DC-capacitors would be $17E$ p.u. and $10.6875CE^2$ J, respectively. The SM converter would require a 16 p.u. DC-bus voltage, 16 HF-switching-cells, 16 HF-IGBTs with 1 p.u. voltage rating, 16 HF-IGBTs with 2 p.u. voltage rating, two sets of FCs wherein each set comprises 7 FCs with voltage ratings ranging from 1 p.u. to 7 p.u., and two DC-bus

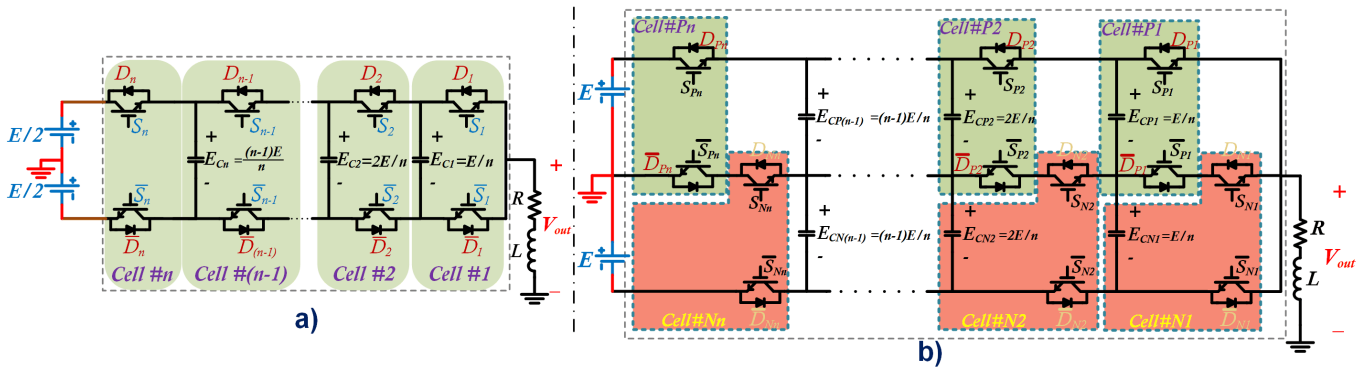


Fig. 1. Generalized topology of: (a) $n$-cell $n+1$-level $E$-peak-to-peak FCM; (b) $n$-cell $2n+1$-level $2E$-peak-to-peak SM converters.

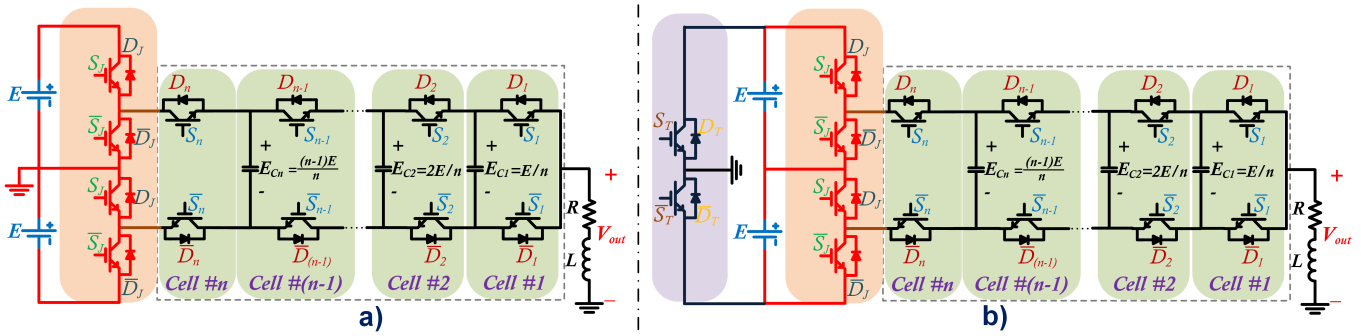


Fig. 2. Generalized topology of: (a) $n$-cell $2n+1$-level $2E$-peak-to-peak ANPC; (b) proposed $n$-cell $4n+1$-level $4E$-peak-to-peak D-ANPC converters.

capacitors with voltage ratings of 8 p.u.. According to Eqs. 3-4 and Table I, the total voltage rating and stored energy of all the DC-capacitors would be $9E$ p.u. and $3.1875CE^2$ J, respectively. The ANPC converter would require a 16 p.u. DC-bus voltage, 8 HF-switching-cells, 16 HF-IGBTs with 1 p.u. voltage rating, 4 LF-IGBTs with 8 p.u. voltage rating, 7 FCs with voltage ratings ranging from 1 p.u. to 7 p.u., and two DC-bus capacitors with voltage ratings of 8 p.u.. According to Eqs. 5-6 and Table I, the total voltage rating and stored energy of all the DC-capacitors would be $5.5E$ p.u. and $2.0938CE^2$ J, respectively. The D-ANPC converter would require a 8 p.u. DC-bus voltage, 4 HF-switching-cells, 8 HF-IGBTs with 1 p.u. voltage rating, 4 LF-IGBTs with 4 p.u. voltage rating, 2 LF-IGBTs with 8 p.u. voltage rating, 3 FCs with voltage ratings ranging from 1 p.u. to 3 p.u., and two DC-bus capacitors with voltage ratings of 4 p.u.. According to Eqs. 7-8 and Table I, the total voltage rating and stored energy of all the DC-capacitors would be $1.75E$ p.u. and $0.3594CE^2$ J, respectively. Therefore, the DC-capacitors total voltage rating and stored energy in D-ANPC converter are 10.29% and 3.36% of the values in FCM converter, respectively. Accordingly, the DC-capacitors total voltage rating and stored energy in D-ANPC converter are 19.44% and 11.27% of the values in SM converter, respectively. Ultimately, the DC-capacitors total voltage rating and stored energy in D-ANPC converter are 31.82% and 17.16% of the values in ANPC converter, respectively. As elaborated in Eqs. 15-20, it is worth pointing out that for a sufficiently large number of voltage levels, these ratios tend to converge to 6.25% and 1.56%, when compared to an FCM, 12.5% and 6.25%, when compared to an SM, 25% and 12.5%, when compared to an ANPC converter. This comparison is depicted in Figs. 3-4. Therefore, the substantial reduction in number of HF IGBTs by 50% in comparison with traditional ANPC converter along with a drastic decrease in the total voltage rating and stored energy of the capacitors are the major advantages offered by D-ANPC multilevel converter over the FC-based inverters.

$$\lim_{n\to+\infty} \frac{\mathcal{E}(n)_{D-ANPC}}{\mathcal{E}(n)_{ANPC}} \approx \left(\frac{1}{2}\right)^3 = 0.125 = 12.5\% \quad (15)$$

$$\lim_{n\to+\infty} \frac{\mathcal{E}(n)_{D-ANPC}}{\mathcal{E}(n)_{SM}} \approx \left(\frac{1}{2}\right)^4 = 0.0625 = 6.25\% \quad (16)$$

$$\lim_{n\to+\infty} \frac{\mathcal{E}(n)_{D-ANPC}}{\mathcal{E}(n)_{FCM}} \approx \left(\frac{1}{2}\right)^6 = 0.015625 = 1.5625\% \quad (17)$$

$$\lim_{n\to+\infty} \frac{\mathcal{V}(n)_{D-ANPC}}{\mathcal{V}(n)_{ANPC}} \approx \left(\frac{1}{2}\right)^2 = 0.25 = 25\% \quad (18)$$

$$\lim_{n\to+\infty}\frac{\mathcal{V}(n)_{D-ANPC}}{\mathcal{V}(n)_{SM}}\approx\left(\frac{1}{2}\right)^3=0.125=12.5\% \tag{19}$$

$$\lim_{n\to+\infty}\frac{\mathcal{V}(n)_{D-ANPC}}{\mathcal{V}(n)_{FCM}}\approx\left(\frac{1}{2}\right)^4=0.0625=6.25\% \tag{20}$$

## III. Proposed Modulation Technique

The proposed control technique for D-ANPC employs the phase-shifted carrier (PSC) pulse width modulation (PSC-PWM) strategy wherein the triangular carriers are interleaved and phase shifted by $\frac{2\pi}{n}$ to achieve a superior harmonic characteristic. The sinusoidal reference waveform, the triangular carriers, and the corresponding switching pulses are defined in Eqs. 21-30, respectively.

$$\Psi(t)=\begin{cases}M\sin\left(\omega_r t+\varphi\right) & -\varphi\le\omega_r t<\pi-\varphi\\ 1+M\sin(\omega_r t+\varphi) & \pi-\varphi\le\omega_r t<2\pi-\varphi\end{cases} \tag{21}$$

$$\Omega(t)=\begin{cases}(2E_c-1)\left(\frac{t}{T_c}-q\right)+0.5 & qT_c\le t\le qT_c+\frac{T_c}{2}\\ (1-2E_c)\left(\frac{t}{T_c}-q-1\right)+0.5 & qT_c+\frac{T_c}{2}\le t\le(q+1)T_c\end{cases} \tag{22}$$

$$\kappa_i(t)=\Omega\Big(t+\frac{\big(i-1\big)T_c}{n}\Big) \tag{23}$$

$$S_T(t)=\begin{cases}0 & -\varphi\le\omega_r t<\pi-\varphi\\ 1 & \pi-\varphi\le\omega_r t<2\pi-\varphi\end{cases} \tag{24}$$

$$S_J(t)=\begin{cases}1 & 0.5\le\Psi(t)\\ 0 & 0.5>\Psi(t)\end{cases} \tag{25}$$

$$\vartheta=\sin^{-1}\left(\frac{1}{2M}\right) \tag{26}$$

$$\Upsilon_1(t)=\begin{cases}0.5 & -\varphi\le\omega_r t<\vartheta-\varphi\\ 0 & \vartheta-\varphi\le\omega_r t<2\pi-\varphi\end{cases} \tag{27}$$

$$\Upsilon_2(t)=\begin{cases}0 & -\varphi\le\omega_r t<\pi-\vartheta-\varphi\\ 0.5 & \pi-\vartheta-\varphi\le\omega_r t<\pi-\varphi\\ 0 & \pi-\varphi\le\omega_r t<2\pi-\varphi\end{cases} \tag{28}$$

$$\Upsilon_3(t)=\begin{cases}0 & -\varphi\le\omega_r t<\pi+\vartheta-\varphi\\ 0.5 & \pi+\vartheta-\varphi\le\omega_r t<2\pi-\vartheta-\varphi\\ 0 & 2\pi-\vartheta-\varphi\le\omega_r t<2\pi-\varphi\end{cases} \tag{29}$$

$$\alpha_i(t)=\begin{cases}1 & \kappa_i(t)\le\Big(\Psi(t)+\Upsilon_1(t)+\Upsilon_2(t)+\Upsilon_3(t)\Big)\\ 0 & \kappa_i(t)>\Big(\Psi(t)+\Upsilon_1(t)+\Upsilon_2(t)+\Upsilon_3(t)\Big)\end{cases} \tag{30}$$

where $M$ is modulation index, $f_r$ is reference frequency, $f_c$ and $T_c$ are the triangular carrier waveform frequency ($f_{sw}$) and period, and $E_c$ is the carrier amplitude. Moreover, the carrier signals amplitude is considered $0.5\ \big(0.5\le\Omega(t)\le1\big)$ along with $\omega_r=2\pi f_r$, $\omega_c=2\pi f_c$, $f_c=1/T_c$, $i=1,2,3,...,n$, $q\in\mathbb{Z}^+$. It is worth noting that $\alpha_i(t)$ are the control pulses for $S_{(n-i+1)}$ within $\big(n-i+1\big)^{th}$-HF cells of the D-ANPC converter. The switching states of a 2-cell-9-level D-ANPC are presented in Table II. Fig. 5 illustrates the switching states and the ON/OFF IGBTs in the 2-cell 9-level D-ANPC with conducting semiconductors being emphasized in red color.

## IV. Experimental Results

To validate the proposed converter topology, a 2-cell-9-level prototype was built using IXYS IXGH48N60B3D1 IGBTs. TMS320F28335 DSP has been utilized to implement the proposed modulation technique. The switching frequency ($f_{sw}$) was 2.5 kHz, the DC-link voltage was 310 V, and the $RL$ load had a resistance of 24 Ω and an inductance of 15 mH. The experimental measurements of two and one cycles of the load voltage and current, dynamics of the FC voltage, and the harmonic content of the D-ANPC converter's generated voltage are depicted in Fig. 6. As demonstrated, the FC voltage is regulated and balanced naturally at 77.5 V exploiting the proposed modulation method. The proposed $n-$cell$-4n+1$-level D-ANPC converter has a harmonic cluster around $\psi\times2\times n\times f_{sw}$ where $\psi$ is an integer. This shows that the generated multilevel voltage of proposed D-ANPC converter has a significantly improved harmonic content as compared to other converters. As presented, harmonics are placed at $\psi\times2\times2\times2500$ including 10 kHz, 20 kHz, etc.

## V. Conclusion

This paper has introduced a new topology for ANPC multilevel family with an innovative control technique and modulation method. The proposed D-ANPC converter reduces the number of HF switching-power-cells in an ANPC converter by 50%. The substantial reduction in the number of HF MV IGBTs by 50% in comparison with traditional ANPC converter along with a drastic decrease in the total voltage rating and stored energy of the FCs are the paramount advantages of the proposed D-ANPC converter. The innovative modulation technique regulates the FC voltages at reference values naturally and retains the indispensable natural balance property within the proposed converter. The fundamental circuitry of the proposed topology is explored along with an exhaustive comparison with classic FC-based converters. The experimental results validates the proposed concept and its modulation method.

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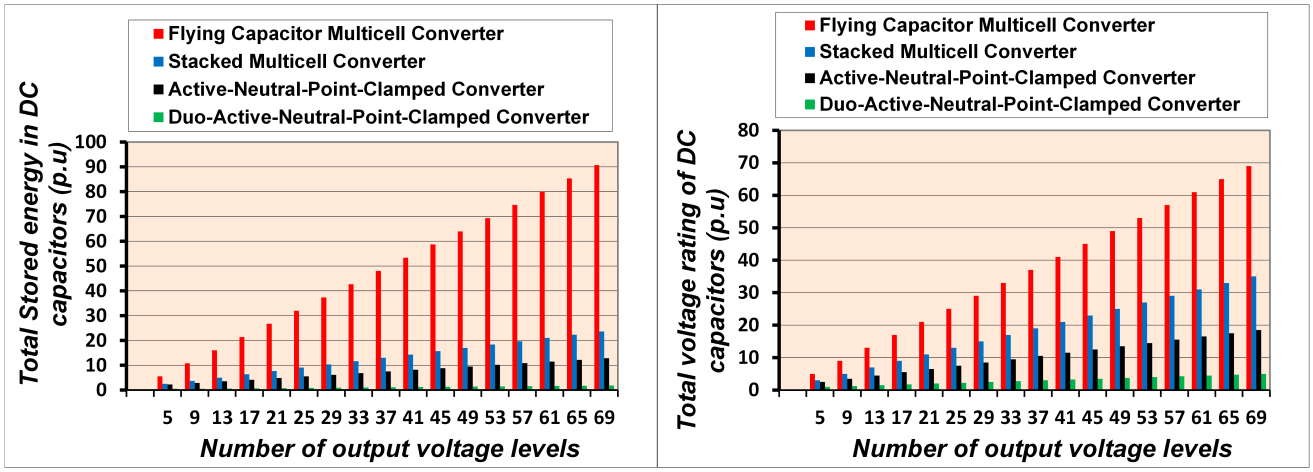


Fig. 3. Capacitors total stored energy and voltage rating comparison in FCM, SM, ANPC, and D-ANPC converters.

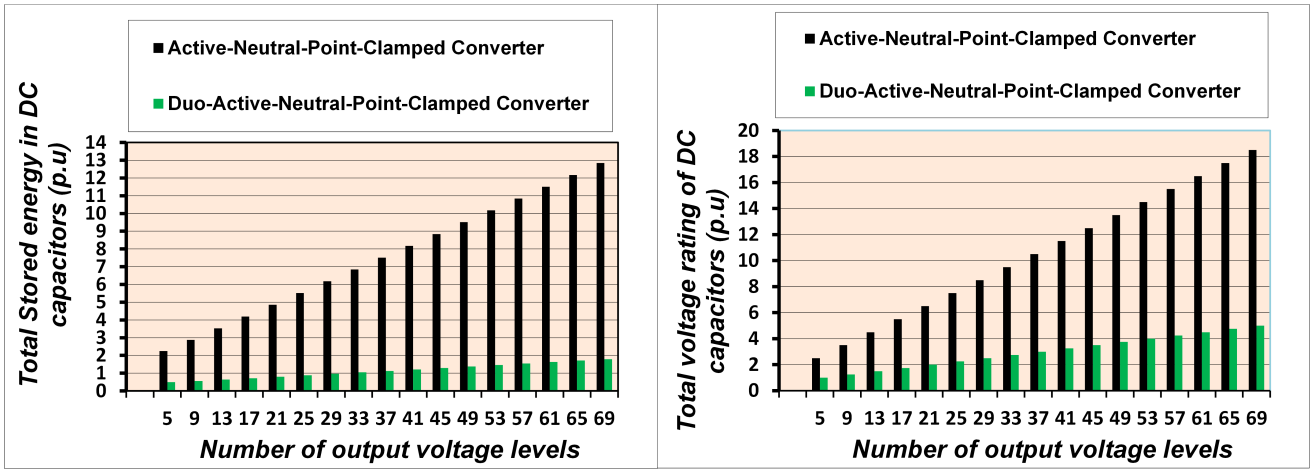


Fig. 4. Capacitors total stored energy and voltage rating comparison in ANPC and D-ANPC converters.

TABLE I

COMPARISON AMONG THE CONVENTIONAL MULTILEVEL CONVERTERS AND PROPOSED D-ANPC CONVERTER FOR GENERATING AN IDENTICAL OUTPUT VOLTAGE (I.E., $4n+1$-LEVEL, $2E$ PEAK-TO-PEAK, $4n$-P.U.)

| Type of multilevel converter | No. of cells | No. of HF switches ($\alpha$) | No. of LF switches ($\beta$) | No. of DC capacitors (DC link and FCs) | Voltage rating of HF switches (p.u)($\gamma$) | Voltage rating of LF switches (p.u)($\lambda$) | Voltage rating of DC sources (p.u) | Voltage rating of capacitors (DC link and FCs) (p.u) | No. of HF modular switches ($\alpha\times\gamma$) | No. of LF modular switches ($\beta\times\lambda$) |
|---|---|---|---|---|---|---|---|---|---|---|
| FCM | $4n$ | $8n$ | 0 | $4n+1$ | 1 | 0 | $4n$ | first type: 1 to $4n-1$ second type: $2\times$ $2n$ p.u. | $8n$ | 0 |
| SM | $2\times2n$ | $8n$ | 0 | $4n$ | $4n$ are 1 $4n$ are 2 | 0 | $4n$ | 2 series: 1 to $2n$ | $12n$ | 0 |
| ANPC | $2n$ | $4n$ | 4 | $2n+1$ | 1 | $2n$ | $4n$ | first type: 1 to $2n-1$ second type: $2\times$ $2n$ p.u. | $4n$ | $8n$ |
| D-ANPC | $n$ | $2n$ | 6 | $n+1$ | 1 | 4 are $n$ 2 are $2n$ | $2n$ | first type: 1 to $n-1$ second type: $2\times$ $n$ p.u. | $2n$ | $8n$ |

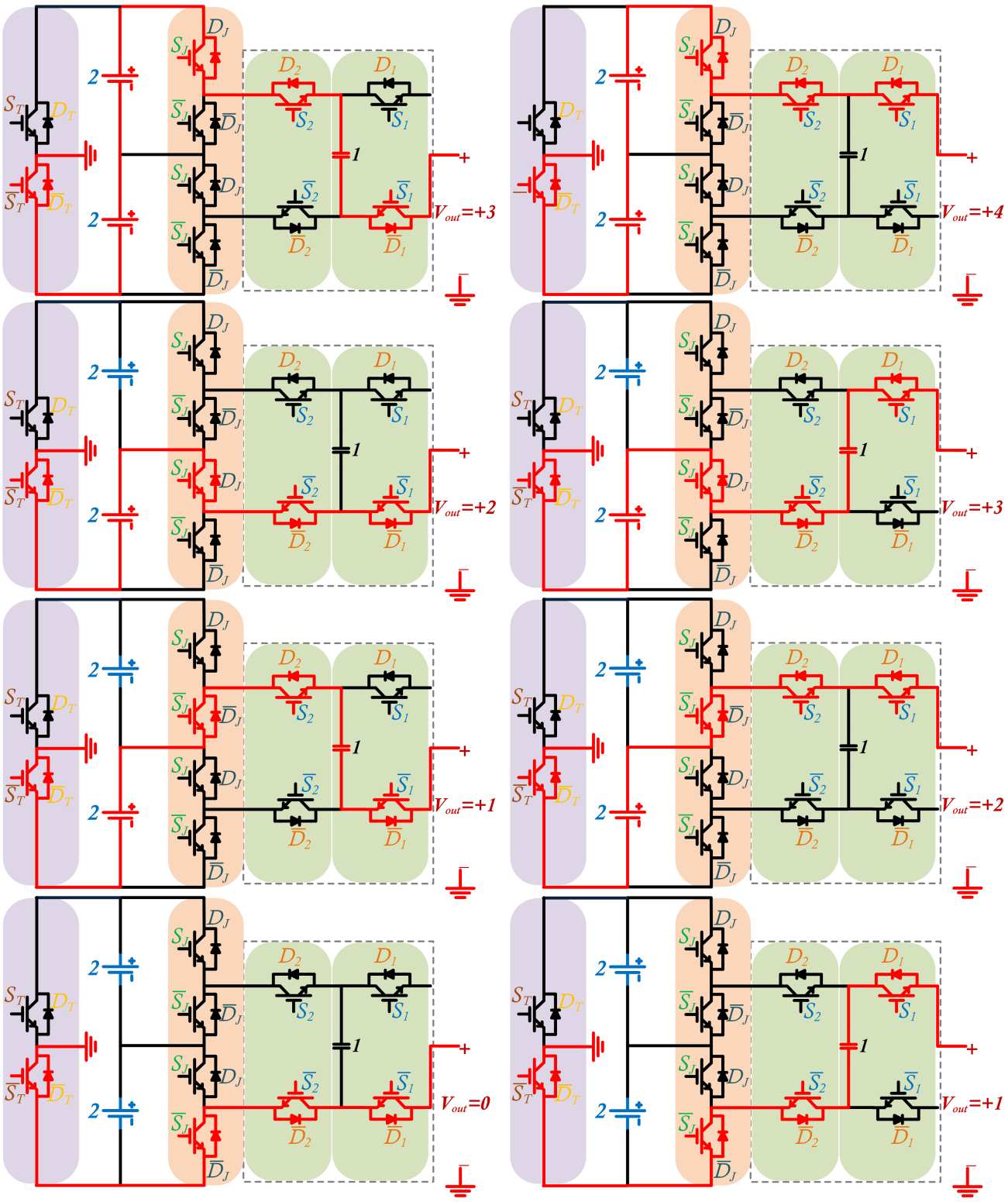


Fig. 5. Illustration of the redundant switching states and ON/OFF IGBTs in a 2-cell 9-level D-ANPC converter.

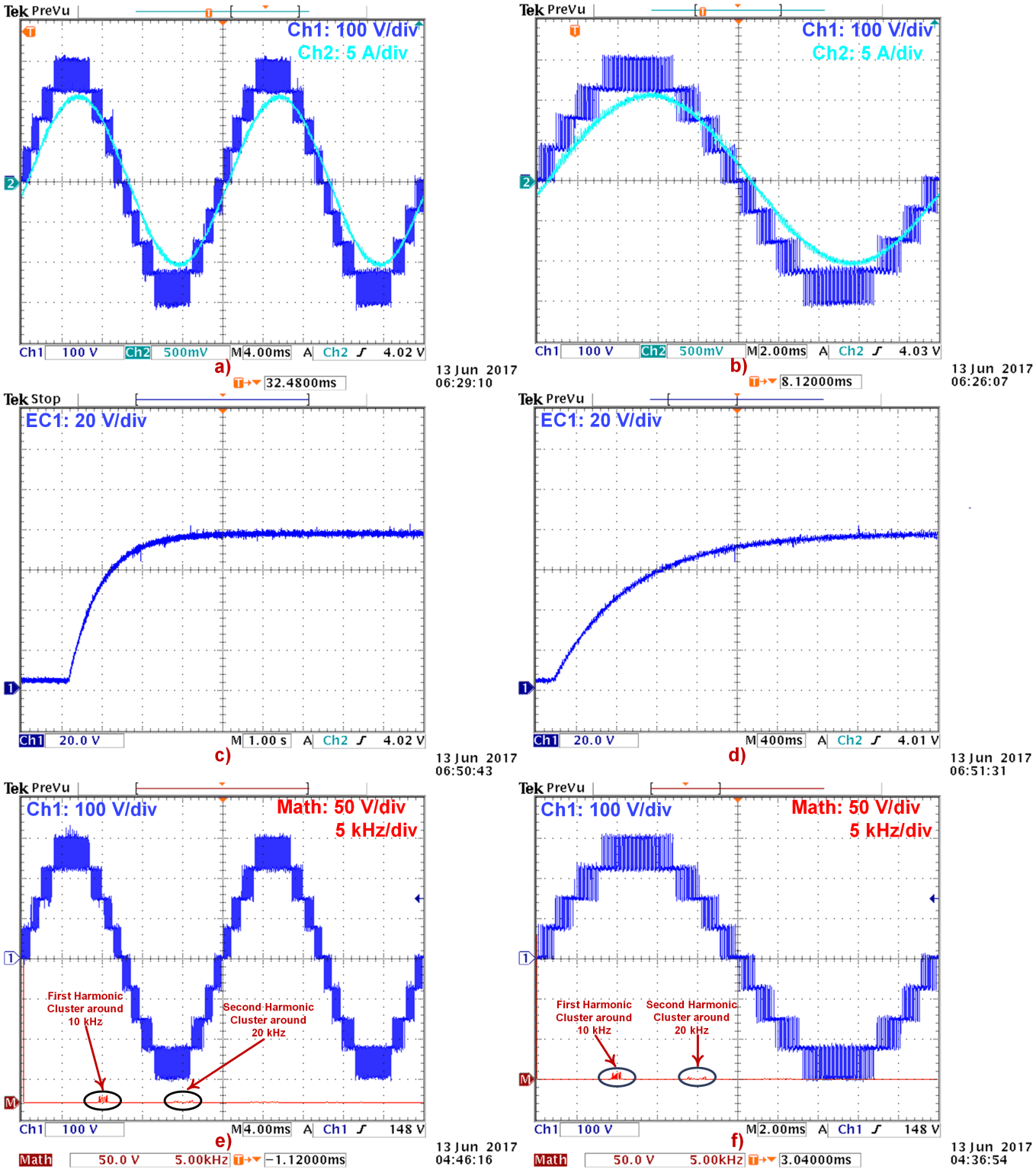


Fig. 6. Experimental results of a 2-cell-9-level proposed D-ANPC converter: Two and one cycles of load voltage and current, dynamics of FC voltage, and harmonic clusters of D-ANPC converter's generated multilevel voltage.

TABLE II
SWITCHING STATES OF THE PROPOSED 2-CELL 9-LEVEL D-ANPC CONVERTER.

| Voltage-Level | State of Switching Devices | | | $\Delta E_{C1}$ | FC Voltage | $i_{Load}$ | Redundant States |
|---|---|---|---|---|---|---|---|
| | $S_T$ | $(S_J, \overline{S}_J)$ | $(S_2, S_1)$ | | | | |
| +4 | 0 | (1,0) | (1,1) | 0 | not impacted | $\lvert i_{Load}\rvert \geq 0$ | 1 |
| +3 | 0 | (1,0) | (1,0) | + | charging(↗) | $i_{Load} > 0$ | 2 |
| | | | | - | discharging(↘) | $i_{Load} < 0$ | |
| | | (1,0) | (0,1) | - | discharging(↘) | $i_{Load} > 0$ | |
| | | | | + | charging(↗) | $i_{Load} < 0$ | |
| +2 | 0 | (1,0) | (0,0) | 0 | not impacted | $i_{Load} > 0$ | 2 |
| | | | | 0 | not impacted | $i_{Load} < 0$ | |
| | | (0,1) | (1,1) | 0 | not impacted | $i_{Load} > 0$ | |
| | | | | 0 | not impacted | $i_{Load} < 0$ | |
| +1 | 0 | (0,1) | (1,0) | + | charging(↗) | $i_{Load} > 0$ | 2 |
| | | | | - | discharging(↘) | $i_{Load} < 0$ | |
| | | (0,1) | (0,1) | - | discharging(↘) | $i_{Load} > 0$ | |
| | | | | + | charging(↗) | $i_{Load} < 0$ | |
| 0 | 0 | (0,1) | (0,0) | 0 | not impacted | $\lvert i_{Load}\rvert \geq 0$ | 2 |
| | 1 | (1,0) | (1,1) | 0 | not impacted | $\lvert i_{Load}\rvert \geq 0$ | |
| −1 | 1 | (1,0) | (1,0) | + | charging(↗) | $i_{Load} > 0$ | 2 |
| | | | | - | discharging(↘) | $i_{Load} < 0$ | |
| | | (1,0) | (0,1) | - | discharging(↘) | $i_{Load} > 0$ | |
| | | | | + | charging(↗) | $i_{Load} < 0$ | |
| −2 | 1 | (1,0) | (0,0) | 0 | not impacted | $i_{Load} > 0$ | 2 |
| | | | | 0 | not impacted | $i_{Load} < 0$ | |
| | | (0,1) | (1,1) | 0 | not impacted | $i_{Load} > 0$ | |
| | | | | 0 | not impacted | $i_{Load} < 0$ | |
| −3 | 1 | (0,1) | (1,0) | + | charging(↗) | $i_{Load} > 0$ | 2 |
| | | | | - | discharging(↘) | $i_{Load} < 0$ | |
| | | (0,1) | (0,1) | - | discharging(↘) | $i_{Load} > 0$ | |
| | | | | + | charging(↗) | $i_{Load} < 0$ | |
| −4 | 1 | (0,1) | (0,0) | 0 | not impacted | $\lvert i_{Load}\rvert \geq 0$ | 1 |


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