Integrated Inductors, Capacitors, and Damping in Bus Bars for *dv/dt* Filter Applications

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***Abstract*—A *dv/dt* filter is useful to mitigate the deleterious effects of voltage pulses with high edge rates, such as voltage overshoot in motor drive systems, which can cause premature motor failure. With the introduction of wide–bandgap semiconductor drives, these issues will become more pronounced. This paper introduces a new type of *dv/dt* filter where the inductor, capacitor, and damping resistor are integrated into the output bus bar or cable of the inverter. This integrated filter may be smaller, lighter, and cheaper to construct than filters built from discrete components. An analytical model of the integrated *dv/dt* filter is developed, and this model is used to design output filters for a 460 V AC, 3–phase silicon carbide motor drive that meet the NEMA MG 1 Part 31 requirements for inverter–rated motors. Prototype filters are constructed and tested with a silicon carbide inverter connected to a 460 Vrms induction motor, and experimental results demonstrate output waveforms that match the analytical model and meet the NEMA requirements.**

Keywords— capacitors, dv/dt filters, inductors, motor drives

I. Introduction

The use of switching power converters to drive motors has several potential issues including motor winding insulation breakdown due to high *dv/dt* [1]–[3], bearing degradation due to electrical currents in the rotor [4]–[6], and high voltage pulses induced by long motor cables [7]–[9]. Many different solutions have been proposed and implemented in order to mitigate these issues. For *dv/dt* reduction, many types of output filters can be incorporated in the circuit [10]. For bearing current reduction, insulated bearings, shaft brushes [11], or capacitive shunts [12], [13] can be applied. Various filter types are also used to limit voltage overshoot on long motor cables [14]. The recent introduction of silicon carbide (SiC) drives will make many of these issues worse due to the very fast switching transients achievable with wide bandgap devices.

A. Standards for Inverter–Fed Motors

In order to allow for proper inverter and motor compatibility that avoids many of these issues, industry standards such as NEMA MG 1 [15] and IEC 60034–25 [16] specify limits for parameters such as minimum inverter voltage rise times and peak voltages. The NEMA MG 1 Part 31 standard specifies limits on rise time and overshoot for connection to inverter–rated motors. It specifies that the 10%–90% voltage rise time should be greater than 100 ns. For a 460 Vrms system, the peak line–line voltage should be less than 1431 V and the motor should operate partial discharge free at voltages below 1025 V [15]. The filters in this paper are designed to provide rise times greater than 100 ns and peak voltages less than 1025 V to ensure compatibility with inverter–rated motors designed to the NEMA specification.

In many cases, silicon IGBT based drives can be directly connected to inverter–rated motors while meeting the NEMA specification without adverse effects on motor life. However, with recent improvements to silicon IGBTs and the introduction of SiC devices, modern inverters may not be able to connect directly to inverter-rated motors without other mitigation techniques in order to meet voltage rise time and peak voltage constraints set out in the NEMA standard. Two filtering techniques to help meet these requirements are: 1) to switch the inverter at higher frequencies and attach an LC sine wave filter to the output, or 2) to switch the inverter at typical IGBT switching speeds and implement a damped LC *dv/dt* filter at the output. One comparison found that the SiC drive with the *dv/dt* filter using the second technique was the most efficient topology for a 10 kW motor drive application while providing comparable *dv/dt* performance to standard silicon IGBT drives [17]. One drawback of this method is that discrete output filters tend to be expensive and bulky, and it would be advantageous to decrease the size, weight, and cost of these *dv/dt* filters.

B. Fundamentals of Integrated Inductors, Capacitors, and Resistors for Filters

In a typical inverter output filter, discrete inductors and capacitors are used as depicted in Fig. 1a and they are connected together, possibly with damping resistors depending on the application. Other types of integrated inductors and capacitors have been proposed that integrate the terminals of the discrete components and arrange the structures in close physical proximity to one another. However, the fields are still contained in separate locations [18], [19]. This is shown schematically in Fig. 1b, where an electric field exists between the two inductor windings that serve as capacitor plates, and a magnetic field exists separately in the core.

This paper proposes a new type of highly integrated *dv/dt* filter that combines the necessary inductor, capacitor, and

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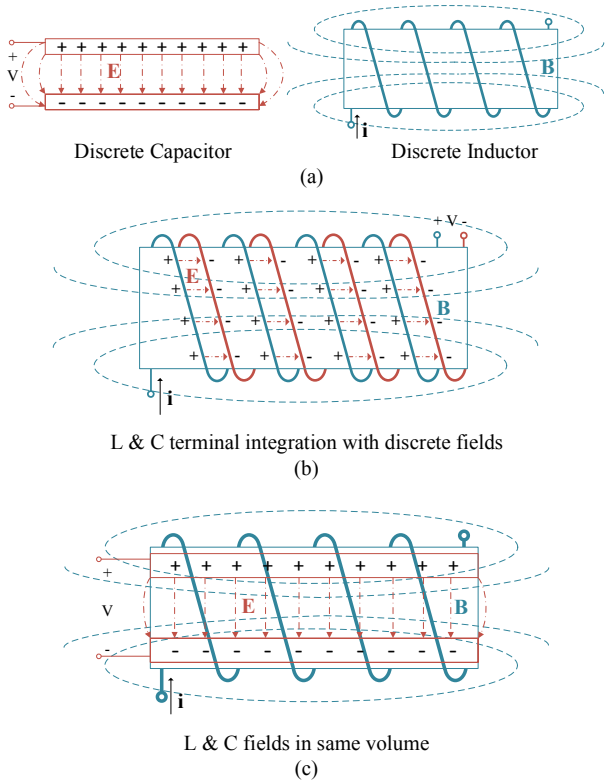

Fig. 1. Different stages of LC filter integration. A conceptual view of a discrete inductor and capacitor (a), a terminal integrated device with discrete fields (b), and a field integrated device (c).

damping resistor of the inverter output *dv/dt* filter into a compact and simple to manufacture structure. The integrated structure may be incorporated into the inverter output bus bars or cable conductors. This integrated filter arranges the capacitor and inductor structures so that the magnetic field of the inductor and the electric field of the capacitor occupy a common volume [20]. This is shown schematically in Fig. 1c, where the electric field and magnetic field both exist in the same core.

II. Integrated Filter for dv/dt Reduction

A. Topology

The proposed integrated *dv/dt* filter design turns a copper bus bar or cable into a highly integrated inductor, capacitor, and damping resistor. Alternating layers of plastic film and metal foil are wrapped around the bus bar in a spiral. Capacitance is exhibited between the metal foil layers, as in conventional film capacitor construction. In addition, if the foil winding incorporates magnetically permeable material, the series inductance of the bus bar is enhanced in the winding region. The parasitic magnetic, conduction, and dielectric losses in the device are tailored to provide the necessary damping.

Fig. 2 shows a schematic view of the proposed device with critical dimensions labeled. In Fig. 2a, the phase current passes through the bus bar from L+ to L–. One capacitor terminal C+

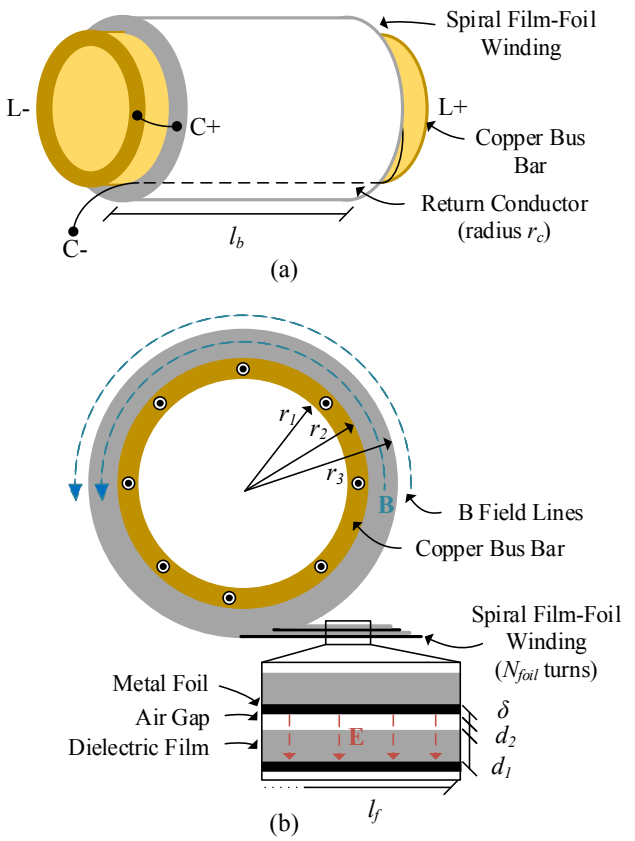

Fig. 2. A schematic view of the proposed filter integrated into a bus bar (a) and a cross section view showing magnetic field lines caused by current through the bus bar in blue and electric field lines in the dielectric material in red (b).

is connected to the bus bar output L–. The other capacitor terminal C– loops back through the middle of the foil winding and is connected to the neutral point in a 3–phase star configuration. The L+ side of the bus bar can be connected to the inverter phase pole, and the L– side of the bus bar can be connected to the motor or motor cable. In Fig. 2b, a cross section view is shown with magnetic field lines due to current through the bus bar shown as blue arrows. Some of this field is in the region of the capacitor winding and some is outside it. Electric field lines in the dielectric between the foil layers are shown as red arrows.

B. Analytical Model

The proposed device shown in Fig. 2 can be modeled using the circuit model shown in Fig. 3. Besides the main inductance and capacitance, only parasitic elements that are relevant to the application are shown. For the inductor portion of the circuit, the model includes the air core self–inductance of the bus bar L_a, the extra inductance due to the inclusion of magnetically permeable material L_p, the permeable material core loss R_p, and the resistance of the bus bar R_b. For the capacitor portion of the circuit, the model includes the capacitance C, the capacitor series resistance R_1, the capacitor parasitic inductance L_1, the extra inductance in the capacitor leg due to

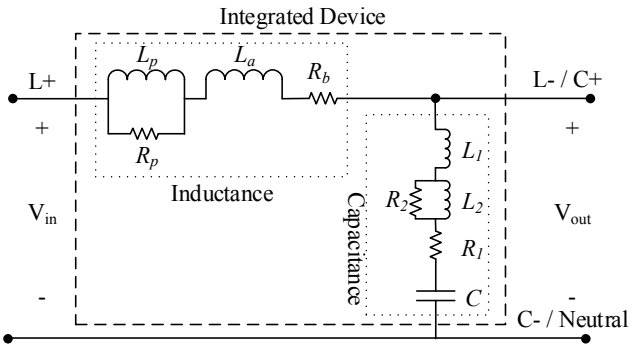

Fig. 3. Detailed per phase circuit model of the integrated filter showing series inductance, shunt capacitance, relevant parasitic components, and damping elements.

the inclusion of magnetically permeable foil material L_2, and the permeable material loss R_2. The parasitic loss components R_p, R_b, R_1, and R_2 provide the damping in the circuit.

Most of the circuit model parameters from Fig. 3 can be calculated analytically based on the dimensions depicted in Fig. 2 and the properties of the materials. The air core inductance L_a outside the winding region with permeable foil can be calculated using the Biot–Savart method for self–inductances [21] as shown in (1). It depends on the length of the bus bar l_b and the outer radius of the winding r_3 assuming the bus bar is hollow in the middle.

$$L_a = \frac{\mu_0}{2\pi}\left[l_b \ln\left(\frac{l_b+\sqrt{l_b^2+r_3^2}}{r_3}\right) - \sqrt{l_b^2+r_3^2}+r_3 \right] \tag{1}$$

The additional inductance due to the permeable material L_p is a function of the bus bar length l_b, the inner and outer radii of the winding r_2 and r_3, and the effective average permeability of the winding μ_{reff} as shown in (2). The effective permeability of the composite dielectric and metal structure can be estimated based on a stacking factor approximation [20].

$$L_p = \frac{\mu_0\mu_{reff}}{2\pi}\left[l_b \ln\left(\frac{l_b+\sqrt{l_b^2+r_2^2}}{r_2}\right) - \sqrt{l_b^2+r_2^2}+r_2 - l_b \ln\left(\frac{l_b+\sqrt{l_b^2+r_3^2}}{r_3}\right) + \sqrt{l_b^2+r_3^2} - r_3 \right] \tag{2}$$

The resistance of the bus bar R_b is a function of the bus bar length l_b, resistivity ρ_b, and cross sectional area as shown in (3). For the case of a hollow copper tube, the cross sectional area is a function of its inner radius r_1 and outer radius r_2. Note that in many cases, this resistance will be dominated by the connection contact resistance of a few milliohms. The value of the core loss resistance R_p will be determined experimentally.

$$R_b = \frac{\rho_b l_b}{\pi r_2^2 - \pi r_1^2} \tag{3}$$

For the capacitor leg of the circuit, the capacitance can be calculated by using the capacitance equation in (4). The capacitance C is a function of the length of the bus bar l_b, the length of the winding l_f, the thickness of the dielectric film d_1, and the thickness of the air gap between layers d_2. Also included are the relative permittivity of the dielectric film ε_{r1} and the relative permittivity of the air gap ε_{r2}. The factor of 2 accounts for the two layers of dielectric in the winding.

$$C = \frac{2\varepsilon_0 l_b l_f}{\frac{d_1}{\varepsilon_{r1}} + \frac{d_2}{\varepsilon_{r2}}} \tag{4}$$

The capacitor series resistance R_1 given in (5) is a function of both the capacitor dielectric loss and the conduction loss. The dielectric loss is highest at lower frequencies and depends on the dissipation factor of the dielectric material DF, the inverter switching frequency f_{pwm} and the capacitance C. The conduction loss is a function of the resistivity of the metal foil ρ_c, the length of the bus bar l_b, the thickness of the metal foil δ, and the length of the foil winding l_f.

$$R_1 = \frac{DF}{4\pi f_{pwm} C} + \frac{\rho_c l_b}{\delta l_f} \tag{5}$$

The parasitic inductance L_1 of the capacitor leg of the circuit is given in (6). This inductance is a function of the inner radius of the capacitor winding r_2, the radius of the return conductor r_c, and the length of the bus bar l_b. The return conductor passes back to the output side of the bus bar through the middle of the film–foil winding forming a loop arrangement similar to a shorted coaxial cable.

$$L_1 = \frac{\mu_0}{2\pi}\ln\left(\frac{r_2}{r_c}\right) l_b \tag{6}$$

The additional parasitic inductance L_2 of the capacitor leg of the circuit due to the permeable metal foil is given in (7). This inductance is a function of the outer radius of the capacitor winding r_3, the inner radius of the capacitor winding r_2, the length of the bus bar l_b, the effective permeability of the winding μ_{reff}, and the number of turns of the film and foil winding around the bus bar N_{foil}. This equation captures the parasitic inductance due to the magnetic field in the winding region caused by the capacitor current. The value of the core loss resistance R_2 will be determined experimentally.

$$L_2 = \frac{\mu_0\mu_{reff}}{2\pi N_{foil}}\ln\left(\frac{r_3}{r_2}\right) l_b \tag{7}$$

III. Design of Integrated dv/dt Filters

Many of the circuit model parameters in (1–7) are strongly influenced by the material properties of the metal foil and

dielectric film used to construct the filter. In order to design integrated *dv/dt* filters in bus bars, dielectric film and metal foil materials with favorable properties will be selected first, then a design routine will be developed to determine material dimensions needed to achieve desired rise times and peak voltages.

A. Material Selection

The dielectric film should be chosen for its permittivity, dielectric loss properties, voltage rating, and temperature rating. The experimental prototypes in this paper use polyimide film. Polyimide film represents a good mix of all of these properties, exhibiting a high relative permittivity for polymer films, a reasonable amount of dielectric loss to assist in damping, a good voltage rating, and excellent temperature resistance. The high temperature capability is important in this application since the damping loss occurs inside the filter itself and not in a discrete damping resistor. Other high temperature films such as polytetrafluoroethylene (PTFE), polyetherimide (PEI), and flexible glass may also be of interest in this application.

For the metal foil, the most important properties are its permeability, resistivity, and core loss properties. The experimental prototypes in this paper use grain–oriented silicon steel foil. This foil has good magnetic properties and its increased electrical resistivity over aluminum assists in the damping action of the circuit. Other metal foils that may work in this application include nickel, carbon steel, and various nickel–iron alloys.

B. Design Procedure

The rise time of the filter response can be estimated as a function of the total inductance $L_a + L_p$, and the capacitance C for a simple LC circuit by utilizing the inverse of its resonant frequency. However, the parasitic and damping elements in the circuit affect the rise time as well, and these elements must be included to ensure that the final rise time and overshoot meet the required specifications and match experimental results for this application. Due to the nature of this topology with permeable material and damping elements incorporated in the integrated device, this simple approach does not provide an accurate calculation of the rise time for design purposes. In addition, adjusting many of the filter dimensions during the design process changes the inductance, capacitance, and parasitics of the circuit simultaneously. For these reasons, a calculation and simulation procedure was developed to design the experimental prototypes in this paper.

With the dielectric film and metal foil already selected above, the next step is to choose the length and diameter of the bus bar based on system geometric constraints and current carrying requirements. Then, the free variable to adjust in order to obtain the desired rise time is the length of the film/foil winding l_f.

The parameters in the detailed circuit model in Fig. 3 are calculated using (1–7) given the selected dimensions and material properties. The loss values R_p and R_2 are obtained by experimentally testing a sample coil/wrapping of the dielectric film and metal foil. These values are substituted into the transfer function (8) of the circuit model of Fig. 3. The transfer function is defined as a simple voltage divider. The values of the parameters calculated as (1–7) are assumed fixed, i.e. an operating point small–signal model since some of the parameters are subject to frequency and saturation dependencies. The response of this transfer function to a voltage pulse is then simulated in MATLAB. The rise time and peak voltage due to a voltage pulse can be obtained from the simulation results.

$$\frac{V_o}{V_i} = \frac{\frac{1}{sC} + R_1 + sL_1 + \frac{sL_2R_2}{sL_2 + R_2}}{\frac{1}{sC} + R_1 + sL_1 + \frac{sL_2R_2}{sL_2 + R_2} + sL_a + R_b + \frac{sL_pR_p}{sL_p + R_p}} \quad (8)$$

Next, the length of the foil/film winding l_f is adjusted, which simultaneously changes the capacitance C and the inductance L_p until the desired rise time is achieved. Note that other dimensions such as the bus bar length l_b, radius r_2, dielectric film thickness d_1, and foil thickness δ can also be adjusted within the limitations of material availability and design constraints in order to tailor the rise time and overshoot results.

IV. Experimental Results

The design procedure above is used to design and construct three devices to filter the output of a SiC inverter connected to a 460 Vrms induction motor. The desired rise time is 150 ns, which will meet the NEMA specification while accounting for extra margin to allow for saturation effects that can decrease the inductance and lower the rise time at high phase currents.

A. Prototype Filters

The prototype filters were constructed using 216 mm (8.5 in) lengths of 12.7 mm (0.5 in) diameter copper pipe as the bus bar. The ends of the pipe were pressed flat to form blade terminals. Alternating layers of 152 mm (6 in) wide, 25.4 μm (0.001 in) thick grain–oriented silicon steel and 50.8 μm (0.002 in) thick polyimide film were wrapped around the bus bars. These dimensions were selected to match readily available materials within the film capacitor and magnetic lamination industries. In the future, the materials may be custom designed for enhanced performance. An extra layer of polyimide film was used for electrical insulation between the bus bar and the inside of the film and foil winding. An end view of one of the prototypes is shown in Fig. 4a and a side view is shown in Fig. 4b. The connections are labeled to match Fig. 2 with one capacitor terminal C+ connected to the filter output L– and the other capacitor terminal C– passing back through the middle of the winding and coming out the output side of the filter in order to minimize the loop inductance.

B. Impedance Measurement Verification

An impedance analyzer was used to examine the impedance and phase of the bus bar filter components as a function of frequency. The impedance and phase with the impedance analyzer connected from C+ to C– across the

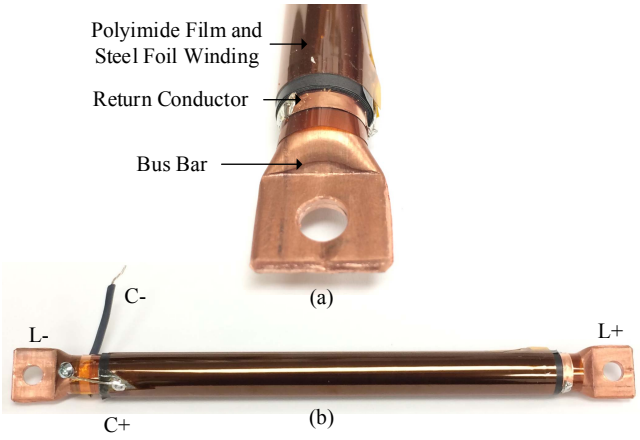

Fig. 4. Prototype filter end view close up (a) and side view with terminals labeled (b).

capacitor leg of the circuit is shown in Fig. 5a as circles. A curve fit was also performed on the data and is shown as a solid line. The impedance and phase from L+ to L– across the inductor leg of the circuit is shown in Fig. 5b as circles with the curve fit shown as a solid line.

The curve fits shown in Fig. 5 were calculated with the magnitude of the impedance of the inductor portion of the circuit model as given in (9) and the capacitor portion of the circuit model as given in (10) using the least squares method. The circuit parameter values calculated in (1–7) were used as initial values in the curve fitting routine. Minor error can be seen in the curve fit at MHz frequencies, and a model that accounts for the material nonlinearities could potentially fit the data more accurately in this frequency range. However, adding this model complexity was not found to have a significant impact on the accuracy of the rise time and overshoot simulation used to design the filter.

$$|Z_L| = \left[\left(R_b + \frac{1}{\frac{R_p}{(\omega L_p)^2} + \frac{1}{R_p}}\right)^2 + \left(\omega L_a + \frac{1}{\frac{1}{\omega L_p} + \frac{\omega L_p}{R_p^2}}\right)^2\right]^{\frac{1}{2}} \quad (9)$$

$$|Z_C| = \left[\left(R_1 + \frac{1}{\frac{R_2}{(\omega L_2)^2} + \frac{1}{R_2}}\right)^2 + \left(\omega L_1 - \frac{1}{\omega C} + \frac{1}{\frac{1}{\omega L_2} + \frac{\omega L_2}{R_2^2}}\right)^2\right]^{\frac{1}{2}} (10)$$

Table I compares the analytical values for the experimental prototypes calculated using (1–7) and the values determined from the curve fitting analysis of one of the experimental prototypes using (9–10). The values are in good agreement, especially considering the large variations possible with hand–built prototypes. Note that the analytical model for R_b does not account for contact resistance, which dominates this term in the experimental data.

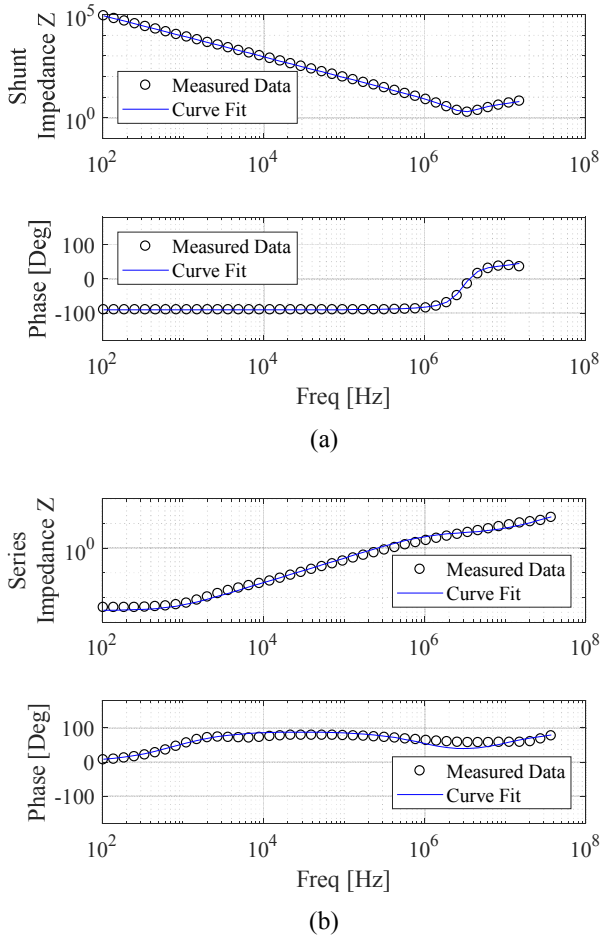

Fig. 5. Measured and calculated shunt impedance and phase of the filter from C+ to C– (a) and series impedance and phase of the filter from L+ to L– (b).

TABLE I. ANALYTICAL AND EXPERIMENTAL PARAMETER VALUES

Parameter	Analytical Model Value	Experimental Curve Fit Value
L_a	83 [nH]	78 [nH]
L_p	510 [nH]	550 [nH]
R_b	0.001 [Ω]	0.004 [Ω]
R_p	—	4 [Ω]
C	17.6 [nF]	17 [nF]
L_1	61 [nH]	50 [nH]
L_2	140 [nH]	100 [nH]
R_1	1.8 [Ω]	1.2 [Ω]
R_2	—	4 [Ω]

C. Motor Drive System Testing

The prototype filters were tested by connecting them to the output of a 3–phase silicon carbide inverter. Fig. 6a shows a schematic of the setup with the filter output connected to a cable, which is connected to an induction machine. The inverter was constructed using Wolfspeed CAS120M12BM2 1200 V SiC half bridge modules. The inverter is capable of

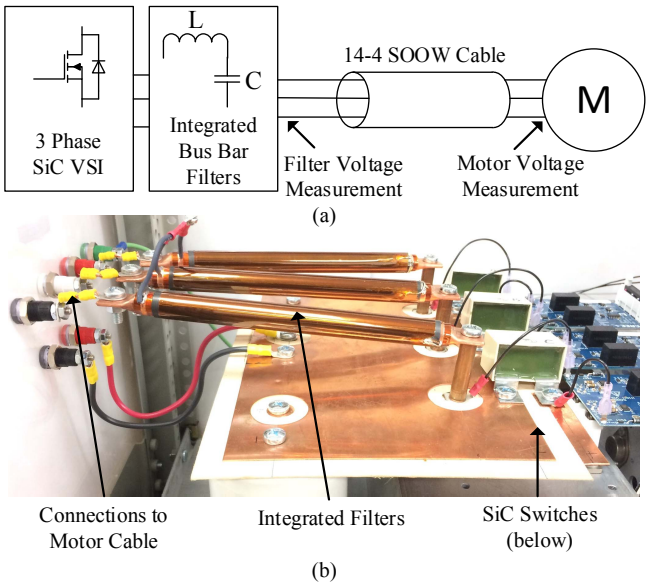

Fig. 6. Schematic of test setup (a) and a photo of the filters connected to a 3–phase SiC inverter (b).

voltage rise times much less than 100 ns depending on the gate resistance used. The L+ filter terminals are connected directly to the phase leg poles of the modules as shown in Fig. 6b. The L– terminals are connected to the motor cable, and the C– terminals are connected in a floating wye/star configuration. A 14–4 SOOW 600V cable is connected to a 460 V line–line 3–phase induction machine rated at 2.2 kW (3 Hp). The tests were performed at no load, as the rise time is a function of voltage and not phase current as long as the permeable foil is not saturated.

The inverter was run with a 700 V DC bus switching at 5 kHz. A line–line voltage rising edge waveform taken at the filter output is shown in Fig. 7a, showing the filtered waveform and an unfiltered waveform for comparison. The filtered 10% to 90% rise time is 161 ns and the peak voltage is 813 V. The filter increases the voltage rise time to a level that meets the NEMA MG 1 Part 31 specification while keeping the peak voltage within limits. If additional damping is desired to eliminate the overshoot, a dielectric with higher dissipation loss, or a metal foil with higher core loss could be selected.

The waveforms were also measured at the motor terminals with a 3–meter cable between the filter and the motor. The resulting waveform at the motor terminals is shown in Fig. 7b. The filtered rise time is 145 ns and the peak voltage is 932 V. Again, the filter increases the voltage rise time to a level that meets the NEMA MG 1 Part 31 specification while keeping the peak voltage within limits. Due to the fast rise times of SiC converters, the voltage doubling effect seen on long motor cables is already apparent at a relatively short cable length of 3 meters without a filter installed.

D. Comparison to Analytical Model

In order to validate the transfer function based voltage rise time simulation used in the design of the filter, the simulated

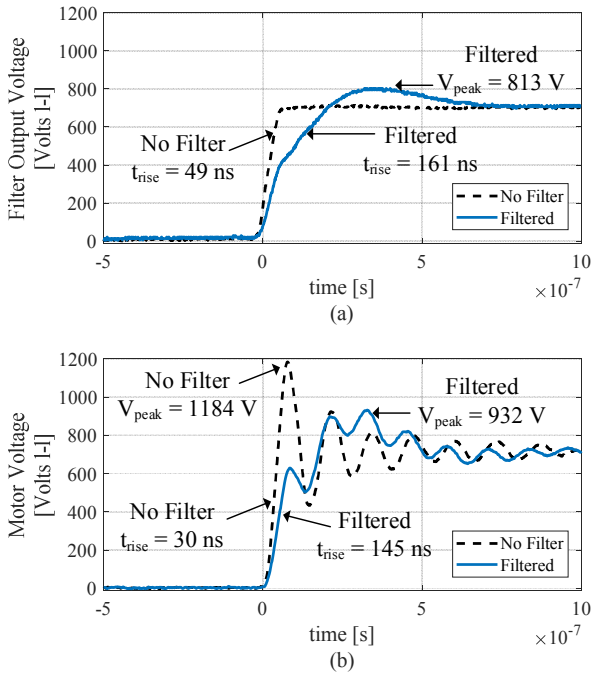

Fig. 7. Line–line voltage rising edge showing *dv/dt* reduction at the filter output (a) and line–line voltage rising edge at motor terminals at the end of a 3–meter cable (b). Both waveforms are compared to waveforms without the filter installed.

voltage rising edge waveform generated via (8) is compared to the experimental voltage rising edge waveform in Fig. 8 as seen at the output of the filter. There is good agreement between the simulation and the experimental results, validating the simulation used to design the filter. A comparison of the simulated versus experimental rise time and overshoot values is given in Table II.

The difference between the simulated values and the experimental values for the rise time and peak voltage does not exceed 5%. This simulation provides a simple, accurate way to estimate the rise time and overshoot in order to properly design and construct integrated *dv/dt* filters, while accurately accounting for the effects of parasitics and integrated damping elements.

E. Damping Losses

The losses in each filter due to the damping elements can be estimated using (11), which accounts for the energy dissipated in the filter each time the filter capacitor is charged [17]. For the experimental prototypes, the estimated loss is 18.5 W/phase at a 5 kHz switching frequency. This loss is primarily a function of DC link voltage and not phase current, so efficiency at full load on larger motor systems can still be very high. This value was verified by comparing the no load power consumption of the entire drive and motor system with and without the filter installed. The additional power consumed at the system level with the filter in the circuit was 60 Watts, or 20 W/phase. This result is in good agreement with the

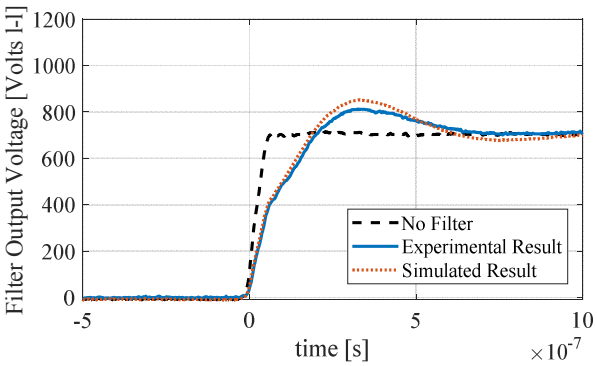

Fig. 8. Experimental line–line voltage rising edge at the filter output compared to the simulated response based on the analytical model used to design the filter.

TABLE II. SIMULATED AND EXPERIMENTAL RESULTS

Parameter	Simulated Value	Experimental Value	Difference
t_{rise}	152 [ns]	160 [ns]	5 [%]
V_{peak}	852 [V]	818 [V]	4 [%]

estimated filter loss above. The loss in this filter is comparable in magnitude to the loss in the discrete component *dv/dt* filter tested in [17]. Filters of this type, when connected to a SiC inverter running at load, can have a higher system efficiency than a standard silicon IGBT drive without filters [17].

$$P_D \approx C\left(\frac{2V_{DC}}{3}\right)^2 f_{pwm} \tag{11}$$

Since the damping losses are integrated into the filter, the filter temperature can be a concern. Fig. 9 shows a thermal image of the prototype filters operating at thermal steady state with a temperature rise of about 80 degrees C above ambient in the film/foil winding with no air movement. This operating temperature is well within acceptable limits for the materials used to construct the filter, and can be lowered with the use of a cooling fan if desired.

V. CONCLUSION

In this paper, a highly integrated filter for *dv/dt* reduction in motor drives was introduced, representing a potentially low cost, simple to manufacture, and plug and play solution for motor drive systems with fast voltage rise times. The incarnation in this paper was designed and built into 3–phase AC bus bars. An analytical model based on the filter equivalent circuit, physical dimensions, and material properties was developed. The model was used to simulated the voltage rise time and overshoot at the output of the filter due to a voltage pulse from a motor drive.

Experimental prototypes were constructed based on the proposed design procedure. These prototypes were tested on a silicon carbide drive connected to an induction machine that

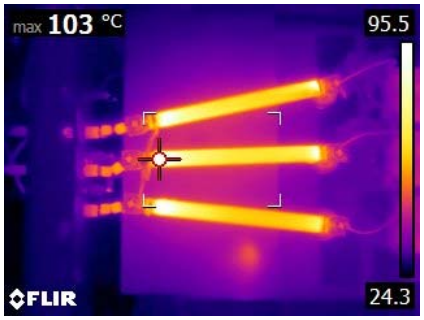

Fig. 9. Thermal image of filters operating at steady state with ~80 degrees C temperature rise above ambient at the hot spot due to the damping incorporated into the integrated device.

validated the accuracy of the model. The prototype integrated *dv/dt* filters increased the voltage rise time, while keeping the overshoot within limits in order to meet the NEMA MG 1 Part 31 specification for inverter–rated motors. The integrated *dv/dt* filters also demonstrated voltage ringing reduction at the motor terminals over a 3–meter cable length. The filters had comparable losses to other damped *dv/dt* filters tested in the literature.

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