Comparison Between Desaturation Sensing and Rogowski Coil Current Sensing for Shortcircuit Protection of 1.2 kV, 300 A SiC MOSFET Module

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***Abstract* — Silicon Carbide (SiC) MOSFET devices have small internal inductance and small on state resistance, resulting in a huge *di/dt* which will cause the current to rise to a high level very fast during shortcircuit (SC), causing possible destruction of module due to excessive dissipated energy or high overshoot during the turn-off. Therefore, fast and reliable protection circuit is important to detect the SC as fast as possible to minimize the power dissipation in the components during the fault, thus preventing the device from overheating and destructing. Furthermore, soft turn-off is required to avoid high voltage spike during the turn-off of the fault current. This paper compares and evaluates the SC performance of two different protection methods on CREE 1.2 kV, 300 A SiC MOSFET module. The first protection method utilizes desaturation technique (DeSat), while the second method utilizes a Rogowski coil to sense the current through the device. Experimental results are analyzed to determine which protection method behaves better under different operating conditions.**

Keywords—desaturation, overcurrent, Rogowski coil, shortcircuit, SiC MOSFET

I. INTRODUCTION

SiC MOSFET as a wide-bandgap (WBG) device has superior performance for its high breakdown electric field, high working temperature, fast switching speed and low on-state resistance [1]. Fast switching speed enables high switching frequency, which improves the power density of converters. In the past few years, cost of SiC MOSFET is decreasing due to the increased usage in industry applications because of the benefits that the devices offer. Hence, SiC MOSFET presents great potential in medium-voltage (MV) high power applications, and can potentially replace MV IGBT devices [2].

Failure modes such as shortcircuit can potentially cause excessive currents and excessive power dissipations which very quickly overheats the power module and destroys it. In order to prevent catastrophic damage, detection and protection must be implemented to reduce or turn-off the overcurrent during the fault condition [3]. When overcurrent (OC) or SC occurs, SiC MOSFETs can only withstand these severe conditions several μs, evidencing for some of the cases lower robustness than the Si IGBT counterpart, where the typical SC withstanding time is 10 μs at the high operating temperature [4]. From thermal point of view, lower SC withstand capability for SiC MOSFET device is expected due to a smaller chip area and higher current density than Si IGBT device. In the event of SC, the gate drive circuit must be able to detect the fault condition and safely shut the device off before a failure occurs [5]. Since SiC MOSFET power module package usually has low internal inductance and the device has low on state resistance, fast SC di/dt will cause the current to rise fast to a high level causing possible destruction of the module due to excessive dissipated energy or high overshoot during the turn-off. Therefore, response time is critical for the SC protection of SiC MOSFETs due to the limited SC withstand time [6]. Robust SC protection with fast detection and reaction, combined with turn-off in a safe manner is absolute necessity.

Several methods exist to realize OC and SC protection. The most common SC indication method for MV high power IGBT applications was based on the collector-emitter voltage measurement, called desaturation method (DeSat). It is also possible to use current sense IGBTs in which a fraction of IGBT cells in the chip are used for current observation. Intelligent power modules often utilize such a solution. Another possibility is to analyze the gate voltage of the IGBT or the behavior of the gate charge at turn-on. The shortcircuit effects the gate voltage and this property can be used in fast fault monitoring. The fourth way for protecting IGBT is based on the collector current measurement. Current measurement can be realized by a shunt resistor, a current transformer, a Rogowski coil, or by voltage measurement over the power module parasitic inductance [7]. As noted in the literature [8 - 9], whichever protection is used, its implementation needs to have following targets:

- fast detection and reaction time which will impact the current peak level, limiting the overheating and current stresses
- responsive for all SC types and not degrade conduction or switching characteristics
- turn-off in a safe manner
- inexpensive and easy implementation\integration in any gate driver design
- high noise immunity

In this work, two SC protection circuits are compared and evaluated. The first is DeSat technique while the second method of protection is based on sensing the current through device. The current will be monitored by Rogowski coil.

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II. TYPES OF SHORTCIRCUIT AND TESTING SETUP

In the half-bridge configuration, 2 types of SC exist. Fig. 1 shows that one type of fault is referred to as shoot-through, while the other is referred to as shortcircuit at the load, or load fault. Focus is set on the bottom switch (Q2) in the half-bridge.

A. Shoot-through type of shortcircuit

When conduction time of both switches in half-bridge configuration overlap, a shoot-through event is created. This can happen in case of a transistor or diode destruction, failure in the controller or signal transmitters, due to noise induced malfunction of the switch-on and switch-off signals etc. Depending on conditions at what shoot-through occurred two possible cases exist. The first case is called "Fault Under Load" (FUL) and the second is "Hard Switching Fault" (HSF) [8 - 13].

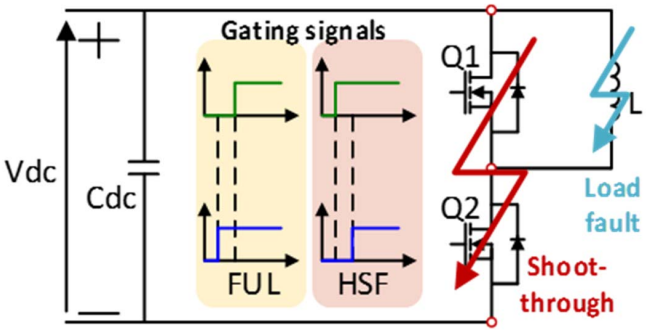

Fig. 1. Types of shortcircuits in the half-bridge configuration

1) FUL

FUL is a type of fault that occurs when the device is on and conducting. Referring to Fig. 1, initially device Q2 is gated on and it is carrying steady current within its ratings. Therefore, voltage across device V_{ds}^{Q2} is low. Fault in the system is created by the turning on of the complementary switch, in this case Q1, thus causing the shoot-through event. Due to a very low stray inductance in the current path, current rise (di/dt) in this case is severe.

2) HSF

HSF fault occurs when the device channel is not opened, and the device is directly gated on into the fault. The inductive load from Fig.1 is shorted by the switch Q1 being on. Switch Q2 is off, meaning that device is holding full dc link voltage. Fault is imposed to the system when Q2 switched on. Upon application of the gate signal to the Q2 and following gate-source voltage reaching gate threshold voltage, current begins to rise. Similar as in FUL case, very low stray inductance will cause a rapid current rise.

B. Load fault type of shortcircuit

Due to an incorrect wiring, dielectric breakdown of load, shortcircuit of the windings of a motor, ground fault etc. load fault type of shortcircuit may occur (Fig.1) [11]. In this case, inductance of the load wire, motor cable or the rest inductance of the motor windings plays a significant part in the behavior of the SC. Current slope is determined by that inductance. Therefore, location of the where the SC occurs, is of great importance, because it will determine fault inductance and hence current slope. There will be high current slope and higher stress to device when the SC happens near the module terminals and slower current slope and lower stress when the SC happens on the motor winding. This type of SC is less stressful to device than the shoot-through types, often called overcurrent event.

C. Shortcircuit protection testing setup

Fig. 2 shows simplified schematics of testing setup.

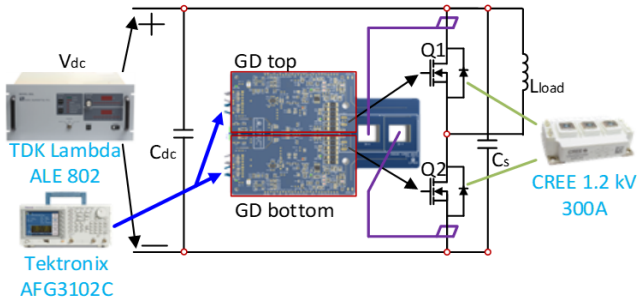

Fig.2. Shortcircuit protection testing setup

The half-bridge SiC MOSFET power module used for testing was a Cree 1.2 kV, 300 A module [14]. The gate driver used for driving the SiC power module is described in detail in [15-16]. This particular gate driver is chosen because of an integrated Rogowski coil sensor used for protection (purple color on Fig. 2.). This gate driver also provides a chance to protect the device via the DeSat method. Principle of operation and schematics of the protection mechanism will be presented in the forthcoming sections. Soft-turn off option, called Two-Level Turn-Off (2LTO), is also provided with the used gate driver. The second voltage level is set to be 7 V, while time spent in this mode is set to be 750 ns to successfully mitigate voltage overshoot during turn off. Used high-voltage power supply is TDK Lambda ALE 802 30 kV with the dc link capacitor of 132 µF. Applications usually require that decoupling capacitors are placed close to the SiC MOSFETs to minimize the equivalent power loop parasitic inductance. During a shortcircuit, most of the fault current is supplied first by the decoupling capacitor C_s due to relatively lower high frequency impedance, and then by the energy storage capacitor C_{dc} if SC is not interrupted. Decoupling capacitor is 1 µF, and the load inductor is set at 8 µH. Gating signals were created by a function generator and transmitted to the gate driver over fiber optic cables. All on-board measurements such as, gate-source voltage, on-board Rogowski current sensor, fault signal and DeSat waveform, are measured with low voltage passive probes. Current in the system is also measured with commercial high current Rogowski current probe to get a full waveform of current during a SC, as the on-board Rogowski probe is not intended to measure high SC currents and will saturate. Voltages across devices are measured with high voltage differential probes.

III. BEHAVIOR IN THE SHORTCIRCUIT EVENT

In order to define important comparison points of SC protections, unprotected non-destructive SC event is created in the system (load fault close to the half-bridge terminals).

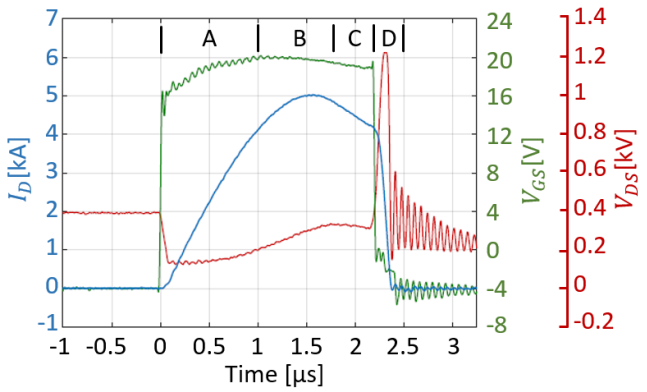

Fig. 3. Experimental waveforms of SC without any protection

Typical experimental waveforms of such SC can be observed in Fig. 3. SC gate signal is limited to be 2.2 μs, while the dc link voltage is $V_{dc} = 400\ V$.

Four distinctive phases can be identified. In phase A, current starts to rise due to applied gate signal. Current rise (di/dt) is dictated by the inductance in the path (stray inductance of the module and additional inductance of the load wire), transistor characteristic (threshold voltage and transconductance), gate driver parameters (gate resistor and applied V_{GS} voltage) and dc link voltage. Voltage over the device drops to a lower value, and that value is determined by parasitics of the device (R_{DSon}, $L_{stray}\frac{di}{dt}$, C_{DS}). According to the Fig.3, at the beginning di/dt was approximately 5 A/ns, which implies that current rises very fast and can reach peak values shortly after applied gate signal which can be destructive due to excessive dissipated heat. Therefore, protection detection and reaction times are crucial. Phase B starts when current reaches a level where SiC MOSFET starts its transfer from the ohmic region to the saturation region and voltage over the SiC MOSFET device builds to the dc link voltage value. At the beginning of Phase C, due to an increase of resistance in the module when dissipated energy is heating the module, current will drop off from its peak. Following that drop, the device is exposed to both high current and high voltage. If the protection still did not react before entering this phase, it is crucial for protection to react as fast as possible, as now energy dissipation and thus heat is tremendous. Since withstand time of SiC device is not as long as the IGBT device, thermal runaway may occur. Start of the Phase D occurs when the gate signal goes low, and the SiC device is turned off. Due to di/dt of the decaying current, V_{DS} voltage will rise significantly over the device's parasitic inductances threatening to destroy the device due to overvoltage. Fig.3. indicates that voltage overshoot in this case is more than 800V, which gives more than 1.2 kV voltage across device. Since 1.2 kV is rated voltage and testing is done on 400 V, it can be expected that on higher dc bus voltages, voltage across the device will be even higher and possible destruction due to overvoltage may occur. Therefore, it is recommended to turn off the device softly due to high current in the switch. One of the methods to turn of device in a safe manner and suppress overvoltage is Soft-turn off [17].

According to the behavior of the device during the SC and all of the previously stated, two protection methods will be compared in: A. Time spent in SC (time from beginning until the end of SC) [μs], B. Detection time (time from beginning to the detection) [ns], C. Reaction time (time from the detection until soft turn-off (STO) is initiated) [ns], D. Energy dissipated on devices during SC [J], E. Current peak [kA] and F. Voltage overshoot (max measured overshoot) [V].

IV. Desaturation Protection Method

A. Protection mechanism

DeSat protection has been the most used shortcircuit protection in MV IGBT applications in the past due to its reliability, low implementation cost and simplicity. Most of the literature describe the principle of operation and how to tune DeSat protection in general for IGBTs. Since SiC devices emerged in the market, design and application engineer are trying to adjust and implement DeSat method of protection to save devices from destruction. DeSat circuit that is implemented in the gate driver is shown on Fig. 4.

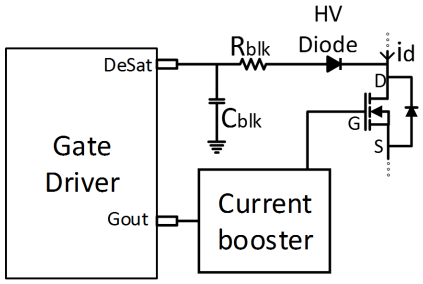

Fig. 4. Desaturation protection circuit

As depicted in Fig.4, the DeSat protection circuit is similar to conventional DeSat for IGBT. There is an output blanking RC filter and high voltage blocking diode. The output blanking RC filter has two purposes: First, the RC filter dumps noises coming from the energy part of circuit at turn on event. Second, blanking capacitor C_{blk} ensures that there is no nuisance tripping during turn-on process by creating blanking time. During turn on, capacitance is charging from internal current source and preventing sensing the V_{ds} voltage due to the oscillations occurring at that time. If sensing is enabled during turn-on, protection would be falsely triggered. This period is called blanking time. Resistor R_{blk} limits the current level drawn from the gate driver when a large negative voltage spike on the DeSat pin occurs because the anti-parallel diode can have a large instantaneous forward voltage transient [3]. The purpose of high voltage DeSat diode is to block high voltage during the period when the switch is blocking voltage and to conduct forward (sensing) current when switch is conducting. Chosen diode needs to be one with very fast reverse recovery and low output-capacitance to minimize the effect from high dv/dt of device switching [6].

The process of tuning DeSat protection is described in next few steps. Firstly, DeSat threshold is set according to the output characteristic on the 150^oC. In that case false tripping will be avoided on 150^oC if the threshold is set according to the low temperature one. According to the characteristics of the used SiC module, chosen current at which protection would react is chosen to be 600 A, and corresponding voltage would be 6 V. Because of the voltage drop across the blanking resistor and high

voltage blocking diode, DeSat threshold voltage is set to be 7 V. Secondly, the RC blanking filter is set according to the switching test on high temperature in a manner that noises coming from power stage do not cause false triggering. Furthermore, capacitor is chosen to be as small as possible so that blanking time is as short as possible since the turn on process is fast. Therefore, $C_{blk} = 24\,pF$ and $R_{blk} = 470\,\Omega$. The Driver IC already has implemented blanking time of 250 ns and additional 170 ns from blanking capacitor will add up to around 420 ns blanking time. With this configuration of DeSat circuit, without false tripping in normal operation, SC protection can be tested and evaluated.

B. *Experimental results*

Fig. 5 shows waveforms of device under FUL condition on 600 V dc bus. It is observable that waveforms for both cold and hot cases are very similar. Differences are small, but totally expected. For instance, in the hot case the module enters a SC event a little bit before than in the cold case. This occurs because the threshold of the device in the hot case is lower and the device starts conducting faster. Therefore, all of events during SC happen a little bit before than they occur in the cold case. Also, current peak is smaller in the hot case because resistances are higher in the system due to increased temperature. As a consequence of this, voltage overshoot will be smaller since smaller current peak is being interrupted. Because the behavior is similar for both temperatures (for both FUL and HSF), only the cold case will be described.

1) *FUL*

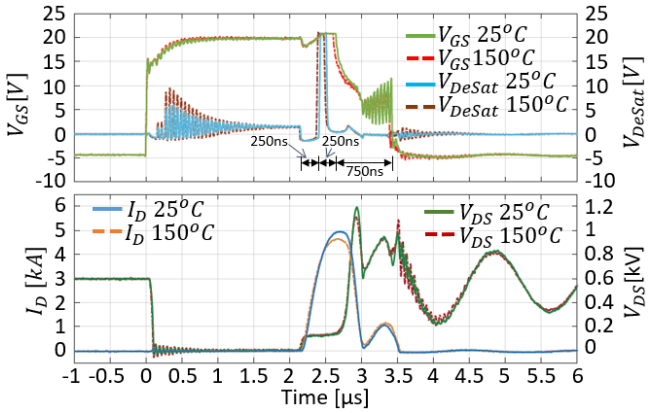

Fig.5. 600 V FUL experimental waveforms of DeSat

Fig.5 shows that device was conducting prior to SC for 2.2 μs. When SC occurs with the top device turn-on, current starts rising with huge $di/dt \approx 15\,A/ns$. Voltage across device jumps to a value that is in this case around 130 V due to parasitics in the module. Meanwhile, DeSat pin is pulled down for 250 ns (internal behavior of driver IC current source), after which it starts sensing. When DeSat pin starts sensing, it immediately jumps to a 20 V because voltage over device is approximately 130 V. This value of 20 V is limited by IC, and voltage cannot go above that value. Driver IC processes that information for 100 ns, which is standard processing time for input signals. After those 100 ns, DeSat pin is pulled low for 150 ns which is DeSat-2LTO initiation time determined by Driver iC. This result in reaction time being 250 ns. After that 2LTO is initiated and device goes into soft-turn off process which lasts 750 ns. Voltage overshoot due to a negative di/dt in cutting of the 5 kA current was 600 V. During this 2LTO process, current is limited and devices are saturated due to a lower value of V_{GS} which is set to 7 V in this case. From V_{GS} waveform it is observable that oscillations in the gate loop exists during 2LTO. It seems that oscillations are unstable, but since 2LTO time is short, the device is turned off successfully. One more phenomenon from V_{GS} can be observed, which considers rise in voltage over 20 V during SC. This rise is caused by current i_{DG} flowing through the Miller capacitance. Due to presence of the gate resistor, voltage will rise (Miller effect). This is undesirable effect resulting in even lower $R_{DS_{on}}$. Low frequency oscillations after turn-off of the SC event are caused by snubber circuit resonating with the parasitic inductances of the power loop, while high frequency ones are result of resonance between parasitic capacitances of the module and parasitic inductances of the power loop. Energies dissipated in module are: $E^{25^oC} = 1.7\,J$ and $E^{150^oC} = 1.66\,J$, which are safe values according to [4].

2) *HSF*

Fig. 6 shows similar behavior as the FUL case. Detection and reaction times are same, as well as the time spent in 2LTO. The main difference is that the device was not conducting prior to SC. Behavior of the DeSat and gate-source voltage is identical as in the previous case. Overshoots in this type of SC reached similar values around 600 V. Miller effect is not so expressed in HSF due to low C_{rss} capacitance when blocking the voltage (smaller di/dt and peak current could be expected). The device was turned off safely in both 25^oC and 150^oC case. Energies dissipated in module are: $E^{25^oC} = 0.9\,J$ and $E^{150^oC} = 0.95\,J$.

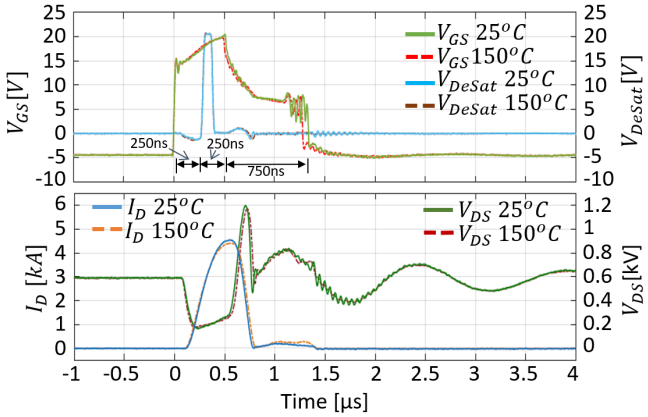

Fig.6. 600 V HSF experimental waveforms of DeSat

3) *Load fault*

Load fault is slower type of fault. Fig. 7 shows typical waveforms for a 600 V load fault with 8 μH load inductance. Desaturation protection system behaves completely different for 25^oC and 150^oC case. At time 0 μs, system starts conducting current. The DeSat pin starts sensing the current after 420 ns blanking time. DeSat waveform follows linearly current rise (measuring V_{DS}). Since DeSat protection is tuned according to 150^oC output characteristic, it is expected that for

cold case reaction current is much higher than what would be for a hot case. From Fig7. in cold case the device reaches DeSat threshold voltage (7 V) at 950 A, while for hot case treshold is reached at 650A, which is the approximate value that has been set. 2LTO initiates after 250 ns. After V_{GS} reach 7 V and current level drops, the device is safely turned off in both cases without overshoot reaching rated voltage and with insignificant energy dissipated to destroy the module ($E^{25^oC} = 160\,mJ$ and $E^{150^oC} = 70\,mJ$). However, if the inductance value was much higher than 8 μH, dissipated energy on 25^oC, due to higher threshold current, would be much higher and destruction could occur.

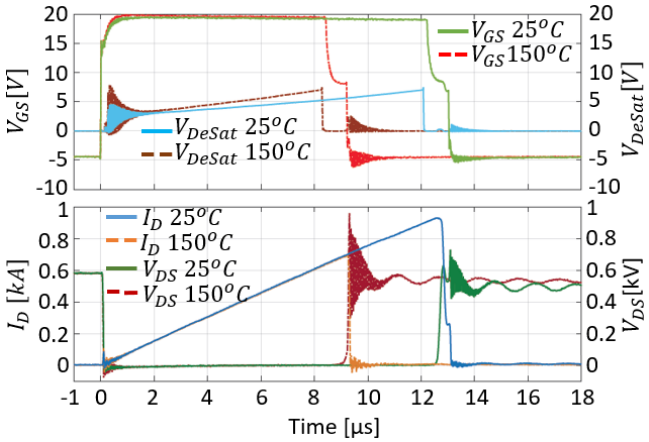

Fig 7. 600 V load fault experimental waveforms of DeSat

V. ROGOWSKI COIL CURRENT SENSE BASED PROTECTION

A. Protection mechanism

Protection mechanism is shown in Fig. 8.

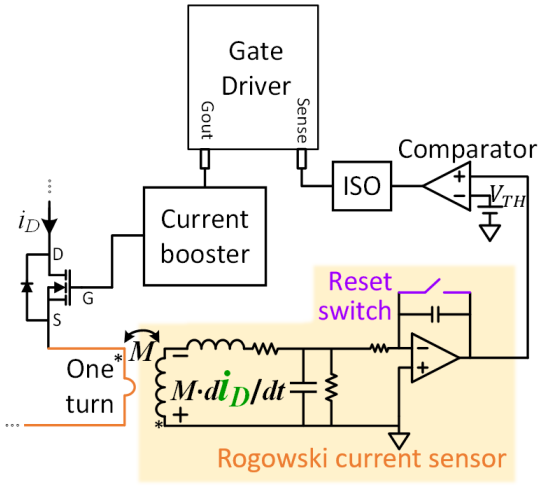

Fig. 8. Rogowski current sensor protection mechanism

The current sensor is composed from a Rogowski coil and an integrator. The Rogowski coil generates di/dt value of the sensed current scaled by a factor of the mutual inductance. The integrator is employed with the coil to convert the di/dt information back to the current information. An ideal integrator does not exist, so error of integration must be eliminated in order to sense correct switch current. In order to resolve it, an active reset switch is added to the integrator to reset the output to zero when the SiC MOSFET is switched off. Eventually the switch current sensor can sense pulsating current with correct amplitude [16]. Current waveform is then being sent to the comparator in which it is compared with the value that is set to be indicator of SC. Voltage source is set to a value that corresponds to a 600 A. When there is current higher than 600 A in the system, the comparator will generate a logic '1'. That signal is then transmitted through the digital isolator and sent to the sense pin of the Gate Driver IC on the isolated side. The original purpose of the Sense pin is overcurrent protection in the systems with IGBTs that have phase current measurement [18]. However, Sense pin in this particular gate driver, is utilized as a SC indicator. When logical '1' is on this pin, driver IC will initiate 2LTO, and system will be shut down in a safe manner.

B. Experimental results

Fig. 9 shows waveforms of the device under FUL condition on 600V dc bus. As it was case for DeSat protection, waveforms for both cold and hot case are very similar. Because of that, only the cold case will be described.

1) FUL

From Fig.9. the device was conducting prior to SC for 1.6 μs. When SC occurs, current start rising with $di/dt \approx 15\,A/ns$. Voltage across the device jumps to a value around 150 V. When the device current exceeds the threshold value of 600 A, a fault signal is generated by the comparator and is then transmitted to the sense pin (≈100 ns detection time). Driver IC processes that information for 100 ns, plus an additional delay time of 100ns which is sense-2LTO initiation time (200 ns reaction time). After that 2LTO is initiated and the device goes into STO process which lasts 750 ns. Maximum voltage overshoot was 200 V, and current peak 4.6 kA. During 2LTO process, current is limited and devices are saturated due to a lower value of $V_{GS} = 7\,V$. As in the DeSat case rise in V_{GS} voltage over 20 V occurs during SC for the same reasons. Oscillations after turn-off of the SC event occur due to same resonances as in Fig. 5. Energies dissipated are: $E^{25^oC} = 0.85\,J$ and $E^{150^oC} = 0.9\,J$.

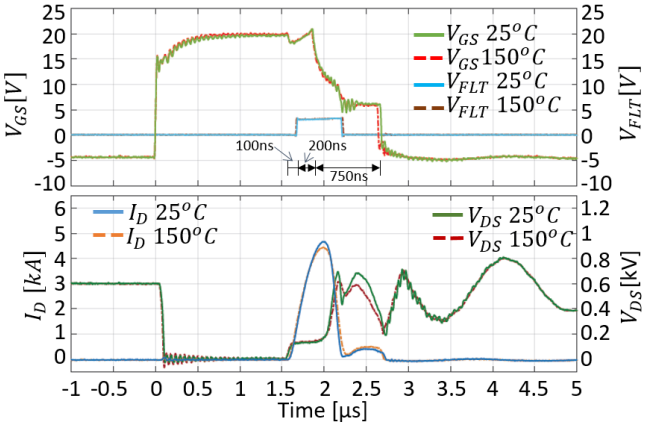

Fig. 9. 600 V FUL experimental waveforms of Rogowski protection

2) HSF

Fig. 10 shows similar behavior as the FUL case. Detection and reaction times are same, as well as the time spent in 2LTO. The main difference is that the device was not conducting prior

to SC. Behavior of the fault and gate-source voltage is identical as in the previous case, except for oscillations. Overshoot in this case was observed to be 300 V. The device was turned off safely in both the 25^oC and 150^oC cases. From V_{GS} waveform observation, it can be seen that oscillations in the gate loop exist during 2LTO, same as they existed in the DeSat protected case. It seems that those oscillations are unstable, but since 2LTO time is short, device is turned off successfully. Energies dissipated are: $E^{25^oC} = 0.9\ J$ and $E^{150^oC} = 1\ J$.

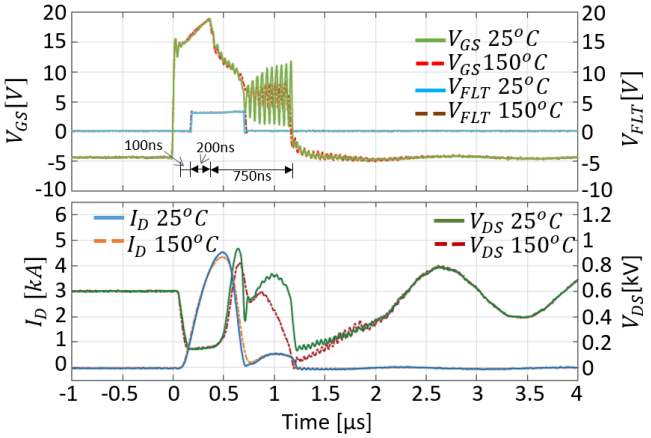

Fig.10. 600 V HSF experimental waveforms of Rogowski protection

1) Load fault

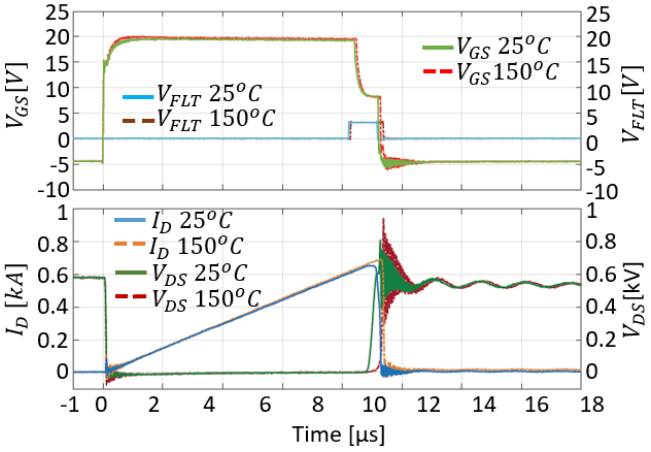

Fig. 11. 600 V load fault experimental waveforms of Rogowski protection

Fig. 11 shows typical waveforms for a 600 V load fault with 8 μH load inductance. The Rogowski protection system for load fault behaves similarly for 25^oC and 150^oC cases since reaction happens at almost the same time. At time instance 0 μs, system starts conducting current. The fault signal is generated as soon as the threshold current of 600 A is reached. After a reaction time of 200 ns that consists of 100 ns delay of Driver IC processing information and 100 ns of sense pin initiating 2LTO, 2LTO initiates and the device is safely turned off in both cases without overshoot reaching rated voltage and with insufficient energy dissipated for destruction ($E^{25^oC} = 100\ mJ$ and $E^{150^oC} = 60\ mJ$).

VI. Comparison between Protection Methods

A. FUL

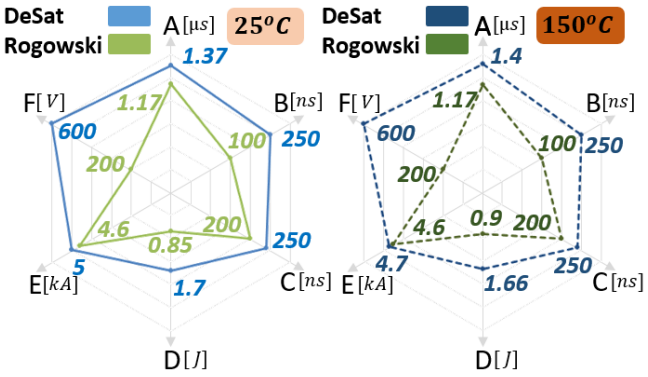

Fig.12. Comparison of protections under FUL

Fig. 12 shows comparison between DeSat and Rogowski coil protection methods in the FUL SC case in the 6 aspects that are mentioned in Section III. As it can be seen, Rogowski coil based protection is superior than DeSat protection in every aspect. Detection time of Rogowski protection (≈100 ns) is shorter for about 150 ns. Reaction time of both DeSat and Rogowski protection are determined by driver IC and are not controllable. Difference in those times comes for using different pins that have different delay associated with them. Even though both DeSat and the Rogowski coil protect the module from destruction, concern must be risen for DeSat protection overshoot since the 1.2 kV rated voltage is achieved, and possible overvoltage destruction may occur if the overshoot is higher. Also, dissipated energy in the module is double than in the Rogowski protected case which brings device closer to reaching breakdown energy point for this particular module.

B. HSF

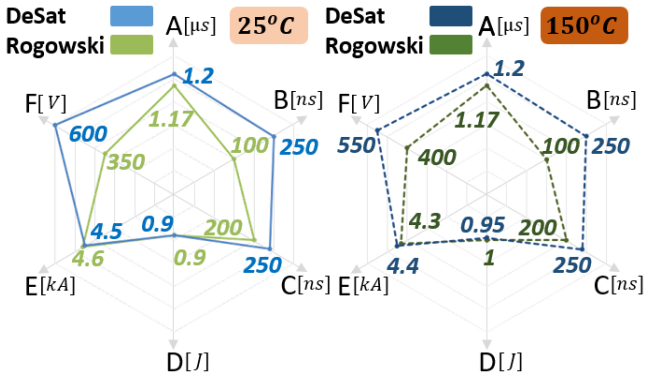

Fig. 13. Comparison of protections under HSF

Fig. 13 shows comparison between DeSat and Rogowski coil protection methods in the HSF SC case in 6 aspects. For this type of fault, protections behave similarly in some aspects such as peak current and dissipated energy. Detection and reaction time are same as in the FUL case. Even though protections have a huge difference in overvoltage aspect, due to lower current in the area of decreased gate voltage, energy remained similar. However, Rogowski protection performs slightly better, especially in the voltage overshoot aspect where

device reached rated voltage being protected by DeSat. Both protections successfully prevent module from being destroyed.

C. Load fault

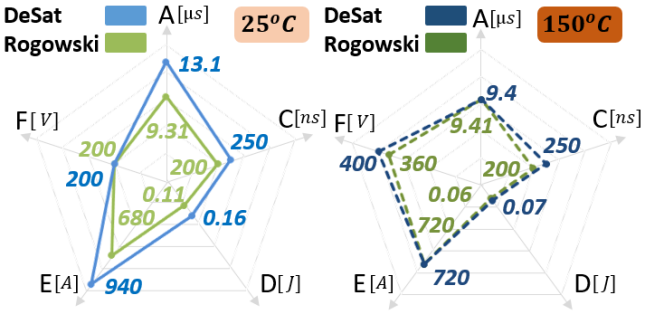

Fig.14. Comparison of protections under load fault

Fig. 14 shows comparison between DeSat and Rogowski coil based protection methods in the Load fault SC case in 5 aspects. Since load faults are slow SC events, detection time (time from beginning to the detection) is not taken into consideration because those times would be similar to the time spent in SC, which is comparison aspect A. From Fig.14 for cold case, Rogowski coil protection performs better in almost every aspect than DeSat protection, except voltage overshoot aspect which is the same. This outcome is expected since DeSat protection is tuned to perform best at 150^oC. Reaction current of the DeSat protection for 25^oC case is higher in accordance with the output characteristics of the device, which means that time spent in SC will be higher and creating higher energy that is being dissipated. As far as the 150^oC is concerned, it can be observed that both protections behave almost the same, without any significant differences.

VII. Conclusions

Both protection methods are successful in protecting the module from destruction no matter the SC type. However, it can be observed that DeSat performance can depend on SC type and temperature (load fault). DeSat protection performance in FUL and HSF case of SC is bearably satisfactory. It is slower than Rogowski coil based protection, resulting in higher peak current and higher dissipated energy especially in FUL case as well as higher overshoot. DeSat in load fault type is highly dependent on the temperature, resulting in better performance of DeSat at higher temperatures because protection is tuned in that manner. As far as the Rogowski coil based protection is concerned, it can be observed that this protection method shows consistent behavior and performance no matter the temperature of module, or the SC type. This behavior is a result of protection based on current measurement, not measuring the V_{DS} voltage which is highly dependent of temperature since the on state resistance depends on temperature.

Some authors argue that DeSat protection is slow for SiC devices. Given that the tested device survived all SC types, with good PCB design, fast driver IC-s and right tuning of parameters, DeSat can also protect SiC device. Although high-bandwidth current sensing with Rogowski coils shows faster protection and better results during SC, this method is much more complex, expensive and requires extra space for mounting embedded PCB coils. Use of Rogowski coils in the system can be justified if the high-bandwidth current sensing is necessary for other purposes such as closed loop control.

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