Single Shot Avalanche Energy Characterization of 10kV, 10A 4H-SiC MOSFETs

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***Abstract*—Higher switching frequency capability and lower switching loss associated with 10kV 4H-SiC MOSFETs make them attractive for medium voltage applications, mostly in inductive circuits e.g. solid state transformers, grid connectors and high speed machine drives. Due to exposure to inductive circuits, avalanche ruggedness of these MOSFETs needs to be established to improve their reliability in case of unintended unclamped inductive switching. In this paper, the avalanche ruggedness of 10kV, 10A 4H-SiC MOSFETs is established experimentally using single shot unclamped inductive switching. The minimum and the maximum energy is found out for the MOSFET to remain in avalanche without being failed permanently. The junction temperature at the permanent failure is estimated using semiconductor device physics.**

***Index Terms*—10kV 4H-SiC MOSFETs, avalanche ruggedness, single pulse unclamped inductive switching, medium voltage power converters.**

I. Introduction

10kV 4H-SiC power MOSFETs are good candidates to replace high voltage silicon power devices in medium voltage power converters, owing to its capability to be switched at relatively higher frequency with lower losses. These MOSFETs have huge potential to be employed in especially solid state transformers, asynchronous grid connectors, high speed electric machine for compressors, and HVDC to MVDC tap [1], [2]. Reliable application of these new devices requires them to undergo various ruggedness tests, namely single pulse short circuit, single pulse avalanche, repetitive avalanche, high temperature gate bias test and high temperature reverse bias test [3]. In this paper, single pulse avalanche ruggedness of these MOSFETs is explored for their operating limits.

Voltage overshoot across the power switches can not be eliminated completely in power electronic circuits, which is one of the most common causes of the failure [4]. Unclamped inductive switching (UIS) of power MOSFETs is used to measure its ruggedness. Most of the modern silicon based power MOSFETs are qualified for good avalanche ruggedness. Recently, a number of research works have been reported related to avalanche/UIS test of 1.2kV SiC MOSFETs, and also discussing the failure mechanism [5]- [12]. A qualifying methodology for UIS test of SiC MOSFETs is documented in [13]. However, little has been reported on the avalanche ruggedness of 10kV 4H-SiC MOSFETs. Reliability of modern 10kV 4H-SiC MOSFETs are still to be established in terms of its avalanche withstanding capability.

The maximum avalanche energy, which results in the MOSFET failure, gives an indication of safety margin to the circut designer while assessing the reliability of these MOSFETs in the converter. In this paper, single pulse UIS test is performed on the 10kV, 10A 4H-SiC MOSFETs, whose static characteristics are reported in [16]. Due to poor availability of these MOSFETs, only one MOSFET is subjected to the test. All the tests are performed at room temperature, as the available MOSFET package does not have an isolated base plate, making it difficult to heat the base plate. Junction temperature of the MOSFET at the avalanche failure is estimated using an analytical expression.

II. Unclamped Inductive Switching

In single shot unclamped inductive switching, the energy stored in the inductor during turn-on is dumped to the power switch during its turn-off. One of the possible test circuits, as mentioned in [14], is shown in Fig. 1(a). The theoretical test waveform with relevant notations are shown in Fig. 1(b) during the avalanche condition without permanent failure of the MOSFET. The device under test (DUT) is Q1. The inductor L is charged to a desired current level I_{AV} to store the energy E_{AV}. Thereafter, Q1 is turned-off, forcing the stored energy to dump into the DUT. Above the minimum value of E_{AV}, the turn-off voltage across the DUT will touch the avalanche value. If the energy is more than the critical value, the DUT will eventually fail. The device physics

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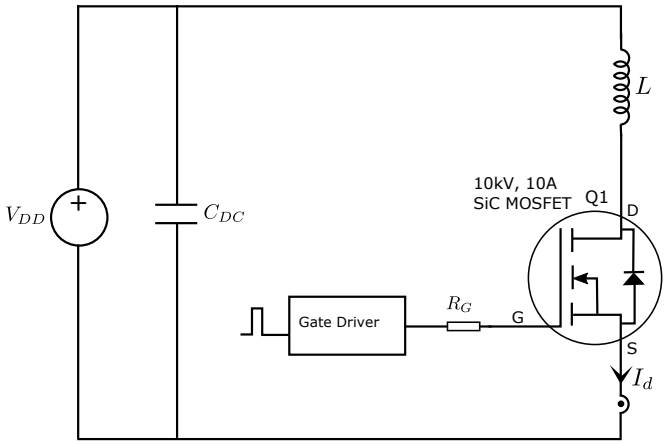

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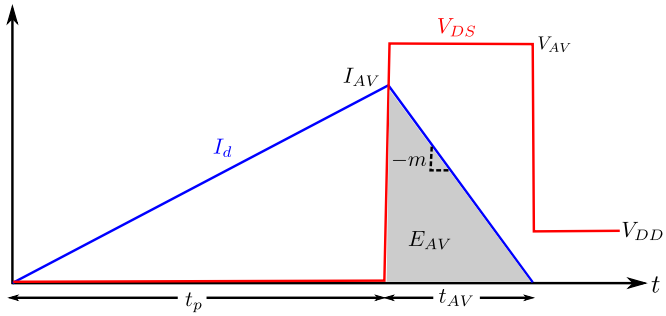


(b)

Fig. 1: Single pulse unclamped inductive switching (a) schematic of the setup, and (b) theoretical waveform during the avalanche condition without permanent failure.

associated with the failure mechanism in similar 4H-SiC power MOSFETs is discussed in [9].

The dc bus voltage is typically, but not necessarily kept below one tenth of the voltage rating of the device under test. The dc bus capacitor C_{DC} must be sufficiently charged to deliver the avalanche energy during the test.

$$\frac{1}{2}C_{DC}V_{DD}^2 \geq \frac{1}{2}LI_{AV}^2$$

III. Estimation of the Junction Temperature

Failure during the avalanche condition in the MOSFET can be attributed to the turn-on of the parasitic BJT or the internal temperature reaching the intrinsic temperature limit. Basic structure of the 4H-SiC MOSFET is shown in Fig. 2. The N+ source and the P-base of the parasitic NPN BJT are shorted electrically by the source contact, which suppresses turn-on of the BJT. In absence of the BJT turn-on, the material breakdown due to internal heating by the avalanche energy may be accountable for the 4H-SiC MOSFET failure.

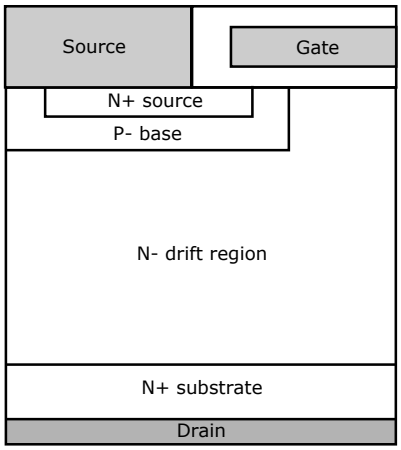


Fig. 2: Basic structure of the 4H-SiC planar MOSFET [15].

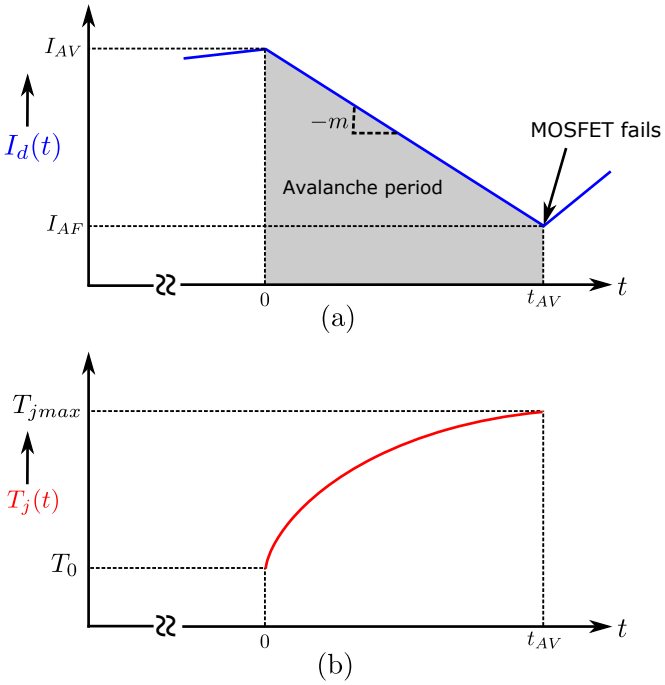


Fig. 3: Avalanche failure of the MOSFET: (a) the current waveform, and (b) the estimated junction temperature. The junction temperature reaches the maximum value T_{jmax} at time t_{AV}, where the MOSFET fails.

A typical current waveform during the avalanche failure is shown in Fig. 3(a). At the beginning of the avalanche period ($t = 0$), the energy stored in the inductor E_{AV} is forced to flow into the MOSFET. The avalanche energy E_{AV} is given as

$$E_{AV} = \frac{1}{2}LI_{AV}^2 \tag{1}$$

Assuming adiabatic process, rise in the junction temperature of the MOSFET is derived as follows:

The drain current I_d flowing through the DUT during the avalanche period, as depicted in Fig. 3(a), is expressed as

$$I_d = -mt + I_{AV} \tag{2}$$

Power density per unit volume during the avalanche is given as

$$P_c = E_c \times J_c = E_c \frac{(-mt + I_{AV})}{A_c}, \tag{3}$$

where E_c is the electric field during the avalanche condition, and A_c is the active area of the MOSFET.

The infinitesimal value of energy flow per unit volume during the avalanche is given as

$$\mathrm{d}E_{av} = P_c \mathrm{d}t \tag{4}$$

This energy is assumed to be totally dissipated inside the MOSFET as heat, which results in

$$dE_{av} = C_V \mathrm{d}T_j, \tag{5}$$

where C_V is the volumetric heat capacity (J/°C/cm^{-3}) of the 4H-SiC material. $\mathrm{d}T_j$ is the change in the junction temperature due to flow of $\mathrm{d}E_{av}$.

Equating (4) and (5), we get

$$C_V \mathrm{d}T_j = E_c \left(\frac{-mt + I_{AV}}{A_c} \right) \mathrm{d}t \tag{6}$$

Integrating the above equation, the junction temperature $T_j(t)$ at time t during the avalanche period is derived as

$$T_j(t) = T_0 + \left(-\frac{mt^2}{2} + I_{AV} t \right) \frac{E_c}{A_c C_V}, \tag{7}$$

where T_0 is the junction temperature at $t = 0$. A_c is the device design parameter. E_c and C_V are assumed to stay constant during the temperature rise, though these parameters vary with temperature. m, t_{AV} and I_{AV} are found from the experimental waveform. T_0 can be assumed to be equal to the ambient temperature.

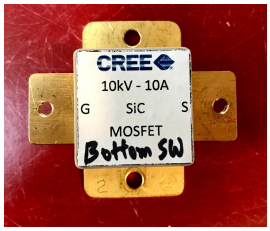
The junction temperature is a parabolic function of time. Its maximum value is derived by setting $\mathrm{d}T_j/\mathrm{d}t$ to zero in (6) at $t = t_{AV}$. Assuming I_{AF} to be negligibly small, we get

$$t_{AV} = \frac{I_{AV}}{m} \tag{8}$$

and, the maximum T_j as:

$$T_{jmax} = T_0 + \frac{I_{AV} t_{AV}}{2} \frac{E_c}{A_c C_V} \tag{9}$$

Eq. (9) gives an estimate of the maximum junction temperature at time t_{AV} of the avalanche failure. A typical variation in T_j with time during the avalanche period is plotted in Fig. 3(b).



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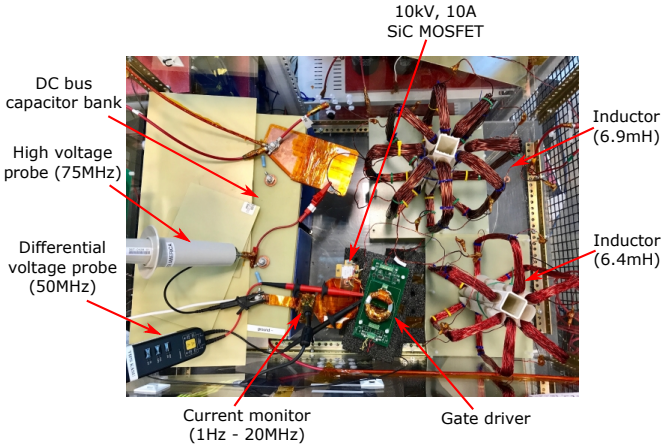


(b)

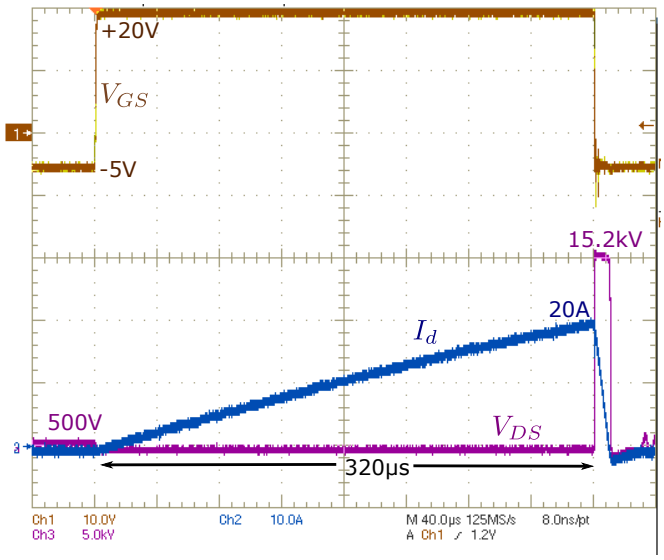
Fig. 4: Photograph of (a) 10kV, 10A 4H-SiC MOSFET die in a package without isolated base plate, and (b) the UIS test hardware setup.

IV. Experimental Results

Fig. 4(a) shows the photograph of the 10kV SiC MOSFET. Its package does not have isolated base plate, and the base plate is connected to the drain terminal. The active area is 32mm^2 with the drift region doping of 6×10^{14}cm^{-3} and thickness of 120μm [16].

The single shot avalanche ruggedness test is performed at room temperature. As the experiment involves high voltage, fatal to human beings, appropriate safety measures must be considered before and during the experiment. Photograph of the experimental hardware setup is shown in Fig. 4(b). High bandwidth voltage and current probes are employed for the measurement. Air-core toroidal inductors are used to avoid current saturation. The high voltage DC bus capacitors may explode, if the voltage across them surpasses the rating. The experimental set-up is energized inside a safety cage. The control circuits are in remote location, and accessed via wireless connection/optical fibers.

Before the MOSFET fails permanently due to avalanche breakdown, a number of experiments are performed to test the avalanche withstanding capability of



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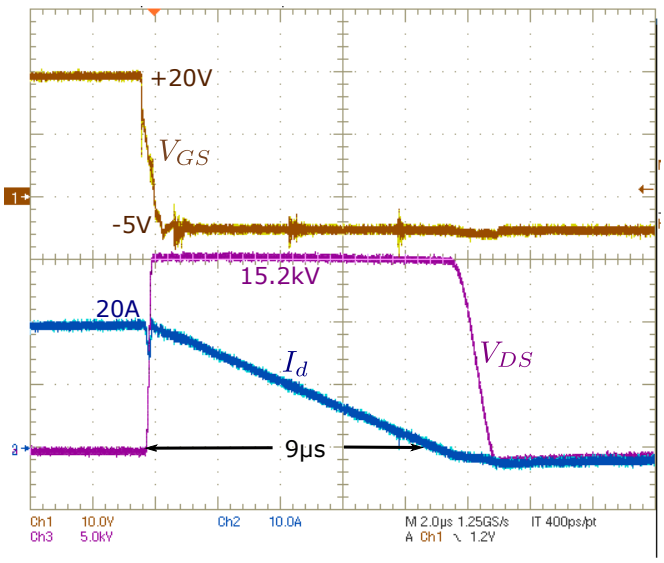
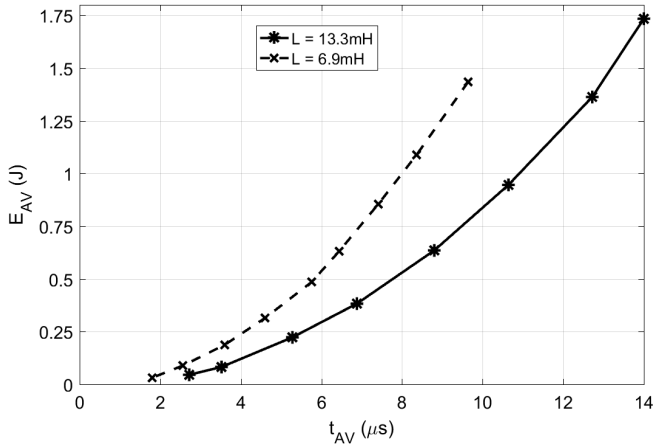


(b)

Fig. 5: Experimental results during single pulse unclamped inductive switching at room temperature (without permanent failure): (a) full waveform, (b) zoomed-in waveform during avalanche condition.
I_{AV}=20A, t_{AV}=9μs, E_{AV}=1.37J. V_{DD} = 500V, L = 6.9mH, R_G = 20Ω, t_p = 320μs.
V_{GS}: 10V/div; V_{DS}: 5kV/div; I_d: 10A/div; time: (a) 40μs/div, (b) 2μs/div.



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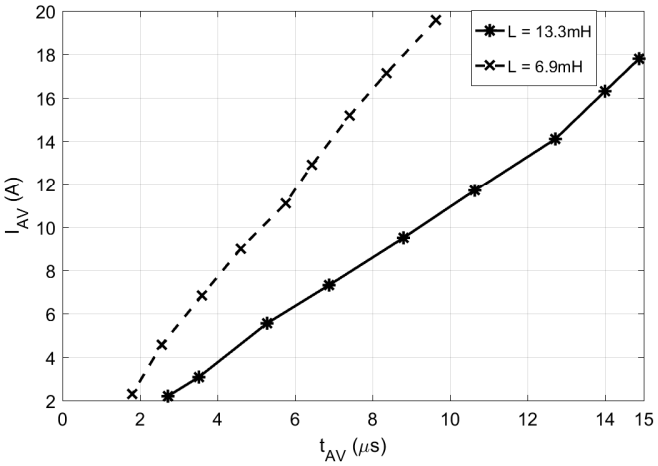


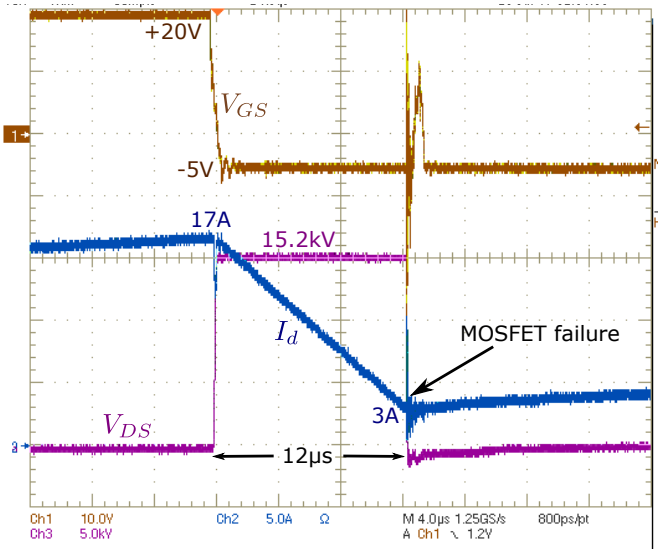
(b)

Fig. 6: Experimental results showing avalanche withstanding capability during single pulse unclamped inductive switching at room temperature (without permanent failure): (a) Avalanche energy E_{AV} vs. t_{AV}, and (b) avalanche current I_{AV} vs. t_{AV} at two different values of inductor L.
V_{DD} = 500V, V_{AV} = 15.2kV.

the MOSFET in single shot UIS event. The current is increased gradually by increasing the gate pulse width t_p. Minimum energy of 32mJ is observed to be required to force the MOSFET into avalanche with the avalanche voltage of 15.2kV. Fig. 5 shows the experimental waveform at avalanche energy of 1.37J without failure. In this case, the calculated avalanche energy using (1) comes out to be 1.38J, which is close to the experimentally observed value ($\frac{1}{2}V_{AV}I_{AV}t_{AV}$ = 1.37J).

Avalanche withstand capability of the MOSFET is depicted in Fig. 6, showing the variation in t_{AV} with E_{AV} and I_{AV} at two different inductance L in the UIS event without failure. This curve can be used to design an application circuit considering prevention of MOSFET failure in case of unintended avalanche condition.

At room temperature, the critical avalanche energy to failure is observed to be 1.82J. The experimental waveform during the MOSFET failure is shown in Fig. 7(a).



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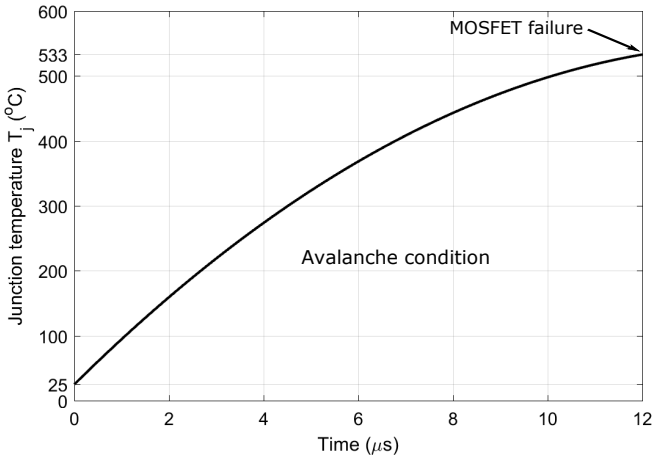

(b)

Fig. 7: Avalanche failure of the 10kV 4H-SiC MOSFET: (a) experimental result at room temperature, and (b) estimated junction temperature during the avalanche condition. The current starts increasing after 12μs of Avalanche duration, showing the failure. The junction temperature reaches 533°C at the failure.
$E_{AV,cric}$ = 1.82J at I_{AV} = 17A and 25°C. V_{DD} = 1000V, L = 13.3mH, R_G = 20Ω, t_p = 240μs.
V_{GS}: 10V/div; V_{DS}: 5kV/div; I_d: 5A/div; time: 4μs/div.

Rise in the current during the avalanche condition is evidence of the MOSFET failure.

Rise in the junction temperature T_j is calculated using (7) and Fig. 7(a). Volumetric heat capacity C_V of the 4H-SiC material is 2.21 J/°C/cm^{-3} [13]. The critical electric field E_c during the avalanche period is assumed to be 3×10^6V/cm [13]. Rise in T_j is plotted in Fig. 7(b) for the waveform shown in Fig. 7(a). T_j is estimated to rise upto 533°C at the failure, which is close to the estimated junction temperature (511°C) of 1.2kV SiC MOSFETs at the avalanche failure reported in [6].

V. Conclusion

Single shot avalanche ruggedness of 10kV, 10A SiC MOSFETs is characterized using unclamped inductive switching test. A minimum energy of 32mJ is required to force the MOSFET into avalanche condition, and a maximum avalanche energy of 1.82J results in permanent failure of the MOSFET at room temperature. This energy is higher compared to that reported for 900V and 1200 SiC MOSFETs. The avalanche withstanding capability is demonstrated for different inductance in terms of I_{AV}-t_{AV} curves. An analytical expression is proposed to estimate the junction temperature of the MOSFET during the avalanche failure. The junction temperature rises upto 533°C at the failure. The above data will be useful in designing application circuit of these 10kV SiC MOSFETs ensuring higher reliability of the devices in medium voltage converters. For future works, similar experiments can be performed at elevated initial junction temperature, and in repetitive UIS mode. In practical conditions, the junction temperature is usually above the room temperature. The UIS test at higher initial junction temperature T_0 will provide more realistic figure of the ruggedness. Connection of the base plate of these MOSFET package makes it difficult to heat the die to elevated temperature, as the heating plate in contact with the drain will be floating electrically to high voltage. An alternate contact-less heating method can be employed to raise the junction temperature.

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REFERENCES

[1] J. W. Palmour, "Silicon carbide power device development for industrial markets," 2014 *IEEE International Electron Devices Meeting*, San Francisco, CA, 2014, pp. 1.1.1-1.1.8

[2] B. J. Baliga, "Advanced High Voltage Power Device Concepts, 1st ed., Springer, 2011.

[3] A. Castellazzi, A. Fayyaz, G. Romano, L. Yang, M. Riccio, A. Irace, "SiC power MOSFETs performance, robustness and technology maturity", *In Microelectronics Reliability*, Volume 58, Pages 164-176, 2016.

[4] R. R. Stoltenburg, "Boundary of power-MOSFET, unclamped inductive-switching (UIS), avalanche-current capability," *Proceedings, Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Baltimore, MD, 1989, pp. 359-364.

[5] X. Zhou; H. Su; R. Yue; G. Dai; J. Li; Y. Wang; Z. Yu, "A Deep Insight into the Degradation of 1.2kV 4H-SiC MOSFETs under Repetitive Unclamped Inductive Switching Stresses," in *IEEE Transactions on Power Electronics* , vol.PP, no.99, pp.1-1

[6] M. D. Kelley, B. N. Pushpakaran and S. B. Bayne, "Single-Pulse Avalanche Mode Robustness of Commercial 1200 V/80 m SiC MOSFETs," in *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6405-6415, Aug. 2017.

[7] I. Dchar, M. Zolkos, C. Buttay and H. Morel, "Robustness of SiC MOSFET under avalanche conditions," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 2263-2268.

[8] S. Liu et al., "Investigations on degradation and optimization of 1.2kV 4H-SiC MOSFET under repetitive unclamped inductive switching stress," *2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, Hong Kong, 2015, pp. 205-208.

[9] Fayyaz, Asad, et al. "A Comprehensive Study on the Avalanche Breakdown Robustness of Silicon Carbide Power MOSFETs." Energies 10.4 (2017): 452.

[10] Claudiu Ionita, Muhammad Nawaz, Kalle Ilves, "On the short-circuit and avalanche ruggedness reliability assessment of SiC MOSFET modules", *Microelectronics Reliability*, Volume 71, 2017, Pages 6-16, ISSN 0026-2714

[11] Y. Nanen, M. Aketa, H. Asahara and T. Nakamura, "Estimation of junction temperature at failure of SiC DMOSFETs in UIS test," *2016 IEEE International Meeting for Future of Electron Devices*, Kansai (IMFEDK), Kyoto, 2016, pp. 1-2.

[12] A. Fayyaz et al., "UIS failure mechanism of SiC power MOSFETs," *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Fayetteville, AR, 2016, pp. 118-122.

[13] V. Pala, B. Hull, J. Richmond, P. Butler, S. Allen and J. Palmour, "Methodology to qualify silicon carbide MOSFETs for single shot avalanche events," *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Blacksburg, VA, 2015, pp. 56-59.

[14] K. Fischer and K. Shenai, "Dynamics of power MOSFET switching under unclamped inductive loading conditions," in *IEEE Transactions on Electron Devices*, vol. 43, no. 6, pp. 1007-1015, Jun 1996.

[15] B J Baliga., "Gallium Nitride and Silicon Carbide Power Devices," World Scientific, 2017.

[16] J. W. Palmour et al., "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV," *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, Waikoloa, HI, 2014, pp. 79-82.