Power semiconductor ageing test bench dedicated to photovoltaic applications

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***Abstract*—This paper presents a new concept of semiconductor ageing test benches dedicated to photovoltaic inverters, where the accelerated ageing test reproduces a typical profile of the photovoltaic inverters RMS output current. The current profile is obtained by analyzing mission profiles of the current and the ambient temperature, extracted over several years from different photovoltaic plants. Accordingly, the ageing test is done by applying simultaneously thermal cycling and power cycling, using power semiconductors in a Pulse Width Modulation inverter and under nominal conditions. The design of the current ageing profile using power losses and thermal models is depicted. Consequently, the double pulse method, as well as thermal impedances measurement tests are presented. Finally, the preliminary experimental results of the accelerated ageing tests are presented in the case of Silicon Carbide MOSFET semiconductors. These results show a remarkable increase in the gate to source threshold voltage, the drain leakage current, the drain to source on resistance, the drain to source on voltage and the body diode forward voltage.**

Keywords—Power Cycling; Photovoltaic inverter; Silicon Carbide MOSFET; Semiconductor Failure Indicators; Double Pulse Test; Thermal Impedance Measurement

I. INTRODUCTION

Silicon Carbide (SiC) semiconductor devices are being increasingly used in power electronic applications, mainly because of their high switching speed, which improves the overall efficiency and/or the compactness of the inverters. On the other hand, in photovoltaic systems the DC/AC inverter has the highest failure rate, and the anticipation of its breakdowns is still difficult [1]. Thus, it is crucial to accelerate the ageing of the inverter devices, in order to study their main failure modes. In this context, accelerated ageing of power modules is carried out under aggravated conditions of current (power cycling) or temperature (thermal cycling) to speed up the natural ageing process. It is used to help determining in a laboratory, the long-term effects of expected levels of stress within a shorter period of time. Unfortunately, by applying the accelerated ageing, mechanisms of failures that do not occur in the real application could be observed, while inversely other mechanisms that usually occur could be not recreated [2].

Thermal cycling consists on cycling the devices between two extreme temperatures, and hence inducing big variations in the module temperature. Power cycling consists in applying a series of current pulses, usually resulting in large variations of the junction temperature of semiconductor devices [3] [4]. Power cycling using the opposition method consists in cycling the power semiconductors in a single-phase PWM inverter, under nominal conditions. It is a power cycling method with more realistic electrical stresses on the power devices, compared with the classical power cycling. The devices are fed with a regulated switched sinusoidal current with an adjustable frequency. For power semiconductor devices, the operating conditions are very close to those existing in a real inverter [5] [6]. The accelerated ageing methods mentioned above are widely used, but do not necessarily represent always the real application [7].

This paper presents a new concept of ageing test benches dedicated to photovoltaic inverters, by considering the mission profiles of the current and ambient temperature, extracted from photovoltaic plants for several years, as presented in Fig. 1. The photovoltaic data analysis leads to create typical profiles of photovoltaic inverters RMS output current and ambient temperature. These profiles are then introduced into a power losses estimation model, coupled with a thermal model to estimate the correspondent junction temperature of the semiconductor devices, considering the electro-thermal coupling of temperature-dependent electrical parameters [3]. Then, the estimated junction temperature profile of the semiconductors, corresponding to the accelerated ageing current profile, are used to determine the ageing profile parameters, after applying the required refinements. Finally, the obtained ageing profile is applied during the new accelerated ageing test, where active and passive cycling are simultaneously done, under switching nominal conditions and pulse width modulation (PWM) operating mode. The accelerated ageing is stopped periodically, in order to apply the diagnostics of the semiconductor devices, using the *Keysight B1506A* Analyzer. The purpose is to identify the potential indicators of ageing/failure of SiC MOSFET devices used in photovoltaic DC/AC inverters. This method that aims to regenerate close constraints of the photovoltaic application will be depicted in the following sections, as well as some preliminary results of the accelerated ageing test.

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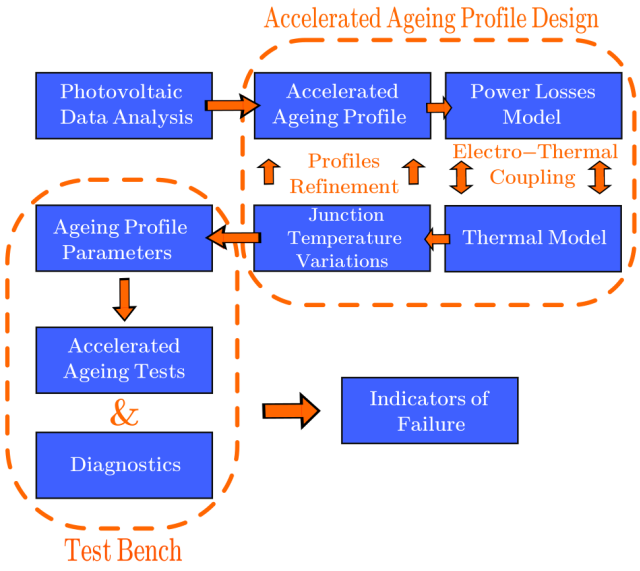


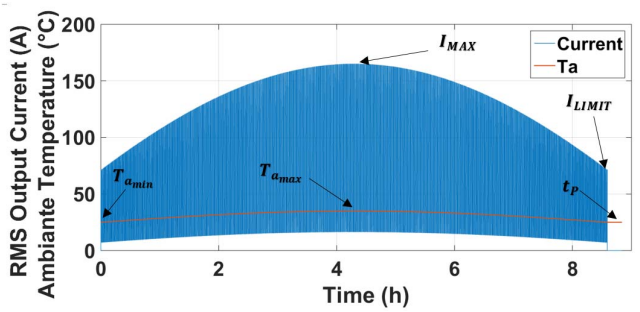
Fig. 1. Synoptic of the full study

II. BUILDING TYPICAL PHOTOVOLTAIC PROFILES

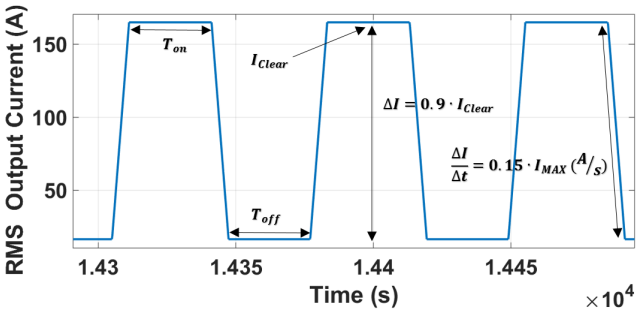
An analysis of current and ambient temperature mission profiles extracted from photovoltaic plants for several years is presented in [8]. The analysis covers the shape of the current, the slope of the current variations, the diffuse radiation, the delays between the current variations, the differences between the seasons and the ambient temperature. The statistical analysis of the photovoltaic mission profiles lead to the typical photovoltaic profile presented in Fig. 2.a. This profile simulates one day of real application (without considering the night). Like in real application, the profile of the RMS output current has a sinusoidal shape, where the minimum current value at a given time is nearly 10% of the current's value, before the occurring variation (Fig. 2b). Hence, the current variation at a given time can be expressed as $\Delta I = 0.9 \cdot I_{Clear}$, where I_{Clear} represents the RMS current's value before the current drop (corresponding to a clear sky). In Fig. 2.b, the slope $\Delta I/\Delta t = 0.15 \cdot I_{MAX}$ (A/s), while T_{on} and T_{off} represent the delays between the variations.

On the other hand, it can be noticed that a truncation is applied at the two extreme sides of the profile, so that the value of the current starts at I_{LIMIT} instead of 0, to prevent the creation of $\Delta T_J < 30$ K (by introducing $\Delta I \geq \Delta I_{min}$). I_{MAX} represents the peak value of the RMS current. As it can be seen in Fig. 2.a, the ambient temperature T_a has a sinusoidal shape, varying between Ta_{min} and Ta_{max}.

The current profile is sequentially applied during the power cycling using the opposition method, by switching the semiconductors of the inverter using the PWM, while a thermal cycling is applied simultaneously by varying the ambient temperature. A pause of $t_p = 15$ minutes is made between two consecutive profiles, to allow for the relaxation of the viscoelastic constraints in the power module [9] [10].



a. Ageing profile simulating one day of real application



b. Zoom on several current variations

Fig. 2. Accelerated ageing profiles of the current and the ambient temperature

III. EXPERIMENTAL SETUP

As presented in Fig. 1, once the accelerated ageing profile is defined, it is then introduced into power losses and thermal models. Then the desired junction temperature cycles can be obtained by determining the profile's parameters presented in Fig. 2, after applying the required refinements on the profile.

In order to conduct this study, a two-level DC/AC single-phase inverter was designed, implementing SiC MOSFET power modules *APTMC120AM16D3AG* (1200V-136A phase-leg power modules without antiparallel diodes). The inverter is cooled down with a cold plate as presented in Fig. 3. It uses 4x420 µF DC-link capacitors (C_{bus}) and 2x1 µF decoupling capacitors (C_{dec}), with a DC bus voltage E = 750V. The equivalent electrical circuit of the inverter is presented in Fig. 4.

The opposition method was implemented using *LabVIEW*; one FPGA core of a *PXI* system (*National Instruments*) drives the MOSFETs as well as the DC-link power source, and controls the coolant fluid temperature. Two pre-driver electronic boards were designed to adapt the output signals of the *PXI*, since the used drivers *PT62SCMD12* (*Cree*) accept only differential input signals. Moreover, two *LEM* current transformers *HAS 100-S* were used for the closed loop control of the load current, where the load used is a 130 µH inductance. Fig. 5 shows the inverter prototype, whereas Fig. 6 represents the global accelerated ageing test bench.

Fig. 3. Two-level single-phase DC/AC inverter

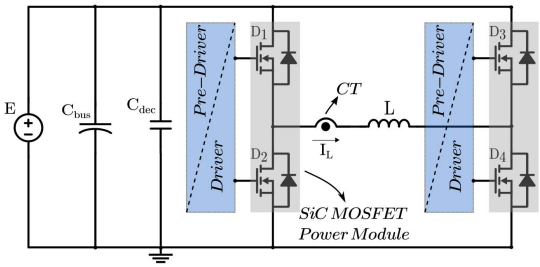


Fig. 4. Equivalent electrical ciruit of the inverter

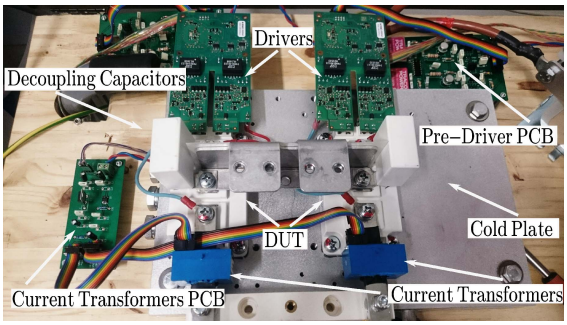


Fig. 5. Inside of the inverter

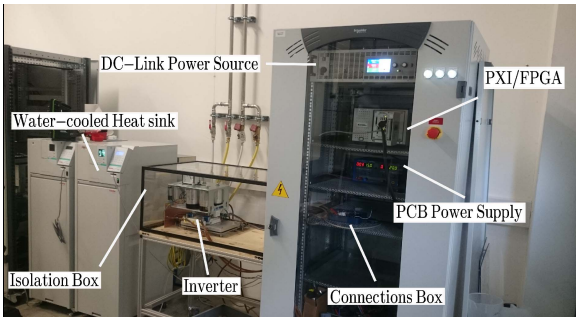


Fig. 6. Global test bench

IV. DETERTMNATION OF POWER LOSSES

A. Power losses model

A power losses model was built with *Matlab* in order to estimate both the conduction and the switching losses of the semiconductor devices [11] [12]. Having current profiles with high number of samples, only the average losses within a fundamental period T_{out} = 20ms were calculated [13]. The power losses model is presented in details in [11], in the case of a two-level PWM DC/AC inverter.

In order to estimate the conduction losses of the MOSFET, the Drain-Source on-state resistance $R_{DS_{on}}$ is extracted from datasheet, given as a function of the current level and the MOSFET junction temperature. Similarly, the conduction power losses of the MOSFET's intrinsic body diode can be obtained by extracting the value of their threshold voltage E_0 and its dynamic resistance R_D from datasheet. However, the values of these parameters were verified with the *B1506A* Analyzer (*Keysight*).

The MOSFET switching power losses can be estimated by multiplying the switching energy losses E_{on} and E_{off} by the switching frequency f_{sw}, and similarly for the diodes using reverse recovery losses E_{rec}. Usually, these energy losses are given in the datasheet, however E_{rec} is not provided for this power module.

On the other hand, the MOSFET's intrinsic body diode was found in the literature to dissipate non-negligible switching losses in the transistor. Despite this, the reverse recovery energy of the MOSFET's body diode was found to be comparable to the Schottky's recovery energy in several recent studies [14] [15] [16]. Hence in order to verify this theory and obtain more accurate values of E_{on} and E_{off}, the double pulse test was applied. In fact, the switching processes are affected by the parasitic connection inductances. They induce transient overvoltages and may cause oscillations due to the circuit and transistor capacitances [4], thus it is more accurate to directly measure the switching losses in the inverter that will be used during the accelerated ageing test.

Finally, since $R_{DS_{on}}$, E_0, R_D, E_{on}, E_{off} and E_{rec} are all temperature-dependent parameters, their values were updated with the calculated T_J, at each iteration of the *Matlab* model's code.

B. Double Pulse Test (DPT)

1) Methodology and test bench

The electrical circuit of the double pulse test setup is presented in Fig. 7, where the MOSFET power module (phase-leg) is tested inside the inverter that will be used later on during the ageing test. In this figure, E is the DC bus voltage source, C_{bus} the DC-link capacitors, C_{dec} the decoupling capacitors and TSCT a Two Stages Current Transformer. In short, the double pulse test consists in applying two consecutive pulses on the gate driver's voltage V_{dr} of the low side MOSFET K_L, while the high side MOSFET K_H is maintained blocked, using a 9V battery in reverse between the gate and the source (V_{GS} = -9 V). [17] [18]. The voltage source E = 750 V, L_{load} = 380µH and the external gate resistances Rg = 10 Ω.

Despite its several advantages, the DPT applied to SiC MOSFETs presents some complexities, such as the need for wide bandwidth current and voltage probes, the insertion of a current sensor in the switching cell (so increasing the stray inductance), and the phase shift between the probes [19].

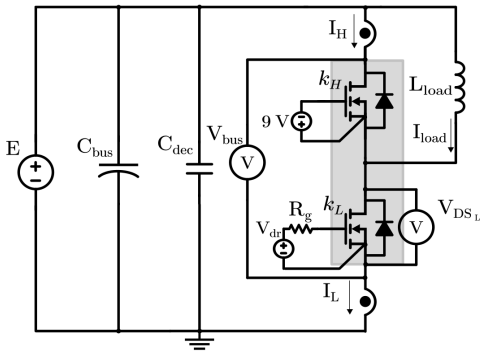


Fig. 7. Double pulse test circuit

Thus, *LECROY* passive voltage probes of 2kV, 1:100 with a wide bandwidth BW = 400 MHz were used to measure the voltages V_{bus} and V_{DSL} (Fig. 7). The passive probe used during the DPT was adjusted as presented in Fig. 8, in order to reduce the stray inductance in the measurement circuit.

The current was measured by adding a second CT (Current Transformer) stage to a Pearson current monitor model 2877, using the method presented in [20]. Finally, the phase shift between probes, also known as skew, which results from the difference between the probes frequency behaviors and from the reflection phenomena, was eliminated using the method proposed in [21]. It is done by measuring the current and the voltage across a non-inductive resistor with the different used probes. The double pulse test bench is presented in Fig. 9, where the DUT (Device Under Test) is fixed to a cold plate, controlled with a water-cooled heat sink. Moreover, a *dSpace* controller is used to apply adjustable pulses, while an oscilloscope measures and saves the probes' signals.

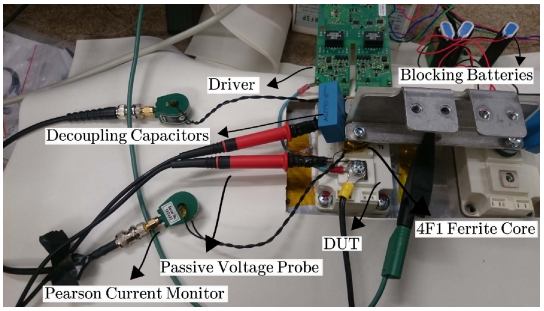


Fig. 8. Inside of the inverter

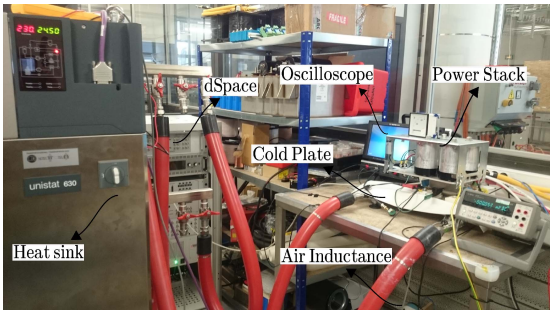


Fig. 9. Double pulse test bench

2) Results

In order to obtain the switching energy losses as a function of the current and the junction temperature, the tests were applied for the following load current values I_{Load} =10A, 30A, 45A, 60A, 90A and 120A, and for two junction temperatures T_J = 25 °C and 100 °C. At thermal equilibrium, the junction temperature can be estimated by measuring the cold plate's temperature, directly under the dies using a thermocouple. Fig. 10 represents the turn-on energy losses as a function of the low side current (E_{on}= f (I_L)) for T_J = 25°C and 100°C, while Fig. 11 represents the same for the turn-off energy losses (E_{off} = f (I_L)). Fig. 12 represents the diode's recovery energy losses as a function of the high side current (E_{rec} = f (I_H)). It can be seen that E_{rec} is largely lower than the other switching energies and seems to confirm the results proposed in [14] [15] [16].

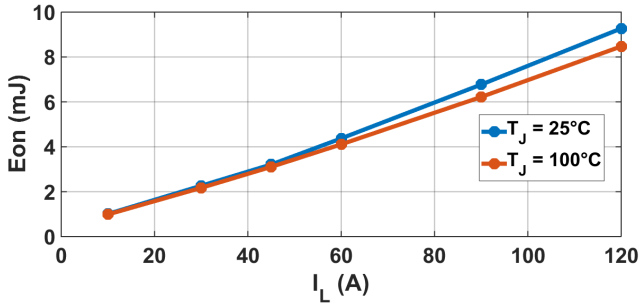


Fig. 10. Turn-on energy losses as a function of the current I_L (E_{on}=f(I_L)) for T_J = 25°C and 100°C

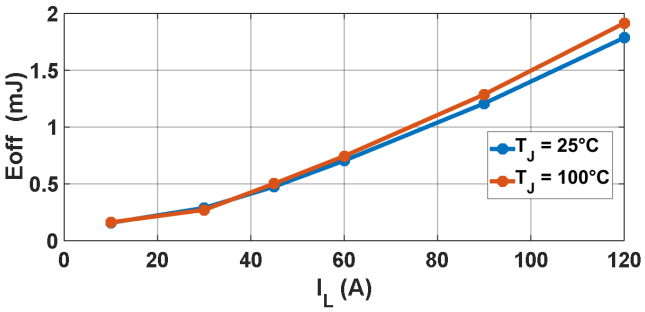


Fig. 11. Turn-off energy losses as a function of the current I_L (E_{off} = f(I_L)) for T_J = 25°C and 100°C

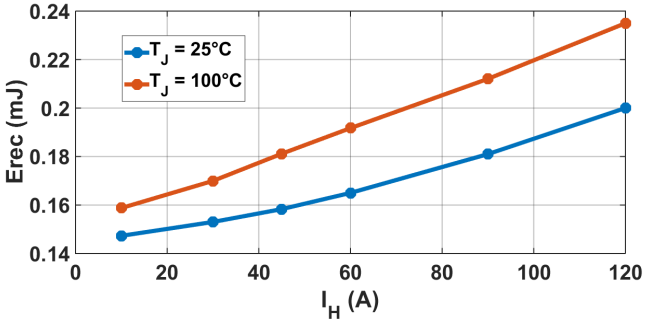


Fig. 12. Recovery energy losses as a function of the current I_H (E_{rec} = f(I_H)) for T_J = 25°C and 100°C

V. IDENTIFICATION OF THE THERMAL MODEL

A. Basics of the thermal model

1) Choice of the equivalent thermal circuit

The thermal model uses Foster networks since the fitting of the measured thermal impedance curves is easier with this equivalent circuit type, rather than with Cauer networks. However, a Foster network represents only a mathematical description of a given system, and should not be considered as a real physical model. Its equivalent thermal impedance can be expressed as follows:

$$Z_{th}(t) = \sum_{i=1}^{i=N} R_{th_i} \cdot (1 - e^{-\frac{t}{\tau_i}}) \quad (1)$$

where Rth_i is one elementary thermal resistance of the model, τ_i one elementary time constant at the point i ($\tau_i = Rth_i \cdot Cth_i$), while N is the number of R-C cells in the model. In order to consider the thermal coupling between the semiconductor devices, the junction temperature of the different devices can be estimated, using the following matrix:

$$\begin{pmatrix} T_{J_1} \\ T_{J_2} \\ T_{J_3} \\ T_{J_4} \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{21} & Z_{31} & Z_{41} \\ Z_{12} & Z_{22} & Z_{32} & Z_{42} \\ Z_{13} & Z_{23} & Z_{33} & Z_{43} \\ Z_{14} & Z_{24} & Z_{34} & Z_{44} \end{pmatrix} \cdot \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{pmatrix} + T_A \cdot \begin{pmatrix} 1 \\ 1 \\ 1 \\ 1 \end{pmatrix} \quad (2)$$

However, a series combination between Foster networks of the power module and the water-cooled heat sink, using the values of R-C cells provided in the datasheets, will lead to non-negligible errors in T_J estimation [27]. Thus, a thermal model of high precision can be only achieved by a direct measurement of the Junction-Ambient self-heating thermal impedances, as well as a measurement of all the mutual thermal coupling impedances existing between the semiconductor devices.

2) Choice of the calculation method

Having accelerated ageing profiles with more than 1.5 million samples each and a complex thermal model of 16 thermal impedances, the junction temperature estimation of each device becomes very time-consuming. Hence, in order to reduce the calculation time, six T_J calculation methods using equivalent combined circuits of Foster networks were implemented and compared in terms of execution time and the ability to consider the electro-thermal coupling. These methods are: Time-Domain Estimation [23], Fast Fourier Transform FFT [22], FFT with Overlap-Add method [24], Breaking down mission profile into single pulses [25], and finally an analytical solution [26]. These methods provided the same output results, which allowed to validate them. As a conclusion, the analytical solution presents the highest performance in term of execution time, mostly with very long mission profiles and complicated systems with multiple power modules, where the thermal coupling effect between the modules is considered. In fact, it took less than 1s to process a profile of 750 ksamples when processing the analytical method, while the calculation machine blocked when processing the Time-Domain method.

B. Thermal impedances measurement

1) Methodology and test bench

The thermal impedances measurement was done using a Thermo-Sensitive Electrical Parameter (TSEP) [3] [25]. The chosen TSEP was the forward voltage under low current of the MOSFET's intrinsic body diode [28].

a) Calibration

Usually, in order to determine the relationship between the TSEP and the semiconductor's junction temperature, a calibration of the TSEP is needed. During the calibration phase, the system's temperature is fixed with the water-cooled heat sink. At thermal equilibrium, it is assumed that the semiconductors' junction temperature is equal to the cold plate temperature, measured with T-type thermocouples. To do so, the cold plate was drilled under the center of the semiconductors' chips positions as represented in Fig. 13, and the thermocouples were inserted in the drilled holes. Fig. 14 represents the resulting graph of the forward voltage V_f of the MOSFET's body diode as a function of the junction temperature. The equations forms of $V_f = f(T_J)$ of the different semiconductor devices were fitted with a polynomial equation of the 3rd degree, in order to achieve high precision.

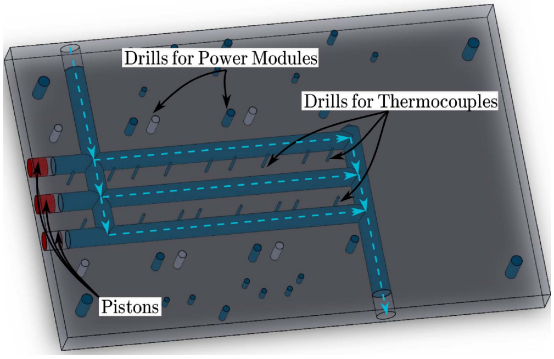


Fig. 13. 3D plan of the cold plate

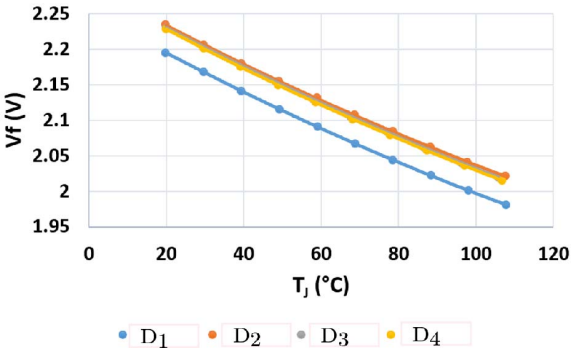


Fig. 14. MOSFET body diode's forward voltage V_f, as a function of the junction temperature

b) Z_{th} measurement

The second step consists on injecting a high current in the DUT which induces high heat losses, and thus rises the semiconductors' junction temperature. The temperature estimation is done during the cooling phase, by injecting a low current of 100mA in the devices. Hence, the Junction-Ambient

self-heating thermal impedance of device D_i can be obtained as follows:

$$Z_{th_{ii}}(t) = \frac{T_{J_{h_i}} - T_{J_{m_i}}(t)}{P_{h_i}} \quad (3)$$

where Ph_i and TJh_i represent respectively the power losses and the junction temperature of device D_i at stationary state, and TJm_i *(t)* the instantaneous junction temperature of the same device during the cooling phase. Next, a high current is injected in the device D_j which induces a rise of D_i's junction temperature. The mutual thermal coupling impedance between device D_j and device D_i can be calculated in the same way as of the self-heating thermal impedance, as follows:

$$Z_{th_{ji}}(t) = \frac{T_{J_{h_i}} - T_{J_{m_i}}(t)}{P_{h_j}} \quad (4)$$

However, since the transition between the high current and the low current is not instantaneous, the switching process introduces some transients to the TSEP measurement. Thus, TJ_h was determined by applying a linear extrapolation on the TSEP curve during the cooling phase, assuming that the temperature decreases linearly with the square root of time [28]. Fig. 15 represents the DUTs, mounted on the cold plate and connected to the current sources. Fig. 16 represents the full measurement test bench, where the data are recorded using a data logger.

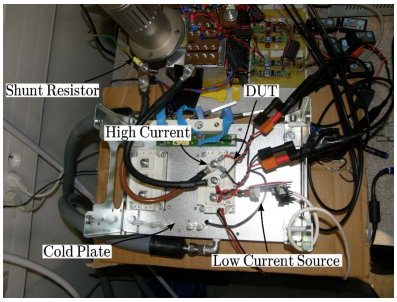


Fig. 15. DUTs mounted on the cold plate, and connected to the current sources

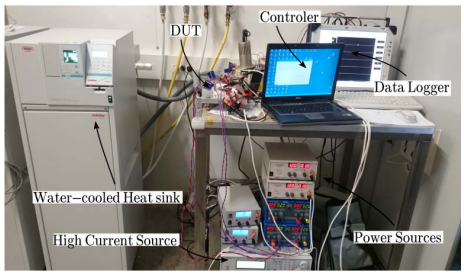


Fig. 16. Thermal impedances measurement test bench

2) Results

Fig. 17 represents the obtained thermal impedances, where "Cat 1" represents the self-heating thermal impedances. "Cat 2" represents the mutual thermal coupling impedances between the semiconductor devices inside the same power module, whereas "Cat 3" represents the same for semiconductors of different power modules. It can be noticed that "Cat 2" impedances cannot be neglected, thus it is crucial to consider the thermal coupling between the semiconductors inside the inverter, in order to accurately build its thermal model. Finally all the thermal impedances were fitted with the Least Squares Methods, as presented in Fig. 18, where Zth_{ii} represents the Junction-Ambient self-heating thermal impedance of the device D_i, whereas Zth_{ji} represents the mutual thermal coupling impedances between devices D_j and D_i. The measured impedances are then implemented in the thermal model of the SiC MOSFET DC/AC inverter, and the junction temperature corresponding to the ageing profile can be thus estimated using (2). Finally, the ageing profile parameters presented in Fig. 1 were then determined after several refinements, correspondingly to the desired junction temperature cycles, as presented in TABLE I.

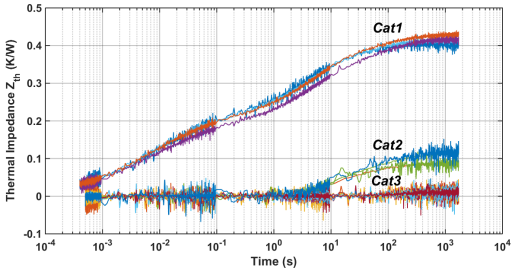


Fig. 17. Thermal impedances of all MOSFETs

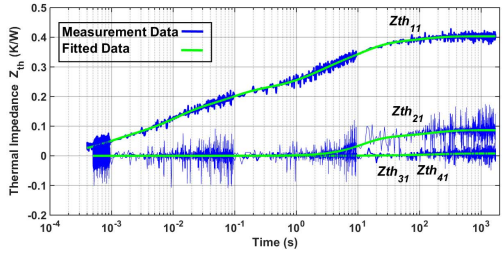


Fig. 18. Fitting the thermal impedances of MOSFET D_1 (Fig. 4)

TABLE I. THE AGEING PROFILE PARAMETERS

Parameter	I_{MAX}	I_{LIMIT}	T_{on}	T_{off}	Ta_{min}	Ta_{max}	t_p
Value	90A	60A	30s	30s	10°C	40°C	15min

VI. PRELIMINARY RESULTS

The accelerated ageing is stopped periodically to apply the diagnostics of the semiconductor devices after disconnecting them, using the *Keysight B1506A* Analyzer, while fixing the DUT temperature using a Thermo Stream, as represented in Fig. 19. This is a complicated and time-consuming process and can be automated in the future. However, the purpose is to monitor the maximum number of electrical parameters, in order to determine the ones that could be considered as indicators of ageing/failure of SiC MOSFET power modules, used in DC/AC photovoltaic inverters. Hence, the monitored electrical parameters are: the gate leakage currents IG_{SS} and

$IG_{SS(-)}$, the drain to source on resistance RDS_{on}, the gate to source threshold voltage VGS_{th}, the drain leakage current ID_{SS}, the drain to source on voltage V_{DSon}, the body diode forward voltage V_{SD}, the internal gate resistance R_g, the input capacitance Ci_{ss}, the output capacitance Co_{ss} and the reverse transfer capacitance Cr_{ss}. It should be noted that a carbon sheet is used as thermal interface between the cold plate and the MOSFETs, which are fixed with a constant tightening torque of 5 N.m, in order to prevent any change in the thermal behavior of the system, while disconnecting the MOSFETs.

All the parameters values are normalized in the following figures to better represent their evolutions as a function of the cycling duration. Fig. 20 represents the evolution of the gate to source threshold voltage VGS_{th} of the MOSFETs during 336 h. VGS_{th} of D_3 and D_4 increases gradually of ~ 6%, whereas VGS_{th} of D_1 and D_2 increases of ~ 5%. Similarly, Fig. 21 represents the evolution of the drain leakage current ID_{SS} of the MOSFETs during 336 h. It decreases a tiny bit gradually during 264 h for all MOSFETs, and then increases abruptly of ~ 300%, 63%, 240% and 73% respectively for D_1, D_2, D_3 and D_4. Similarly, Fig. 22 represents the evolution of the MOSFETs drain to source on resistance RDS_{on} during 336 h of cycling time. This parameter increases gradually of ~ 12%, 13%, 5% and 16.5% respectively for D_1, D_2, D_3 and D_4. It should be noted that V_{SD} shows a similar evolution as RDS_{on}, being not represented here. Finally, Fig. 23 represents the evolution of Ci_{ss}, Co_{ss} and Cr_{ss} for D_1 as a function of the cycling duration, where Co_{ss} and Cr_{ss} slightly increase ($\leq$ 3%), whereas Ci_{ss} lightly decreases ($\leq$ 1%). The other MOSFETs show similar evolution of these parasitic capacitances. The other monitored parameters do not show remarkable changes, however it should be noted that none of the MOSFETs has failed yet.

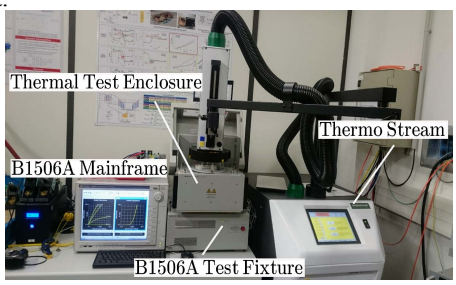


Fig. 19. Monitoring the electrical parameters using the *B1506A* Analyser with the Thermo Stream.

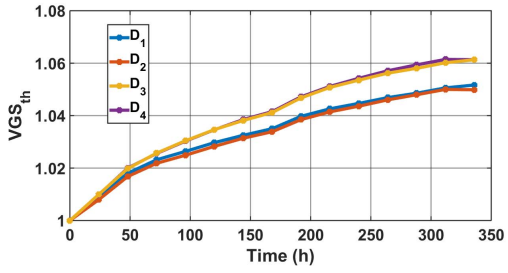


Fig. 20. Evolution of VGS_{th} as a function of the cycling duration

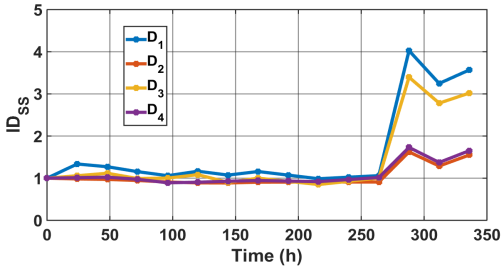


Fig. 21. Evolution of ID_{SS} as a function of the cycling duration

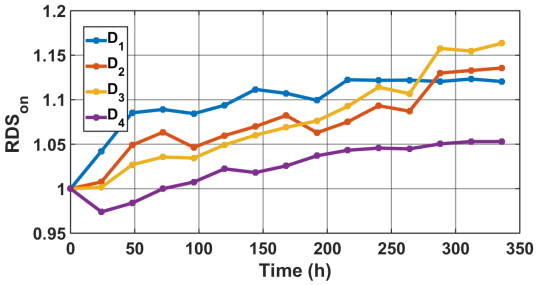


Fig. 22. Evolution of RDS_{on} as a function of the cycling duration

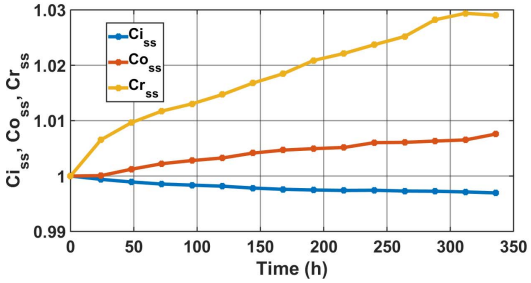


Fig. 23. Evolution of Ci_{ss}, Co_{ss} and Cr_{ss} of D_1 as a function of the cycling duration

VII. Conclusions

This paper presents a new concept of ageing test bench dedicated to photovoltaic inverters, where the accelerated ageing test reproduces a typical profile of the photovoltaic inverters RMS output current. The current profile was obtained by analyzing the mission profiles of the current and the ambient temperature, extracted over several years from different photovoltaic plants. The profile was then introduced into a power losses estimation model, coupled with a thermal model to estimate the correspondent junction temperature of the semiconductor devices, in order to determine the profile parameters. To do so, a double pulse test was applied on the semiconductor devices, in order to measure the switching and the recovery energy losses of the devices, in the same conditions of the accelerated ageing test. Then the self-heating and the mutual thermal coupling impedances between the devices were measured, using the forward voltage of the MOSFET's intrinsic body diode as a TSEP. Finally, the obtained ageing profile was applied during the accelerated ageing test, where active and passive cycling were

simultaneously done, under switching nominal conditions and pulse width modulation (PWM) operating mode. The accelerated ageing was stopped periodically, in order to apply the diagnostics of the semiconductor devices, using the *Keysight B1506A* Analyzer. The results showed for all the MOSFETs a progressive increase in the values of V_{GSth}, R_{DSon}, V_{DSon}, and V_{SD}, whereas an abrupt increase in I_{DSS}. These are preliminary results of just one ageing test where none of the MOSFETs has failed yet. Hence, more similar accelerated ageing tests should be performed on different MOSFET devices, in order to confirm that these parameters can serve as indicators of ageing/failures of SiC MOSFET power modules used in photovoltaic inverters.

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REFERENCES

[1] C. Sintamarean, H. Wang, F. Blaabjerg, F. Iannuzzo, "The Impact of Gate-Driver Parameters Variation and Device Degradation in the PV-Inverter Lifetime", Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE 2014), Pittsburgh, PA, USA,14-18 September, 2014.

[2] J. M. Thebaud, E. Woirgard, C. Zardini, S. Azzopardi, O. Briat and J. M. Vinassa, "Strategy for designing accelerated aging tests to evaluate IGBT power modules lifetime in real operation mode", in IEEE Transactions on Components and Packaging Technologies, vol. 26, no. 2, pp. 429-438, June 2003. doi: 10.1109/TCAPT.2003.815112.

[3] ECPE Tutorial, "Thermal Engineering of Power Electronic Systems Part II", Oct 18th-19th., 2016, Nuremberg, Deutschland.

[4] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, "Application Manual Power Semiconductors", ISLE Verlag 2011.

[5] V. Smet *et al*., "Ageing and Failure Modes of IGBT Modules in High-Temperature Power Cycling," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 10, pp. 4931-4941, Oct. 2011. doi: 10.1109/TIE.2011.2114313.

[6] U. M. Choi; F. Blaabjerg; S. Jorgensen, "Power Cycling Test Methods for Reliability Assessment of Power Device Modules in respect to Temperature Stress," in IEEE Transactions on Power Electronics , vol.PP, no.99, pp.1-1. doi: 10.1109/TPEL.2017.2690500.

[7] Bahman, A.S., Iannuzzo, F., Blaabjerg, F. "Mission-profile-based stress analysis of bond-wires in SiC power modules", Microelectronics Reliability, Volume 64, September 2016, pp. 419-424, 2016.

[8] M. G. Dbeiss, Y. Avenas, H. Zara and L. Dupont, "A method for accelerated ageing tests of photovoltaic inverters considering the application's mission profiles," *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Warsaw, Poland, 2017, pp. P.1-P.10. doi: 10.23919/EPE17ECCEEurope.2017.8099055.

[9] G. Grossmann, G. Nicoletti and U. Soler, "Results of comparative reliability tests on lead-free solder alloys," 52nd Electronic Components and Technology Conference 2002. (Cat. No.02CH37345), 2002, pp. 1232-1237.doi: 10.1109/ECTC.2002.1008264

[10] M. Ciappa, F. Carbognani and W. Fichtner, "Lifetime prediction and design of reliability tests for high-power devices in automotive applications," in *IEEE Transactions on Device and Materials Reliability*, vol. 3, no. 4, pp. 191-196, Dec. 2003.doi: 10.1109/TDMR.2003.818148

[11] Mouhannad Dbeiss, Yvan Avenas, Henri Zara, "Comparison of the electro-thermal constraints on SiC MOSFET and Si IGBT power modules in photovoltaic DC/AC inverters", In Microelectronics Reliability, Volume 78, 2017, Pages 65-71, ISSN 0026-2714. doi.org/10.1016/j.microrel.2017.07.087.

[12] A.Wintrich, U. Nicolai, W. Tursky, T. Reimann, Application Manual Power Semiconductors, ISLE Verlag, 2011.

[13] Y. Yang, H. Wang and F. Blaabjerg, "Improved reliability of single phase PV inverters by limiting the maximum feed-in power," *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh, PA, 2014, pp. 128-135. doi: 10.1109/ECCE.2014.6953385.

[14] Z. Wang, J. Zhang, X. Wu and K. Sheng, "Evaluation of reverse recovery characteristic of silicon carbide metal–oxide–semiconductor field-effect transistor intrinsic diode," in *IET Power Electronics*, vol. 9, no. 5, pp. 969-976, 4 20 2016. doi: 10.1049/iet-pel.2014.0965

[15] S. Bontemps, A. Basler and P. L. Doumergue, "Evaluation of the need for SiC SBD in parallel with SiC MOSFETs in a module phase leg configuration," *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, 2015, pp. 1-7.

[16] R. Horff, A. März, M. Lechler and M. M. Bakran, "Optimised switching of a SiC MOSFET in a VSI using the body diode and additional Schottky barrier diode," *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Geneva, 2015, pp. 1-11.doi: 10.1109/EPE.2015.7309102.

[17] Z. Zhang *et al*., "Methodology for switching characterization evaluation of wide band-gap devices in a phase-leg configuration," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014, pp. 2534-2541. doi: 10.1109/APEC.2014.6803660.

[18] ROHM Application Note 'SiC Power Devices and Modules', Rev.001, Issue of June 2013.

[19] Brandelero, J. C. (2015). Conception et réalisation d'un convertisseur multicellulaire DC/DC isolé pour application aéronautique (Doctoral dissertation, École Doctorale Génie Électrique, Électronique et Télécommunications: du système au nanosystème (Toulouse); 154235504).

[20] H. Li, S. Beczkowski, S. Munk-Nielsen, K. Lu and Q. Wu, "Current measurement method for characterization of fast switching power semiconductors with Silicon Steel Current Transformer," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 2527-2531. doi: 10.1109/APEC.2015.7104706.

[21] *Callanan, B. (2011). SiC MOSFET double pulse fixture. Cree Application Note.*

[22] J. J. Nelson, G. Venkataramanan and A. M. El-Refaie, "Fast thermal profiling of power semiconductor devices using Fourier techniques," in *IEEE Transactions on Industrial Electronics*, vol. 53, no. 2, pp. 521-529, April 2006. doi: 10.1109/TIE.2006.870714.

[23] M. Correvon, "Electronique de puissance", Chapitre 9: Modélisation thermique des composants de puissance, Heig-vd, Heis.so.

[24] Dr.D.Kundur, "Overlap-Save and Overlap-Add", University of Toronto.

[25] ECPE Tutorial "Thermal Engineering of Power Electronic Systems", Part I: Thermal Design and Verification, 19 – 20 July 2016, Erlangen, Germany.

[26] A.Wintrich, "Junction temperature prediction by using integrated temperature sensors", Application note January 2018, Semikron.

[27] Infineon, "Thermal equivalent circuit models", AN8003, Application Note V1.0, 2008

[28] Y. Avenas, L. Dupont and Z. Khatir, "Temperature Measurement of Power Semiconductor Devices by Thermo-Sensitive Electrical Parameters—A Review," in *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 3081-3092, June 2012. doi: 10.1109/TPEL.2011.2178433.