Top Die Surface Reprocessing for Planar Package with Double Sided Cooling

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***Abstract*—In this paper, a compact planar package module design is presented for EV application. The top surfaces of dies are reprocessed and sputtered to enlarge the gate pad for easy soldering. This method can help to build a double sided-cooled thermal system in converter systems..**

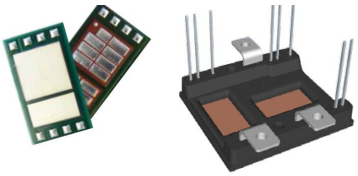
Keywords—planar packaging; power module.

I. INTRODUCTION

During the last decade, people have made great efforts on exploiting the ability of electric vehicles (HEV/EVs). Power semiconductor module is one of the most important components in EV system [1,2]. Recently, to increase the power density and reduce cost, many advanced power converter system and power modules for EV applications were developed [3]. In an EV converter system, parasitic parameters in a power module have a detrimental effect on switching loss and dynamic behavior [1]. They cause voltage overshoot, affect blocking voltage requirements of the power devices, and influence device switching losses. These phenomena are exaggerated when power density increases. Novel power semiconductor packaging methods were introduced and they targeted to reduce conduction and switching power losses while obtaining the minimum volume and weight. Recently, advanced die top-side interconnection methods, instead of bond wires, have emerged in many planar package designs [5-10].

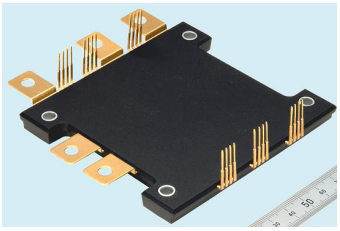
Moreover, double-sided cooling enables reduction of thermal resistances in an EV converter system. Smaller dies can be used for the same power rating [6]. Double-sided cooling also requires planar assembly methods to remove wire-bond interconnections. In the past 10 years, planar package technologies already demonstrate improvements in electrical and thermal performance for EV applications. Some of the existing planar packages are shown in Fig.1.

Although efforts have been spent in realizing the planar packages, issues are still remain in most of the packaging techniques. The main problem comes from the gate pads. The dimensions of gate pads are too small, and some of them are enclosed by emitter pads. All these limits increase the challenge of the die top-side interconnection. The dimensions of some gate pads are listed in Table 1.

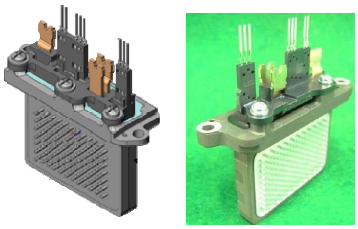


International Rectifier COOLiR²Bridge[6]

Infineon FF400R07A01E3_S6[7]



Mitsubishi CT600CJ1A060[8]



Hitachi DWDSCPM[9]

Fig. 1. IGBT module product with planar package.

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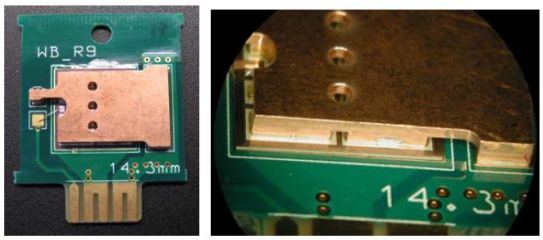
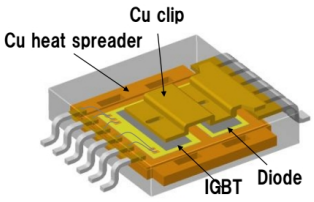
TABLE I. GATE PAD SIZE FOR SI AND SIC DIES

Die	Part number	Gate pad size(mm × mm)
Si IGBT	IGC100T65T8RM (650 V 200 A)	1 × 1.7 (corner)
Si IGBT	IRGC4275B(650 V 200 A)	0.82 × 1.62(die center)
SiC JFET	UJN1205Z(1200 V 23 A)	0.35 × 0.7(edge center)
SiC MOSFET	CPM2-1200-0025B(1200 V 50 A)	0.5 × 0.8(corner)
SiC MOSFET	CPM3-0900-0010A(900 V 100 A)	0.5 × 1.2(corner)

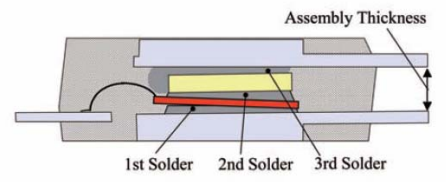
With small gate pad, many planar module designs were pushed back to use wirebond again for gate signal connection. Examples can be found from International Rectifier Cu-clip IGBT, Renesas Clip Bonding Package, Denso Double-sided Cooling Power Modules and Mitsubishi TPM BLD modules (as shown in Fig. 2).



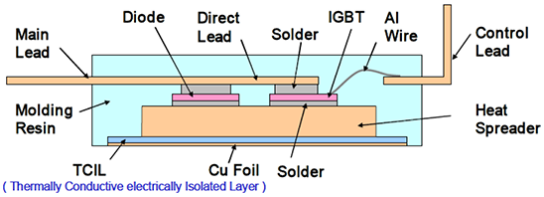
International Rectifier Cu-clip IGBT[10]



Renesas Clip Bonding Package[11]



Denso Double-sided Cooling Power Modules[12]



Mitsubishi TPM BLD[13]

Fig. 2. Planar package with wire bonded gate signal.

To align and bond die top-side pads, a top surface reprocessing method is presented. It can perform as the main feature of multi-chip planar package designs (device number over 10). Based on this reprocessing method, this paper describes a planar package design for a compact Si IGBT module. It could be a major step to improve the overall performance of future planar modules.

II. A DIE TOP SURFACE REPROCESSING

In planar packaged module designs, there are more than 30 device bonding methods and related structure presented in literatures [14]. By top side bonding methods, it can be classified as direct soldering, indirect soldering, pressure contact and sputtering plus electroplating (shown in Table.2). However, these methods are seldom used for multi-chip module, especially when die number is over 10. Since small gate pad does not provide enough bonding margin, it requires very precise alignment which may cost a lot in large volume productions.

TABLE II. PLANAR PACKAGE BONDING CATEGORY

Bonding Category	Organization	Method name	Methods for possible issues
Direct soldering	Vishay Siliconix	PowerConnect	Using buffer layer or thick solder layer to reduce CTE mismatch and other reliability issues.
	Fairchild	DR.MOS	
	International Rectifier	CopperStrap	
		Cu-clip	
		Power Pack	
		DirectFET	
		COOLiR^{2}Bridge	
	NXP	LFPAK	
	Nottingham Univ	Power sandwich	
	Infineon	HybridPack DSC	
	Renesas	Clip Bonding	
	Denso	Double-sided Cooling	
	Mitsubishi	TPM BLD	
Indirect soldering	CPES	MPIPPS	Using thermal conduct and electrical insulation encapsulant to compensate relatively low heat dissipation from top side
		D2BGA	
		FCOF	
		Dimple array	
		Flex-power	
		J. Xu high voltage	
	Fairchild	SO-8 wireless	
		BGA MOSFET	
		PowerTrench	
	Alstom	Power bump	
	International Rectifier	FlipFet	
Pressure contact	Westcode of IXYS	Press-Pack	Using special mechanical contact gadget to relieve large stress and mis-alignment
	ABB	StakPak	
	China SGRI	High voltage IGBT Pack	
	CRRC Zhuzhou	High voltage IGBT Pack	

Sputtering + electroplat -ing	GE	Power overlay	Current can not be large
	Embedded power	CPES	
Ag paste sintering	CPES	Flex-power	Multi-step top side interconnection for mis-alignment
		APEC09	
	Semikron	SkiN	

To solve this problem, gate pads can be reprocessed and enlarged to reduce the alignment requirement (shown in Fig.3).

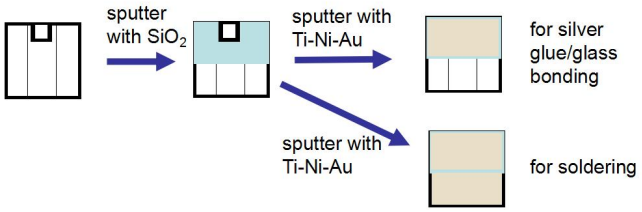


Fig. 3. Die top surface reprocessing.

In the first reprocessing step, part of emitter pads, which surrounding gate pads are sputtered with SiO2. Since there is usually less than 50 V requirement between emitter pad and gate pad, a 300 nm thick SiO2 layer is enough. With fixture and masks shown in Fig.4, the gate pads on IGBTs will not be covered by SiO2. In the next step, another mask will be used for metal sputtering on gate pads. If silver glass bonding is selected as top interconnection method, the original aluminum layer is enough, and the third mask in Fig.4 is chosen. If choosing soldering as top side bonding method, emitter pads need to be sputtered with solderable metal, for example, Au, Ag or Cu. Before Au and Ag sputtering, a thin Ti layer and Ni layer are required.

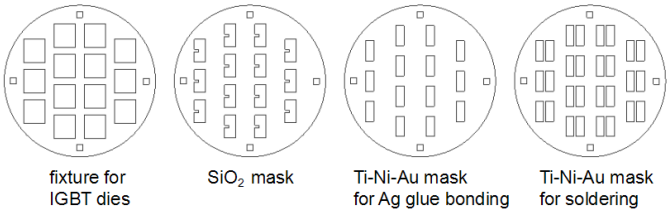


Fig. 4. Fig.4. Fixture and masks for reprocessing.

Fig. 5. Sputtering machine for die top surface reprocessing.

To speed up the reprocess and reduce the pollution possibility, multiple source sputtering machine is preferred. The sputtering machine is shown in Fig.5.

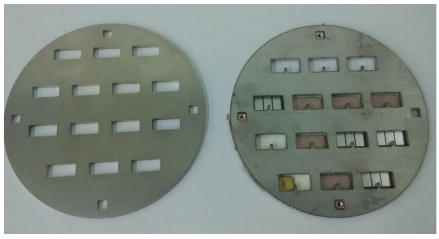


Fig. 6. fixture mounted with dies

To mitigate the different die heights for multi-chip package (die number over 10), the first investigation begin with the silver glue bonding for top die surface. For bottom side bonding, SAC305 solder preform is selected. The fabricated sputtering fixture and mask is shown in Fig.6.

The reprocessed Diode dies with Ti-Ni-Au are shown in Fig.7. The IGBT dies were reprocessed both with Ti-Ni-Ag and Ti-Ni-Au for comparison purpose, they are shown in Fig. 8 (four dies with Ag and four dies with Au).

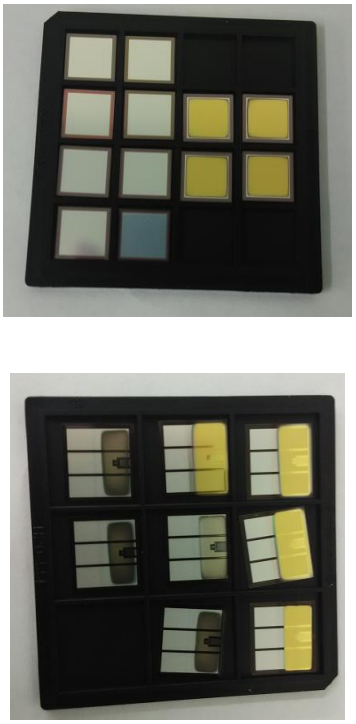


Fig. 7. Diode and IGBT reprocessed with Ti-Ni-Au.

To reduce the cost and reprocessing time, copper was also tried and sputtered directly on the top of SiO_2 layer. The reprocessed IGBT dies are shown in Fig.8. After the sputtering, the device need to be soldered or bonded immediately to mitigate the oxidation.

Fig. 8. IGBT die top surface reprocessed with Cu.

The thickness of sputtered layers is listed in Table 3.

TABLE III. THICKNESS OF SPUTTERED LAYERS

Layer	Thickness
SiO2	300 nm
Ti	80 nm
Ni	50 nm
Ag	50 nm
Au	50 nm
Cu	150 nm

III. PLANAR PACKAGE DEVELOPMENT AND EVALUATION

For 30~120 kW EV applications, 650 V, 400A to 600A three phase power modules are very popular. Based on 650 V/200 A Si IGBT IRGC4275B and 650 V/200 A Si diode SIDC50D65C8, a phase-leg planar module (6 IGBTs and 6 diodes) is designed and shown in Fig. 9. Dies are reprocessed by the presented method.

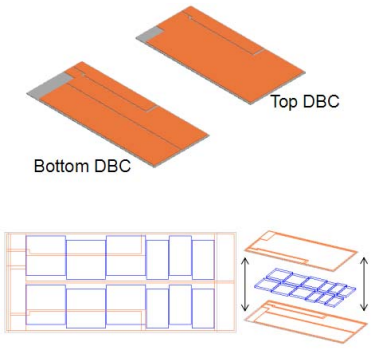


Fig. 9. DBC designs and phase-leg module assembly.

Fig. 10. Single phase planar module.

A phase-leg planar module is developed and shown in Fig.10. It can be further integrated as a three phase module. With the same power rating, the size is reduced by 18% compared with the compact wirebond module presented in [15] . The double sided cooling structure is depicted in Fig.11.

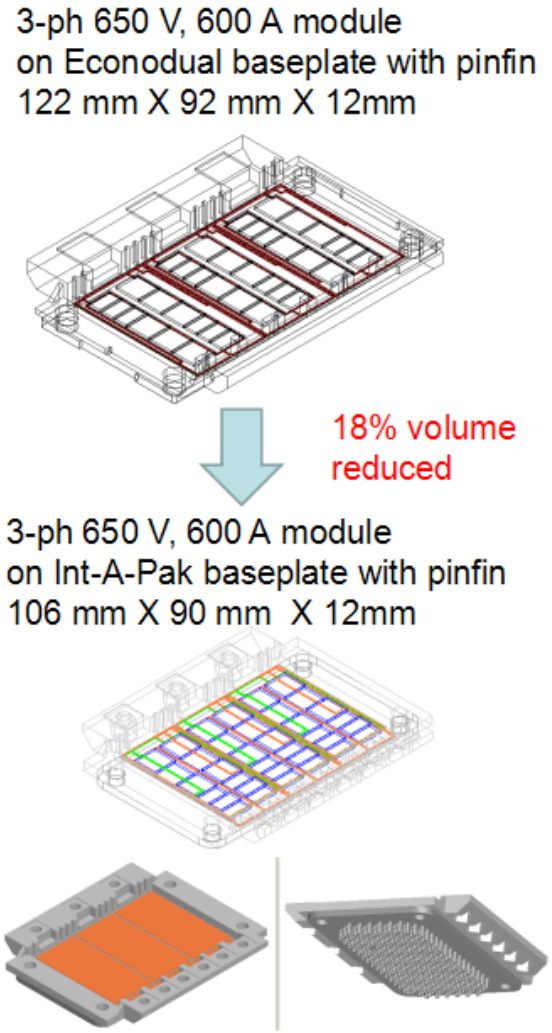


Fig. 11. Three phase planar module design.

To dissipate the heat from top side of planar module, pinfin baseplate and related cooling fixtures are added to the module. The double sided cooling structure is depicted in Fig.12.

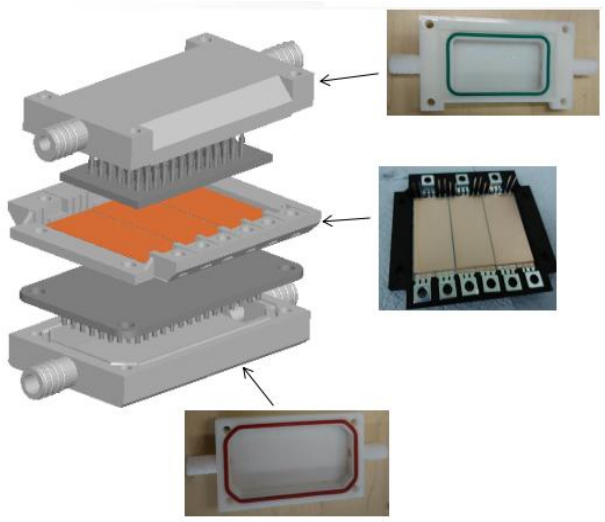
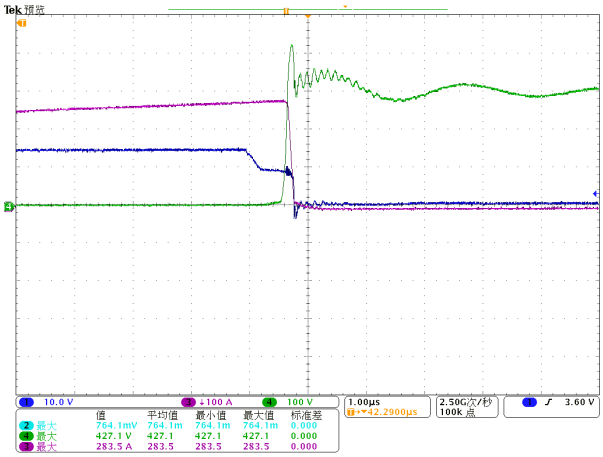


Fig. 12. Double sided cooling structure.

A developed 1200 V/600 A three phase prototype module with double sided cooling structure is shown in Fig.13.

Fig. 13. Three phase module will double sided cooling.



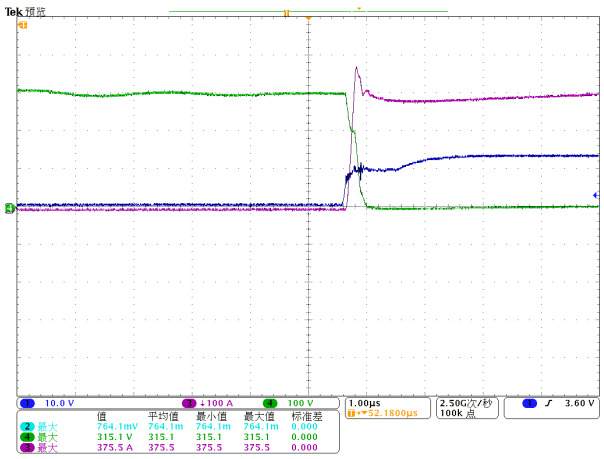


Fig. 14. Double pulse test waveform

Double-pulse testing was used to evaluate electrical performance of the prototype module. It is performed by operating the phase-leg module in a standard switching process, which includes switch-on, conduction, switch-off and blocking modes with an inductive load. The switching waveform at 600 V/280 A is shown in Fig.14.

In the next step, after the full evaluation, the presented module will be used for a 50 kW EV motor drive system. At the same time, soldering will be used for both top and bottom connection.

IV. SUMMARY AND CONCLUSION

This paper discusses a planar package based compact power module for EV applications. Some practical considerations are introduced and implemented in the die top surface reprocessing. It could be a major step to improve the overall performance of future converters..

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