# Modular Heat Sink for Chip-Scale GaN Transistors in Multilevel Converters

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***Abstract*—The flying capacitor multilevel topology shows promise for high power density inverter designs and presents new cooling challenges. Typical implementations feature a number of coplanar power transistors, including those with top-cooled, flip-chip packages, assembled on a single printed circuit board or array of switching cell daughter boards. Cooling each transistor requires the use of a compressible thermal interface material to compensate for component height tolerance and to provide electrical insulation. However, this interface material presents a high impedance in the thermal path. Thus, a modular approach for forced-air heat sinking is proposed, where variation in height can be accommodated per device while electrical isolation may no longer be necessary. This scheme allows a thinner, less compliant, and higher performance interface material to be used. Additionally, a 3D-printed manifold is presented as a means to favorably direct forced-air across the cooling surfaces.**

## I. Introduction

The current thrust towards more electric vehicles demands major advances in high efficiency and high power density electric drive systems [1]–[4]. For future electric aircrafts, high specific power density of electric machines and power electronics has been identified as a key challenge that must be addressed. Recent work has shown the potential of very high power density inverter designs using the flying capacitor multilevel (FCML) topology [5]. A multi-level topology may be particularly suitable for driving high density electric machines, which can achieve very low weight through the removal of iron, yielding a high reluctance (i.e., low inductance) machine [6]. Conventional two-level inverters would require additional filtering to be added at the inverter output to generate the low total harmonic distortion (THD) waveforms needed for smooth and efficient motor operation. Multi-level topologies [7], in contrast, can provide a waveform with low THD that requires little to no filtering, depending on the motor requirements. Recent 9- and 13-level FCML designs [8], [9] have demonstrated the feasibility of these designs at high frequency and voltage, utilizing gallium-nitride (GaN) transistors to achieve high efficiency and specific power density.

However, implementing this topology at high power introduces new cooling challenges due to the increased number of power transistors requiring heat sinking. Additionally, the use of chip-scale, wide-bandgap (WBG) devices to facilitate compact layouts and higher switching frequencies requires the extraction of a greater amount of heat per area as compared to equivalent power MOSFETs [10]. Lightweight and compact heat sink design is thus an important consideration for any high power density converter; Therefore, this work focuses a modular heat sink strategy that enables both increased heat transfer and reduced weight for FCML converters using WBG, flip-chip devices. The remainder of this manuscript is organized as follows; Section II outlines some challenges and opportunities associated with thermal management of multi-level converters, and Section III details the approach taken in this work, demonstrating how thermal management might be integrated into the packaging of each switching cell. Then, Section IV presents simulation results used to verify the proposed heat sink performance and choice of fan. Next, Section V provides the methodology for characterizing the experimental performance of the proposed TIM material as well as the thermal and electrical performance of a prototype converter operating up to 5 kW output power. Finally, Section VI concludes the manuscript and sets goals for future work.

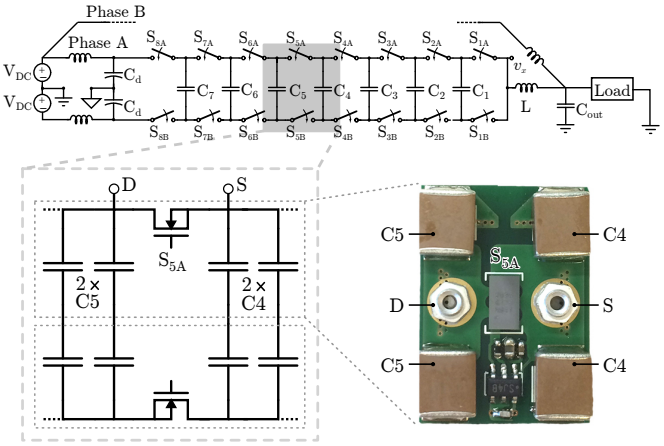


Fig. 1: Schematic of a dual-interleaved 9-level FCML inverter with a switching cell that includes modular heat sink mounts.

## II. Multi-Level Converter Thermal Management Challenges and Opportunities

### A. Heat spreading benefits of FCML converter

In addition to dramatically reduced inductor size [5] due to the decreased voltage and increased effective ripple fre-

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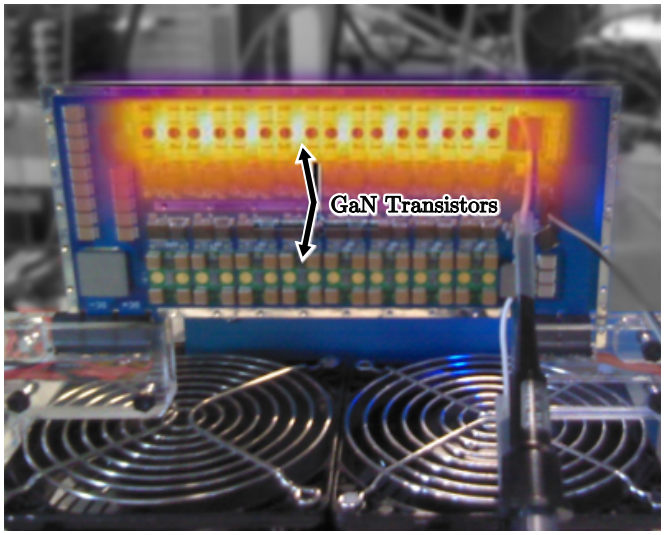


Fig. 2: Thermal image demonstrating heat spreading properties of the FCML converter. Eight GaN transistors are on the top-side of the PCB, with the remaining eight complementary switches on the opposite side of the PCB (not shown).

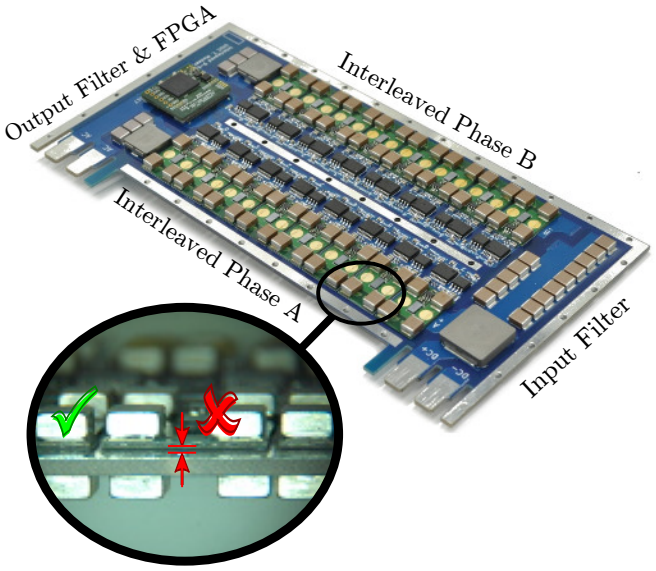


Fig. 3: Annotated 9-level interleaved converter adapted for this study. Inset figure shows how variations in device height can arise from uneven switching cell placement.

quency at the switching node ($v_x$ in Figure 1), the FCML topology provides desirable heat spreading that enables improved thermal management designs. Specifically, as each transistor sees only a fraction of the input voltage ($\frac{V_{in}}{N-1}$ for an N-level FCML converter), low-voltage transistors can be employed, with correspondingly low on-state resistance and parasitic capacitance. Overall, each transistor thus sees lower conduction and switching losses than what would be realized in a conventional, 2-level design. Of course, the increased number of switches in the FCML topology means that the overall transistor losses are not necessarily lower than for a 2-level design; the detailed loss scaling of FCML converters versus 2-level converters depends on many factors, some of which are discussed in [5].

However, the spreading of transistor losses over several distributed (in space) transistors does yield certain thermal management advantages, in particular with respect to the avoidance of hot-spots on the converter itself. For the 9-level FCML converter considered in this work (of which a high-level schematic drawing is provided in Figure 1), there are a total of 16 transistors in each phase (with a total of two interleaved phases in this design). As shown in the composite[] thermal image of Figure 2, the heat generated due to transistor conduction and switching losses is spread out across all of the top-side transistors, generating a heat profile that is evenly distributed across a relatively large area.

### *B. Heatsink and thermal interface material challenges of chip-scale power transistors*

The use of chip-scale GaN power transistors in this application enables very low packaging inductance and resistance, critical for the high frequency operation needed to reduce the passive component sizes. Moreover, through careful layout of an integrated switching cell (Figure 1), the commutation loop of complimentary switches in the FCML converter can be kept tight, using local decoupling capacitance and optimized traces and vias [11]. The GaN power transistors employed in this work (EPC 2034) are supplied as passivated die with solder bumps, yielding excellent electrical characteristics but challenging mechanical and thermal management. In particular, the devices are designed primarily for top-cooling, with significantly lower (i.e., $\sim$ 10x [12]) thermal resistance to the top side than through the solder bumps to the board.

Previously, designers have sought to use a single heat sink for cooling power devices assembled on a single side [9], [13], or a two-part clamshell heat sink for dual-sided cooling [8]. However, mating several components to a single heat sink requires the use of a compressible thermal interface material (TIM) to compensate for variation in component height. Tight tolerances on heat sink features are also necessary to ensure components are not compressed beyond manufacturer recommendations [14] but still achieve adequate thermal contact [9], [10]. Furthermore, use of a single heat sink requires the TIM to be electrically insulating [10], limiting the choice of materials.

An added challenge in the FCML design is the mechanical tolerance of the heights of individual GaN transistors. Different surface finishes, pad designs or assembly processes can lead to die tilt or variation in seated die height [15]. Additionally, these transistors are usually mounted on thin switching cell daughter boards that are then assembled onto a converter motherboard. Poor process control during switching cell attachment can lead to uneven seating across the converter, as illustrated in Figure 3, further affecting coplanarity among device surfaces across in the converter.

## III. Modular Design

Given these challenges associated with accommodating device tolerances with a single heat sink, consideration might be

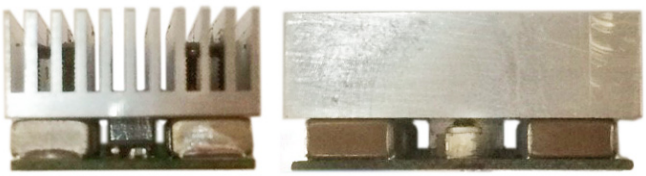

Fig. 4: Front and side views of the new switching cell with modular heat sink mounted using the SMT nuts.

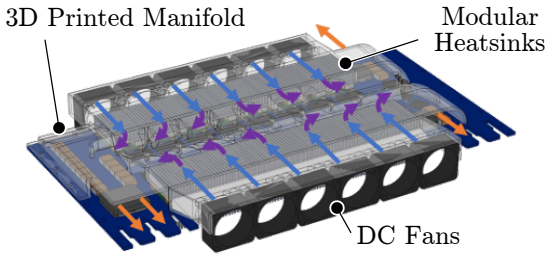


Fig. 5: Render illustrating the assembled manifold and forced-air cooling path. Intake air (blue) passes through the modular heat sinks, along the PCB and other components (purple), then exhausts across the inlet and outlet filter passives (orange).

given to an approach that focuses on addressing the thermal management of individual devices. Such a modular design has two main key components – the heat sink and thermal interface, and the coolant source (such as forced-air from a DC fan) and ducting to direct its flow.

### A. Heat Sink and Mounting

Tight spacing between the flying capacitors and transistors (necessary for low inductance designs [8]), as well as the routed copper traces that connect them, precludes the use of through-hole heat sink mount points close to the active device. Additionally, locating mount points far away from the package is undesirable due to the additional mass from the heat sink extending to the mount point, and the rigidity between device and mount point necessary to ensure a good thermal contact. However, if insulating fasteners are used, surface mount (SMT) nuts provide a means to mount the heat sink very close to the device; the nuts can be attached to otherwise vacant space above the copper traces. Furthermore, many FCML implementations utilize an electrically-thin [16] switching cell daughter board approach, packaging the gate driver, WBG transistor and flying capacitors on a single, low-inductance sub-assembly which is then attached to a mother-board using a low temperature solder; additionally packaging the heat sink with this switching cell is a step towards tighter device integration. The switching cell is designed with pads for SMT nuts on copper connected to the source and drain of the WBG chip, shown in Figure 1. Then, the heat sink can be mounted using insulating screws, shown in Figure 4, assuring good thermal contact to the WBG device without the use of a thick, compressible TIM. Now, component height variation is no longer an issue, and mounting force can be set to the manufacturer specification [14] by controlling the torque applied to the screws.

### B. 3D Printed Manifold

With the heat sinks mounted on the individual switching cells, thermal design at the system level now consists of directing the desired airflow across the heat sinks. This can be accomplished through thoughtful fan placement and ducting attached to the inverter, and is a much less constrained design space than that of the single- or dual-sided heat sinks of previous FCML inverter designs. Figure 5 shows a model of an interleaved 9-level FCML inverter with an annotated view of the aforementioned manifold for directing the forced-air. Here, air is directed into the manifold by twelve DC fans, six on both the front and back, and across the heat sinks. Then, the air travels down through the inner ducting, across the PCB surface, and exhausts out the sides to provide additional cooling to the PCB and finally the filter passives on each side. These manifold parts are designed to be 3D printed and retrofitted onto the existing inverter design of [17].

## IV. Simulation Results

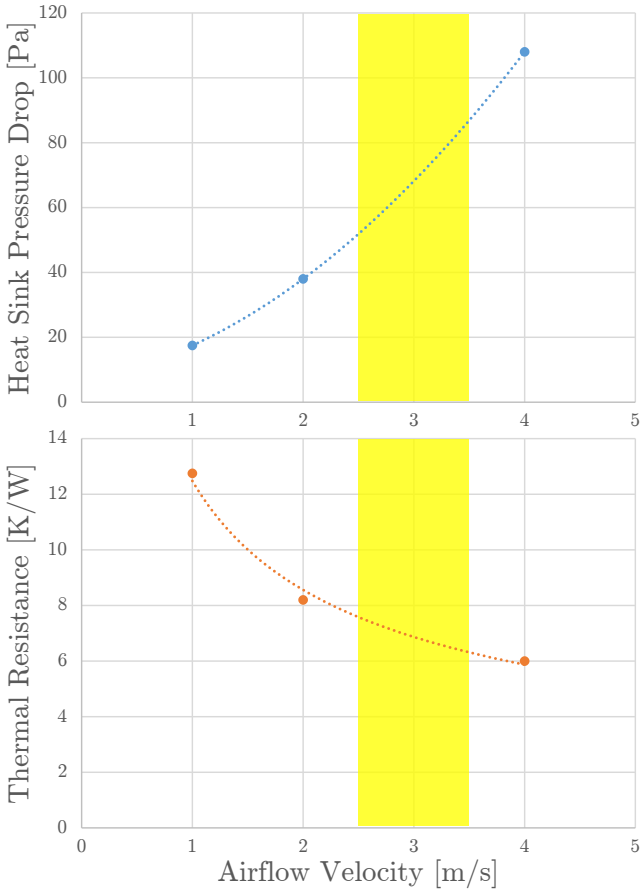


Fig. 6: CFD simulation results. The target for an achievable fan operating point highlighted in yellow.

The proposed heat sink in Figure 4 was designed with features that could reasonably be machined while minimizing the metal cross section. As part of this design process, CFD simulations were conducted to estimate the pressure drop and thermal resistance across a single heat sink as a function of airflow. Using results of this analysis, shown in Figure 6, the cooling needs of the entire converter, and form factor constraints as part search parameters, SUNON MC20100V2 5V DC fans were selected as the best match.

Although this approach seeks the additional capacity of using the airflow exiting the modular heat sinks to provide cooling to the PCB and filter passives, it is important that additional resistance in the fluid path caused by the manifold and ducting not hinder the performance of the heat sinks. Here, CFD analysis could also be performed to study how routing this exhaust air through the full inverter system will affect pressures and airflow. However, due to the complexity and dynamic range of the features and volumes in the fluid channels for this converter, this type of CFD study was not completed by the time of publication but will be explored in future work. Additionally, while the heat sink in Figure 4 was fabricated using traditional machining, a folded fin variant was also considered as a means to reduce pressure drop across the heat sink and allow for higher airflow velocities. However, additional simulations indicated the folded fin variant was within 5% of the thermal resistance of the traditionally machined heat sink. Given that the traditionally machined heat sink was easier to fabricate and mount to the switching cell, the folded fin design was not pursued.

## V. Experimental Results

### A. Thermal Interface Material Characterization

The TIM used in prior high density FCML converters has a high specified thermal conductivity [13], [18], but experimental measurements of these converters have indicated it may pose a major barrier towards higher efficiency and output power. Therefore, in addition to aiding the selection of a thinner TIM with a lower thermal impedance, experimental validation of the TIM thermal performance in-situ can confirm manufacturer specifications for a given application. Although various methods for characterizing TIMs for power electronics have been presented [19], [20], IR microscopy was the preferred approach in this work. Unlike [21], which required a black surface for accurate measurements, here the fixture, shown in Figure 7, is first set to a uniform temperature and the IR microscope is calibrated to compensate for the various emissivities of the materials in the fixture.

TABLE I: Experimentally measured values of $R_{TIM}$.

| 22 N Applied Pressure<br>0.7 – 5W Heat Flux | |
|---|---|
| Henkel Gap Pad 5000S35, 40 mil (1mm) | 2.94 K/W |
| Alphacool Eisschicht 17 W/mK, 1 mm | 1.47 K/W |
| Dow Corning 340 Silicone Paste | 0.82 K/W |

For thermal measurements, a switching cell is configured with the gate and source pins of the GaN transistors shorted, and current is driven in reverse direction through the GaN devices. This current flowing through the diode-like forward-conducting channel generates heat in the device; the amount of heat generated, and thus flowing through the fixture, can then be varied by controlling the dc power into the device. Next, this "thermal dummy" cell is loaded into the fixture of Figure 7. Here, the bottom copper block is controlled to match the resulting temperature of the powered device, while the upper copper block acts as a heat sink. Thus, the the heat flux is driven in only one direction – towards the upper copper block and through the TIM under test. By measuring the temperatures in the micrograph, also plotted in Figure 7, and recording the power into the thermal load, the TIM thermal resistance, $R_{TIM}$, can be calculated.

This method is beneficial in two ways: First, the TIM performance can be characterized in a mechanical configuration comparable to the end application. Second, appreciable losses in the power transistor can be emulated at low voltage and dc,

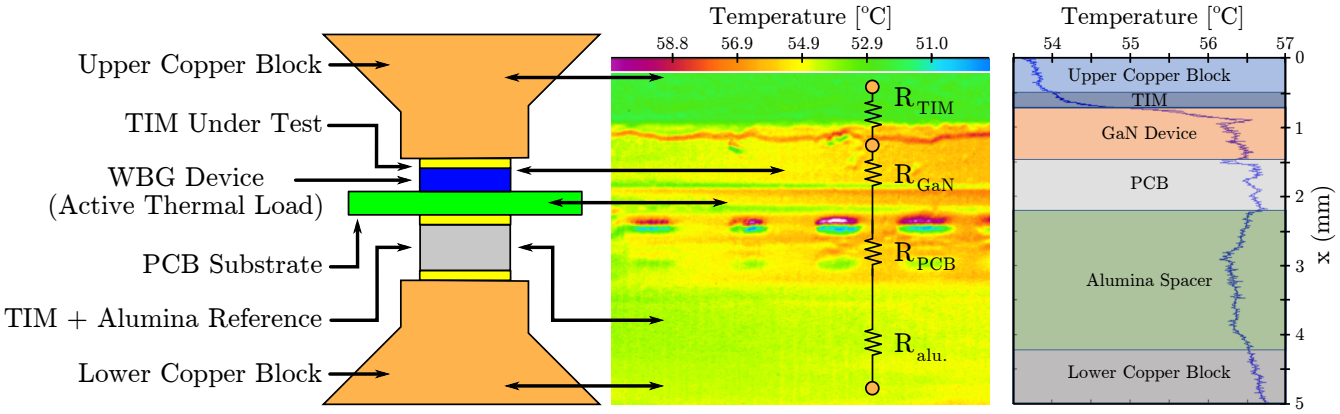


Fig. 7: Experimental setup for IR microscopy characterization of TIM thermal impedance, $R_{TIM}$. The thermal model is shown overlaid over a micrograph of the setup, with the temperature across the setup plotted on the right.

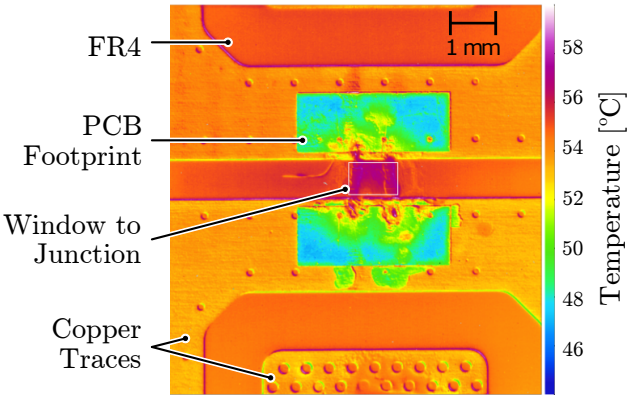


Fig. 8: IR micrograph of the bottom face (footprint side) of a switching cell . The WBG transistor is visible through the PCB via a laser-cut window between the device pads.

allowing for much safer testing compared to the equivalent losses that would arise from normal switching operation at high voltage and high current.

Table I lists the experimentally determined thermal resistances for the Henkel gap pad material used in [8], [9], [13], as well as a relatively new, higher performance material by Alphacool. Additionally, Dow Corning 340 silicone grease, a common heat sink compound, was chosen for comparison to investigate the potential gain in thermal conductivity if compliance and isolation constraints are relaxed; while Dow Corning is not specifically electrically conductive, application of the grease and mounting of the heat sink cannot guarantee the same barrier provided by the gap pads. These measured values for $R_{TIM}$ indicate a 3.5x decrease in TIM thermal resistance when using the thermal grease over a gap pad, and correspondingly a modular approach over a single heat sink.

As the device junction (and source of heat) is located on the *bottom* of the WBG part, it was necessary to verify that temperatures measured from the accessible *side* of the device die would provide an accurate representation of device temperature. Therefore, a switching cell was laser etched between the copper traces to expose a view of the part through the PCB. Then, IR micrographs through this laser-etched window

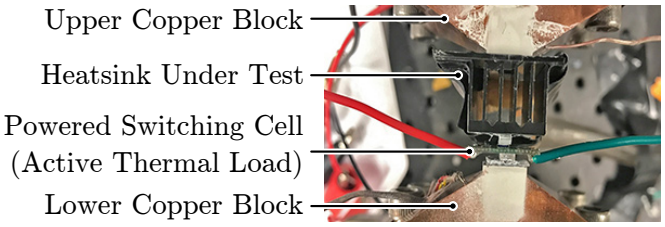


Fig. 9: Experimental setup for measuring heat sink thermal impedance with forced-air convection.

in the PCB, like that shown in Figure 8, were used to study the difference between junction and case temperature, which was measured at the side using a thermocouple. For all tests at varied power, the two temperature measurements were within 1 K, indicating that both a thermocouple measurement and IR micrograph taken from the side can provide a good indication of the device junction temperature in future studies.

### *B. System Level Thermal Performance*

After the TIM resistances were characterized, the overall per-cell thermal performance as a function of air velocity was evaluated using the setup shown in Figure 9 – a similar configuration to that in Figure 7. This again used the GaN device as the heat source, but also included the heat sink as well as the TIM, and a means to control the airflow through the heat sink. The results of this test, under 3 W thermal load provided by the transistor reverse conduction, are shown in Figure 11. Not only do they show good agreement with the simulation, but the air velocity required for a target of 5 K/W per switching cell suggests this performance is achievable for the full inverter with all twelve of the chosen fans.

To evaluate how well this proposed thermal management strategy extends to the full inverter, a converter motherboard was populated with all of the switching cells configured to perform as thermal loads as described above, forming a series-connected chain of thermal loads. This "thermal dummy" converter allowed for emulation of the losses of all of the switches in the converter without incurring the additional challenge of performing accurate temperature measurements in close proximity to high frequency, high voltage and high current traces during normal operation. Although it may be the

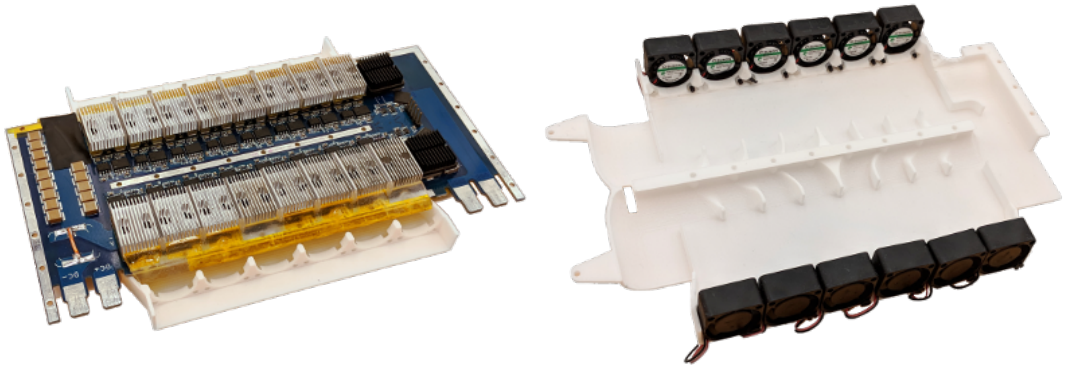

Fig. 10: Converter with modular heat sinking and laser-sintered plastic manifold with installed DC fans.

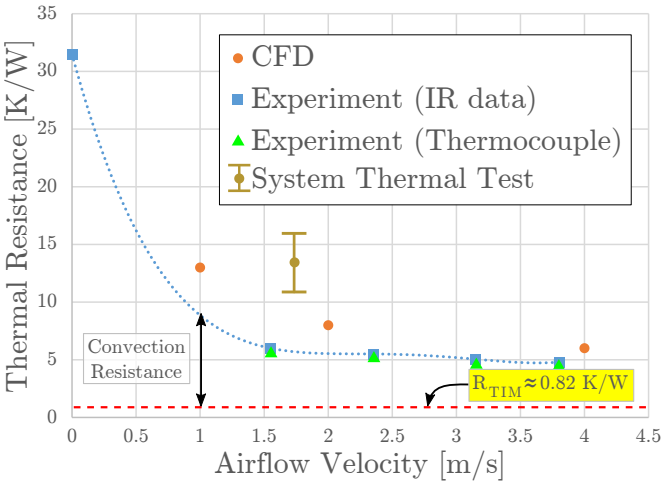


Fig. 11: Comparison of the simulated results experimental measurements of the system thermal performance.

case that these series-connected transistors unevenly share the total voltage drop, and therefore unevenly heat the individual devices, it is a convenient simplification for system performance study. For the system testing purposes, the full thermal management package, illustrated in Figure 10, was assembled around this ersatz converter. With the cooling fans running, the device temperatures across both sides of the board were simultaneously logged as the injected power was varied. These temperatures are plotted as the dashed lines in Figure 12 and vary between each location, but are not particularly associated with differences in any one region of the converter.

These temperatures can be correlated with the programmed dc power, air inlet velocity and air inlet temperature, to determine the thermal resistances seen by each device across the board. Like the temperature measurements, the thermal resistances also vary from location to location, with a mean value of 13.5 K/W and a standard deviation of 2.6 K/W, as indicated on Figure 11. This system thermal test data is plotted

TABLE II: Inverter bill of materials.

| Component | Part Number | Parameters |
|---|---|---|
| Gate driver | LM5114 | GaN |
| Gate resistors | | 22 Ω |
| GaN switches | EPC2034 | 200V, 7 mΩ |
| Output inductors | IHLP5050CE | 10 $\mu$F |
| Digital isolators | Si8423BB | |
| Power isolators | ADUM5210 | |
| Flying capacitors | 2220CC105KAZ2A | 1 $\mu$F, X7R |

alongside of the simulation and experimental results from the single switching cell tests above. While the variation in measured device temperatures and thermal resistances can be explained by the uneven power sharing of the series-connected transistors, converter variations or component mechanical defects, the error in the observed average thermal resistance compared to expectations from simulation will be a topic of future study.

### C. System Level Electrical Performance

Though the results above yielded a system thermal resistance higher than anticipated, testing a fully functional converter with modular heat sinking was nonetheless valuable to examine the practical challenges of the assembly process and validate the thermal performance under normal operation against the simulations and thermal experiments detailed above. This converter is based on the design of [8], with the bill of materials is listed in Table II. To correlate the thermal performance under inverter operation, a thermocouple was carefully affixed to one of the modular heat sinks and one of the flying capacitors; as the capacitors are not in thermal contact with the modular heat sink, there was concern that they may be inadequately cooled during high power operation.

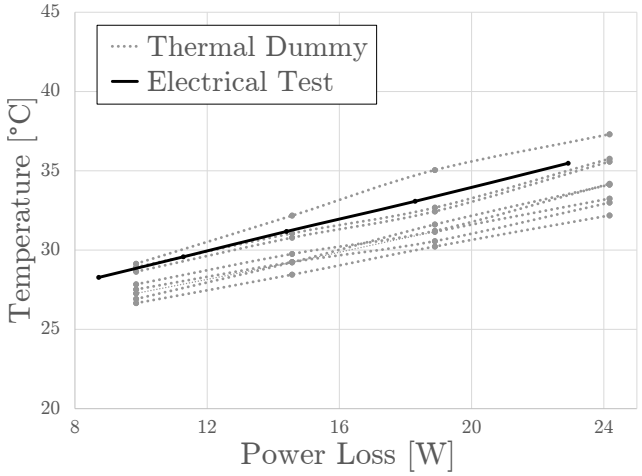


Fig. 12: Transistor temperatures for a given dissipation for both the thermal and electrical system tests.

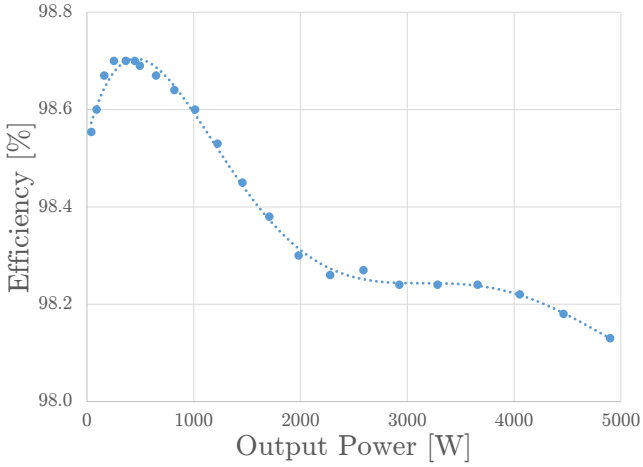


Fig. 13: System efficiency of the dual-interleaved 9-level FCML inverter with modular heat sinking.

However, the capacitor temperature closely tracked that of the heat sink indicating this may be a minor concern.

For simplicity, the converter was connected to a fixed 10 Ω load resistance and power was ramped up to 5 kW by increasing the dc supply voltage to the inverter. The measured heat sink temperature is plotted as the solid line in Figure 12 and, after accounting for difference in room temperatures between the two experiments, it can be see that there is reasonable agreement of between the two system temperatures. The system efficiency, measured using a Yokogawa WT3000E, is plotted in Figure 13.

## VI. Conclusion & Next Steps

A modular approach to heat sinking an interleaved, 9-level, flying capacitor multilevel converter was demonstrated. Experimental results on the thermal performance of individual switching cells, as well as simulated results on the entire system, indicated that higher thermal performance of the inverter could be achieved using this modular design – dropping overall thermal resistance to an experimentally measured 5 K/W for an airflow of 3 m/s. The converter performance, summarized in Table III, demonstrates high efficiency (with the cooling system power consumption included) and high power density, with very little auxiliary power required for the thermal management.

Moreover, this work demonstrated a methodology for designing, installing and validating modular heat sinks for chip-scale GaN transistors. Having illustrated the potential increase in performance using this approach, future work should address both static and cyclic stresses placed on the GaN devices by the rigid mate to the heat sink. Additionally, there is an opportunity to further improve the manufacturing process; this converter contained over 60 discrete fasteners whereas the next generation may attach the heat sinks to the manifold cover using springs for faster assembly of the converter module or employ snap-in fasteners over screws and bolts.

Finally, the next stage of development should emphasize analysis and simulation of the full converter airflow. In this study, heat sinks performed much better individually than when taken as an ensemble. Duct length between the fans and the heat sink intakes should be investigated as a cause for the lower than predicted flow rate, while low flow at the outlets will lead to an increase in temperature on the input and output filters for this design; infrared imagery suggests that the output inductors could possibly approach the manufacturer's rated temperature limits at higher power.

TABLE III: Peak experimental performance of the 9-level flying capacitor multilevel inverter with modular heat sink.

| Parameter | Value |
|---|---|
| Input Voltage | 670 $V_{dc}$ |
| Output Voltage | 233 $V_{RMS}$ |
| Peak Efficiency | 98.7 % |
| Peak Power | 5 kW |
| Cooling Power Supply | 9 W |
| Converter Mass | 350 g |
| Converter Volume | 275 $cm^3$ |
| Mass Power Density | 14.3 kW/kg |
| Volume Power Density | 9.5 kW/L |
| Switching Frequency | 120 kHz |
| Inductor Ripple Frequency | 960 kHz |

## VII. Acknowledgment

The authors gratefully acknowledge support for this work in part from the NASA Fixed Wing research program through NASA cooperative agreement NASA NNX14AL79A and from the Power Optimization of Electro-Thermal Systems (POETS) NSF Engineering Research Center.

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