Online Junction Temperature Extraction and Aging Detection of IGBT via Miller Plateau Width

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***Abstract*—The width of the Miller plateau during IGBT turn-off process is temperature sensitive and suitable for online junction temperature monitoring. In this paper, the online measurement system to detect this parameter is achieved at the gate driver side. The advantages of using the Miller plateau width for practical applications are discussed by comparison of three existing parameters. An accelerated aging test has been performed to determine the evolution of the Miller plateau width and validate the effectiveness of the method during the entire lifetime. Results show that as the bond-wire degradation develops and the junction temperature rises in the aging process, the Miller plateau width decreases, and it varies conversely with the on-state voltage. Therefore, the Miller plateau width is proposed as the indicator for online aging detection and remaining life prediction of IGBT.**

Keywords—IGBT; Semiconductor Reliability; Junction Temperature; Condition Monitoring; Failure Indicator

I. INTRODUCTION

In modern power systems scenario, semiconductor device reliability is a major concern [1]. According to an industry-based survey, power semiconductor devices are regarded as the weakest link of the system [2]. It is reported that more than 50% of their failures are thermal induced [3]. Therefore, the precise junction temperature (T_j) extraction of the power devices is essential for the aging estimation, health management and reliability assessment of the high power conversion systems.

Among the existing T_j extraction solutions, including the optical method, the physical contact method, and the electrical method, the thermo-sensitive electrical parameter (TSEP) method is a noninvasive and promising way to carry out fast, online T_j measurements on the fully packaged devices [4].

Several TSEPs have been developed in recent years. The on-state voltage ($V_{CE(on)}$) is a classic TSEP and has been widely used [5]. H. Kuhn and H. Luo proposed the turn-off delay time ($t_{d(off)}$) as a TSEP [6], [7], and its measurement circuit was designed by L. Li [8]. A. Bryant presented the method by using the derivative of the collector voltage (dv_{CE}/dt) at turn-off [9]. T_j can be extracted indirectly by detecting the change of the output harmonic. N. Baker proposed T_j estimation via the peak gate current [10]. Its measurement is possible to be integrated into the gate driver.

However, the application of TSEPs into field operation is notoriously limited. Further technological advances are demanded with respect to the following issues:

1) Accurate measurement of the electrical parameters is difficult. The temperature sensitivity of most TSEPs is relatively small, so the measurement requires complex circuitry. In addition, the circuit is costly, oversized and suffers from insulation problems.

2) Aging effect of TSEPs is not included in the literature. With the degradation of the device throughout the whole lifetime, external electrical parameters will also vary remarkably. To use them as TSEPs properly, a recalibration or compensation may be needed. Alternatively, there is a possibility that the variations of these TSEPs can be indicative of aging failure.

3) TSEP method has an inherent limitation that it only provides a "global" temperature. The estimated temperature is essentially an average temperature within the device. In some circumstances, it is the maximum temperature that matters.

The temperature sensitivity of the Miller plateau width (t_{GP}) at turn-off is first proposed in [11]. This TSEP can be measured at the gate driver level without interrupting normal operation, which is appropriate for real-time T_j extraction on site. In this paper, the dedicated *in situ* measurement system to recognize t_{GP} of the insulated gate bipolar transistor (IGBT) is designed and realized. The Miller plateau width is compared with three other existing dynamic TSEPs on the sensitivity, robustness, and circuit complexity, especially on the feasibility of online T_j extraction. Specific focus is given to the aging effect of using t_{GP} as a TSEP. An accelerated power cycling test is conducted to verify the long-term stability of the proposed method and observe the evolution of the parameter in the aging process.

II. THEORETICAL BASIS

A. Definition of t_{GP} During Turn-off Process

As shown in Fig. 1, the electrical model of IGBT consists of a PNP bipolar junction transistor (BJT), an N-channel metal oxide semiconductor field effect transistor (MOSFET), the gate resistance (R_G), and the parasitic capacitances (C_{GE}, C_{GC}, and C_{CE}).

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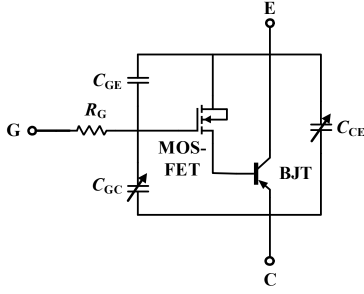


Fig. 1. IGBT electrical model

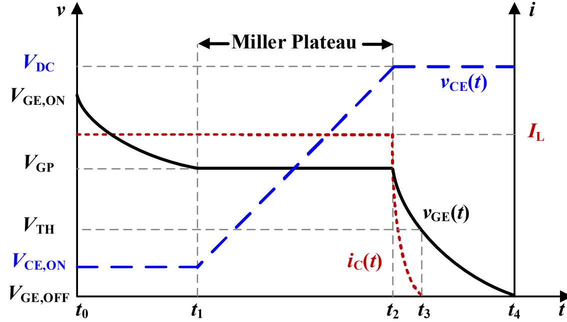


Fig. 2. IGBT turn-off transient behavior and the definition of t_{GP}

The theoretical transient characteristics of IGBT turn-off process are illustrated in Fig. 2. As a result of the voltage dependency of the gate-collector capacitance (Miller capacitance) C_{GC}, the gate discharging behavior of IGBT turn-off transient is varying. From t_1 to t_2, the collector voltage v_{CE} begins to increase. C_{GC} is decreasing, so the gate current discharges only C_{GC}. Consequently, the gate voltage (v_{GE}) remains constant, which forms the Miller plateau.

The width of the Miller plateau is defined as the duration between the first and second falling edge of v_{GE} during turn-off, with its expression given by [12]:

$$t_{GP}=\frac{R_G\cdot C_{GC,av}\cdot\left(V_{DC}-V_{CE(on)}\right)}{\frac{I_L}{g_m}+V_{TH}} \tag{1}$$

where $C_{GC,av}$ is the average value of C_{GC} during turn-off, V_{DC} is the DC-link voltage, g_m is the transconductance, and V_{TH} is the threshold voltage.

The physical mechanism of t_{GP} shift as a function of the temperature is well explained in [11]. Due to the temperature dependency of the carrier concentration and plasma distribution, C_{GC} increases at a higher temperature. Therefore, t_{GP} can be used as a TSEP for T_j extraction.

The proposed t_{GP} can be measured online by differentiating v_{GE} signal during turn-off transient. The output of the differentiator is proportional to the slope of v_{GE}, so two pulses are generated before and after the plateau phase. By counting the time interval between two pluses, t_{GP} is extracted.

B. *Aging Mechanisms for IGBT*

The IGBT devices are typically packaged in discretes or power modules that provide heat dissipation and protection. These packages consist of several different materials, each with a different coefficient of thermal expansion (CTE). When the device is subject to temperature swings, the mismatch in CTE causes thermomechanical stress at the interfaces, which would be worn out and finally break. Normally, the interconnection between the silicon semiconductor and the attached aluminum bond-wires is prone to fail in the thermal aging process.

Bond-wire degradation, including aluminum reconstruction and bond-wire liftoff, is known to increase the contact resistance, and increase $V_{CE(on)}$. In addition, it degrades the gate-oxide layer by reducing the effective gate area, which results in the reduction of C_{GC} [13]. Therefore, according to (1), the Miller plateau width would decrease as the bond-wire degrades during the aging process.

III. Experimental Setup and Online Measurement

Discrete IGBT device IHW20N120R3 (1200 V, 40 A, TO-247) is chosen as the device under test (DUT). A DC clamped inductive circuit is set up to perform the IGBT operation, as well as the accelerated aging test. The parameters of the main circuit are given in TABLE I. A measurement system connected to the gate driver is designed to extract the proposed Miller plateau width during turn-off. The measurement system consists of a v_{GE} signal processing circuit, a pulse time interval measurement circuit, a case temperature (T_c) measurement circuit, and their control board.

A. *Experimental Platform*

Fig. 3 shows the diagram and photo of the experimental platform. The construction of the platform is listed as follows:

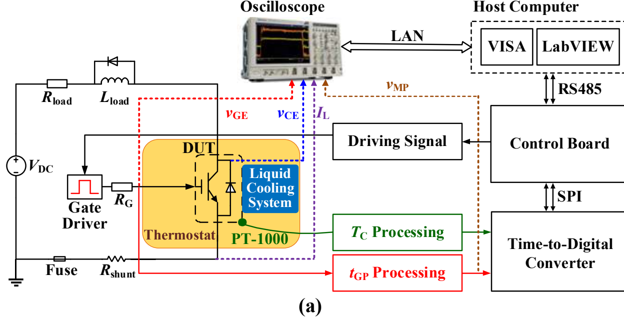
1) *High-power DC source:* Keysight N8951A.
2) *IGBT gate driver:* photocoupler TLP358H.
3) *Thermostat:* to stabilize the ambient temperature.
4) *Heat sink and liquid cooling system:* to adjust the desired heat dissipation condition.
5) *v_{GE} signal processing circuit:* the differentiator, the comparator, and the isolator.
6) *Pulse time interval measurement:* time-to-digital converter (TDC) TDC-GP21, time measuring mode 2 (90 ps accuracy, 4 ms range).
7) *T_c measurement:* TDC-GP21, temperature measuring mode, PT-1000 platinum resistor.
8) *Controller:* MSP430f5438A, to provide the control signal for the gate driver and measurement system, and acquire the time and temperature measuring results.
9) *Oscilloscope:* Tektronix DPO7104 (1 GHz bandwidth, 125 M memory depth, 4 channels) to collect the transient voltage and current waveforms.
10) *Host computer: to* communicate with the controller and the oscilloscope.

B. *v_{GE} Signal Processing Circuit*

The signal processing circuit to pre-process v_{GE} waveform during turn-off is the key to realize t_{GP} extraction. The circuit

TABLE I. PARAMETERS OF TEST CIRCUIT

Parameters	Value
Load inductance L_{load}	100 μH
Load resistance R_{load}	1 Ω
Gate voltage $V_{GE(on)}/V_{GE(off)}$	15 V/0 V
Gate resistance R_G	10 Ω



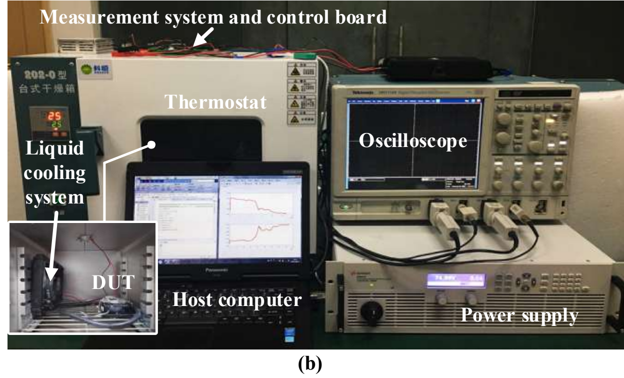


Fig. 3. Experimental setup and measurement system: (a) schematic diagram, and (b) photo.

is designed to generate two pulses from two negative edges of v_{GE} signal.

The circuit consists of 3 parts, namely the differentiator, the comparator, and the isolator. The differentiator uses the resistance-capacitance network to achieve the differential transformation. By comparing to a constant negative reference voltage (VBIAS=1.5 V), the comparator converts the differentiator output to logical pluses. Details of the circuit are illustrated in Fig. 4.

C. Miller Plateau Width Measurement

The time interval between the two logical pluses transformed by the v_{GE} processing circuit, which refers to the proposed t_{GP}, are then counted by the TDC chip (TDC-GP21). The circuit configuration of TDC is illustrated in Fig. 5.

The operation principle of the TDC chip is that once its START pin receives the high-level signal from the controller, TDC counts the time interval between the rising edges (or falling edges) of the pulses input to its STOP channel. Therefore, the START signal is provided right after when the IGBT turn-off signal is sent. Two pluses from the v_{GE} processing circuit is put into the STOP channel. In this case, the rising edges of two pluses serve as the triggers for TDC. TDC measures the time interval between the two triggers. Measuring results are stored in the output register, and transferred to the controller via SPI interface, and finally to the host computer via RS485 communication protocol.

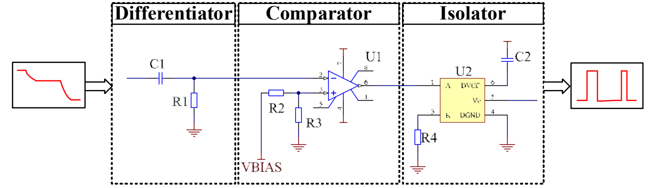


Fig. 4. Configuration of the t_{GP} signal processing circuit.

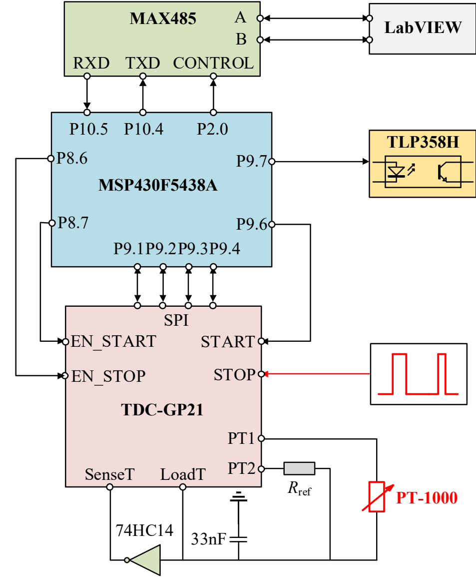


Fig. 5. Configuration of the t_{GP} and T_c measurement circuit.

Along with the v_{GE} processing circuit, the construction of t_{GP} measurement system is compact and cost-effective. In particular, it can be implemented into the gate driver and does not cause any disruption to normal operation, which is favorable for field practice.

D. Case Temperature Measurement

T_c measurement is also performed by TDC-GP21, as shown in Fig. 5. The 33 nF capacitor discharges the reference resistor (R_{ref}) and PT-1000 resistor respectively. TDC counts and compares two discharge time, so the resistance of PT-1000 is obtained. Automatically, the resistance is measured and stored in the output register. The controller can read the results and translate it to T_c by querying the pre-defined look-up table.

IV. Junction Temperature Extraction

To evaluate the strengths and weaknesses of t_{GP} as a TSEP, it was compared with three existing dynamic TSEPs, including $V_{CE(on)}$, $t_{d(off)}$, and dv_{CE}/dt, in terms of sensitivity, robustness, integration, and feasibility for online estimation.

In this paper, t_{GP} is measured by the designed circuit, whereas the other three TSEPs are recorded by the oscilloscope. $V_{CE(on)}$ is measured just before the IGBT turn-off signal is sent. $t_{d(off)}$ is calculated as the period between v_{GE} falls to 90% of its maximum value and v_{CE} rises to 90% V_{DC}. dv_{CE}/dt is extracted when $v_{CE} = V_{DC}$.

The application of the TSEP method for T_j measurement can be divided into two steps. The first step is calibration which determines the correlations between TSEPs and T_j, and creates the fitted calibration curves. The second step is extraction which translates the measured TSEPs by calibration curves into T_j in operation.

A. Output of the Signal Processing Circuit

The output of the v_{GE} signal processing circuit is shown in Fig. 6. Two pulses are generated from two falling edges of v_{GE} signal. The first pulse (trigger 1) is generated before the Miller plateau, and the second pulse (trigger 2) is generated after the Miller plateau. These two pulses are then fed to the TDC, which counts the time interval between trigger 1 and trigger 2 to determine t_{GP}. Multiple TDC measurement experiments are conducted, and the maximum standard deviation of the measuring results is less than 10 ns.

Note that the measured time interval by TDC is not exactly the required Miller plateau width, but its variation can represent the variation of the Miller plateau width.

B. Calibration of TSEPs

In the calibration step, because a gate pulse of 4 μs is adopted to minimize self-heating effect, T_j is thought the same as T_c and is controlled up to 120 °C by the thermostat, In addition, all of the four TSEPs have dependencies of the load current. Thus, load current in the calibration step is changed from 10 A to 40 A.

Fig. 7 shows the measured values and linear fitted curves from the TSEPs calibration. It can be observed that all four TSEPs have good linearity with the temperature. As the temperature increases, t_{GP} and $t_{d(off)}$ increases, together with $V_{CE(on)}$ and dv_{CE}/dt decreases. As the load current increases, the sensitivity of t_{GP}, $V_{CE(on)}$ and $t_{d(off)}$ varies considerably while the sensitivity of dv_{CE}/dt seems to be not affected. At 30 A, temperature sensitivity is 0.13 ns/°C, 6.930 mV/°C, 0.76 ns/°C and 2.481 V/(μs·°C) for four TSEPs, respectively. Note that the sub-nanosecond variation in t_{GP} is impossible for the measurement circuit to respond, so it is needed to raise the sensitivity of t_{GP}.

C. Method to Raise the Temperature Sensitivity

The approach for raising the temperature sensitivity of t_{GP} is simply extending the scale of the turn-off process by increasing R_G. According to (1), the value of t_{GP} is in direct pro-

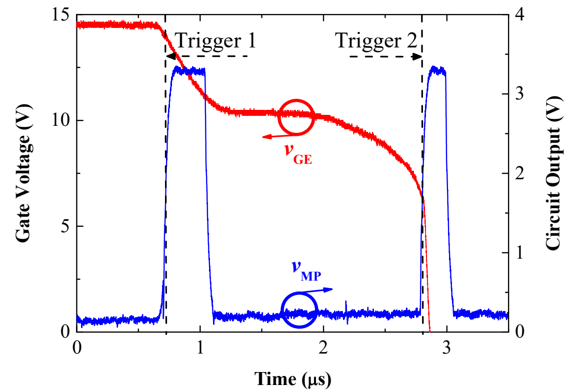


Fig. 6. Output waveform of the t_{GP} signal processing circuit.

portion to R_G. Since T_j has little effect on R_G, the sensitivity is thought to be positively correlated with R_G.

Fig. 8 shows the TSEPs calibration results using different gate resistance. By increasing R_G from 10 Ω to 100 Ω, the temperature sensitivity at 30 A of t_{GP} goes up from 0.13 ns/°C to 1.78 ns/°C, which is acceptable for the signal processing circuit and the TDC chip. Therefore, a 100 Ω R_G is selected in the rest of this paper. Therefore, by compromising the switching speed/frequency, a precise t_{GP} measurement can be achieved.

D. Online Junction Temperature Extraction

In the temperature extraction step, the TSEP method is compared to the thermistor measurement. Various current duration conditions (up to 6 s) of 30 A are adapted to introduce T_j up to 120 °C by self-heating. With the calibration curves, four TSEPs are converted to T_j, respectively.

The final results are shown in Fig. 9. It can be seen that the estimated T_j using the TSEP method follows the same trend as T_c measured by PT-1000 thermistor. Obviously, T_j is about 5 °C higher than T_c, as expected. The temperature difference is given by the power losses in the chip and the thermal path from the chip to the case.

The comparison is made between TSEP estimation and the dashed line (T_c plus 5 °C), as the reference of the actual junction temperature. The deviation occurs at some points for all TSEPs. t_{GP} has the lowest deviation, whereas $V_{CE(on)}$ and $t_{d(off)}$ have larger deviation. For dv_{CE}/dt, there is a large discrepancy at below 40 °C. The maximum standard deviation of four TSEPs is less than 10 °C. Generally, T_j extracted from TSEPs measurement agrees well with that T_c measured by the thermistor, showing the effectiveness of the TSEP technique.

Finally, the evaluation of 4 TSEPs is summarized in TABLE II.

To normalize temperature sensitivity of different TSEPs, the relative temperature sensitivity factor is defined as the ratio of the temperature sensitivity and the maximum measured value [8]. The results show that $t_{d(off)}$ has the highest sensitivity, whereas t_{GP} and $V_{CE(on)}$ have low sensitivity.

Robustness represents the degree of dependencies from the

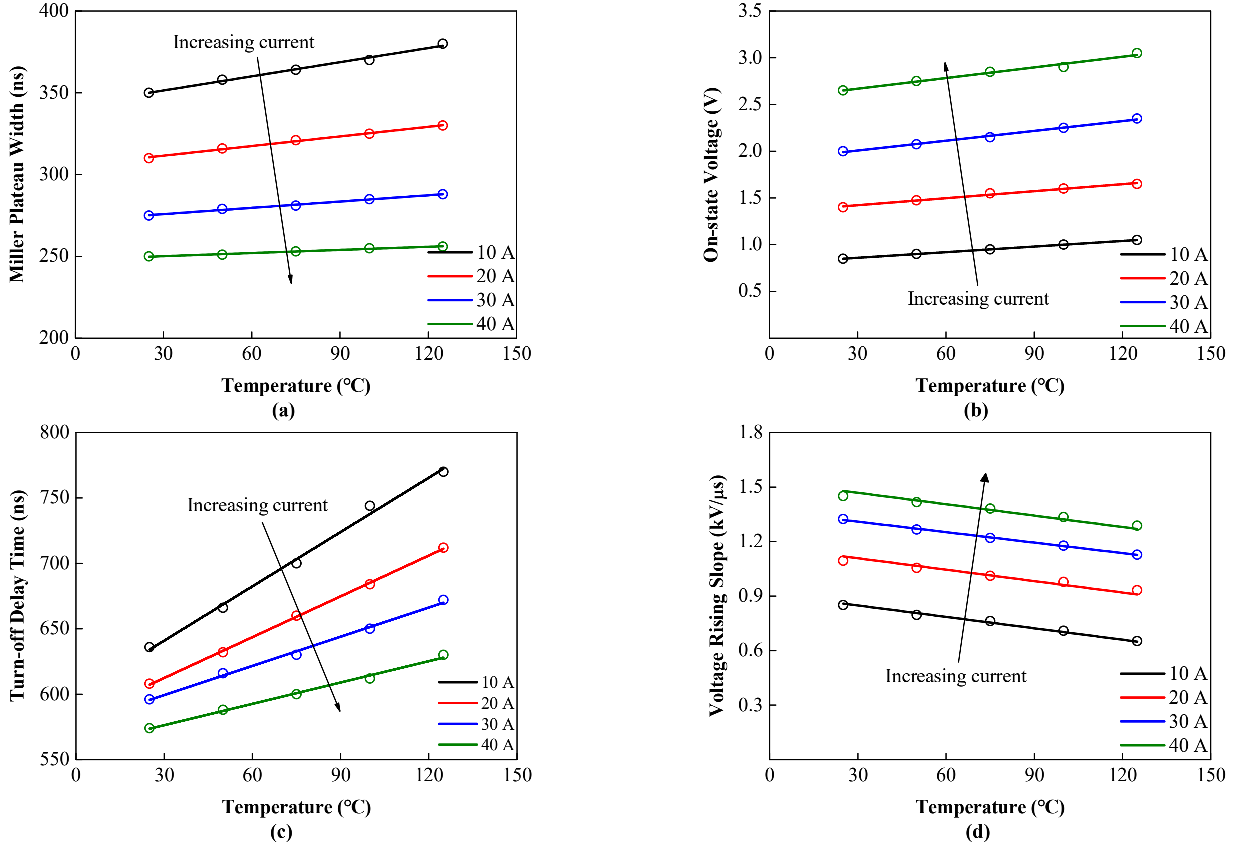


Fig. 7. Calibration curves of 4 TSEPs: (a) t_{GP}, (b) $V_{CE(on)}$, (c) $t_{d(off)}$, and (d) dv_{CE}/dt.

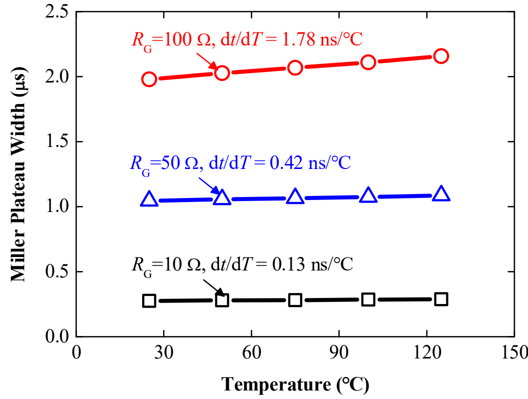


Fig. 8. t_{GP} calibration curves with various gate resistances.

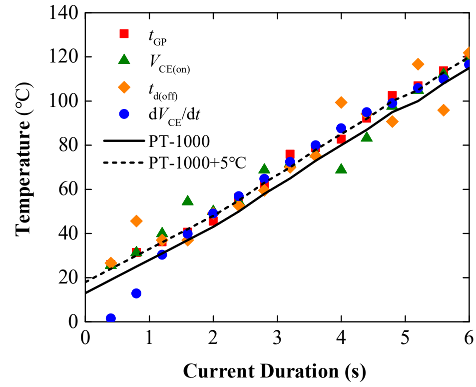


Fig. 9. Online junction temperature estimation by TSEPs and case temperature measurement by PT-1000.

TABLE II. EVALUATION OF FOUR TSEPS

	t_{GP}	$V_{CE(on)}$	$t_{d(off)}$	dv_{CE}/dt
Sensitivity	0.08%/°C	0.07%/°C	0.46%/°C	0.19%/°C
Robustness	Low	High	Low	Low
Integration	Simple	Possible	Possible	Complicated
Online Estimation	Feasible	Possible	Difficult	Difficult

parameters except for T_j on TSEPs. $V_{CE(on)}$ varies with the gate voltage and collector current, whereas t_{GP}, $t_{d(off)}$, and dv_{CE}/dt have dependencies on other operating conditions, including the DC-link voltage, gate resistance, circuit parasitic, etc. The calibration and information of these parameters are needed regarding the T_j extraction by TSEP.

Integration stands for the practicality of the measurement circuit integrated into the system. As shown in Section III, t_{GP} measurement circuit is not complicated. The real-time

measurement circuits for $V_{CE(on)}$ and $t_{d(off)}$ have also been designed and tested [3], [8]. dv_{CE}/dt is difficult to measure directly, and it is proposed to be extracted by detecting the change of the output harmonic.

All of the four TSEPs can be aquired during IGBT operation. However, $V_{CE(on)}$, $t_{d(off)}$, and dv_{CE}/dt have to be measured at the main circuit, which may introduce isolation problems. As a contrast, the t_{GP} measurement is on the driver side; thus it seems to be more feasible for real-time online monitoring, especially in high-voltage, high-power applications.

V. AGING EFFECT

A. Accelerated Aging Test

As discussed previously, t_{GP}-based TSEP method is promising for online T_j extraction. In order to determine variations of the Miller plateau width and verify the effectiveness of the method during the entire lifetime, an accelerated degradation test is carried out on the same platform in Fig. 3. Power cycling is the most common thermal acceleration tests used in assessing the reliability of power devices and is used to simulate full life experiment of DUT in this paper. The control strategy is the fixed turn-on and turn-off time, which is regarded as the most severe strategy [14]. A degradation of the device will have an immediate impact on the resulting temperature swing with no compensation.

In the literature, end-of-life criterion is normally defined as 5% or 10% increase of $V_{CE(on)}$ from its initial value [3]. Accordingly, the 10% $V_{CE(on)}$ criterion is adopted in the accelerated degradation test. The measurement of $V_{CE(on)}$ is performed by a commercial voltage measurement module with an accuracy of 0.02%.

DUT switches 30 A current in 5 Hz, and 50 % duty cycle. As a result of the short turn-on time, T_c reaches an equilibrium of 120 °C at the beginning of the aging test. The junction temperature swing, which is calculated by the variations of $V_{CE(on)}$, is less than 40 °C. t_{GP} is measured during the turn-on transient process, and $V_{CE(on)}$ is measured 3 ms before the turn-off of each cycle. t_{GP}, T_c, and $V_{CE(on)}$ results are collected per second.

B. Experimental Results

The power cycling test lasts for 806k cycles (44 hours' test period) before $V_{CE(on)}$ increases 10%. T_j results by t_{GP} and T_c results by PT-1000 during the test are illustrated in Fig. 10.

Before 236k cycles, T_j extraction by t_{GP} works well. The extracted T_j has the same varying trend with T_c. T_j is about 5 °C higher than the T_c, same as results in the experiment of Section IV. After 236k cycles, the temperature difference between t_{GP} extraction and PT-1000 measurement gradually decreases and becomes less than 5 °C, so the extracted T_j is below its actual value, indicating t_{GP} and thus DUT being deteriorated.

Zoomed graphs of the period before and after 236k cycles are illustrated to identify the difference between the pre-aged and post-aged devices. In Fig. 10(b), before 236k cycles, T_j by

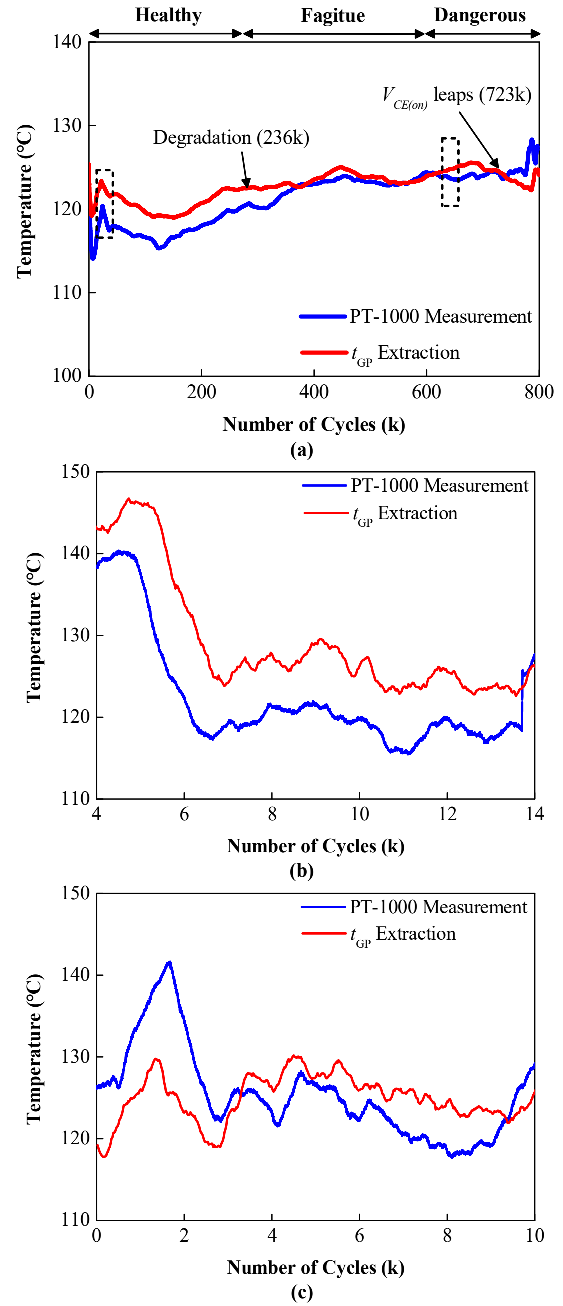


Fig. 10. Extracted junction temperature and measured case temperature variations during the aging test: (a) whole lifetime, (b) zoom of the healthy stage, and (c) zoom of the dangerous stage.

t_{GP} extraction rises and drops in pace with T_c, and the temperature difference is almost constant. However, in Fig. 10(c), after 236k cycles, the matchup relation is uncertain, and the temperature difference is much smaller. Dramatically, at some cycles, the extracted T_j is even lower than the measured T_c, which is obviously unrealistic. Therefore, the proposed TSEP t_{GP} suffers from degradation with aging. In this case, to use the Miller plateau width as a TSEP properly, a recalibration is necessary after 236k cycles.

A more direct explanation is given by analyzing the evolution of t_{GP} and $V_{CE(on)}$, as depicted in Fig. 11. Note that t_{GP} goes an opposite direction of $V_{CE(on)}$ in the whole aging process. As the power cycling experiment proceeds, $V_{CE(on)}$ constantly increases from 3.11 V to 3.43 V, whereas t_{GP} decreased from 2.055 μs to 1.962 μs simultaneously. DUT finally failed after 806k cycles, and shortly before end-of-life (723k cycle), the steep upper step of $V_{CE(on)}$ and the steep lower step of t_{GP} appear, indicating the first failure in the bond-wire.

Fig. 12 shows the turn-off v_{GE} waveforms at different stages of the aging process. Apparently, t_{GP} reduces during the aging process, and the final time reduction is 93 ns, which is practicable for the measuring circuit and the TDC chip.

Therefore, by monitoring the variations of $V_{CE(on)}$ and t_{GP}, the health condition of the DUT can be divided into three stages in the whole period. In the test presented in this paper, the first 236k cycles are defined as the "healthy" stage, the period between 236k and 723k cycles are defined as the "fatigue" stage, and the period after 723k cycles are defined as the "dangerous" stage.

C. Discussion on Aging Detection by Miller Plateau Width

As explained in Section II, in IGBT aging process, the bond-wire is the "weakest link in the chain". Bond-wire degradation and its corresponding gate oxide degradation contribute to the increase of $V_{CE(on)}$ and the decrease of t_{GP} observed during the power cycling test.

As a matter of fact, with the increase of $V_{CE(on)}$, the power loss on the device, and thereby T_j also increases. Because $V_{CE(on)}$ has a dependency on T_j, the variation of $V_{CE(on)}$ is divided into two separate parts: the thermal part, and the degradation part. Both parts contribute to the increment of $V_{CE(on)}$.

Similarly, the variation of t_{GP} comprises the thermal part and the degradation part, too. The difference is that these two parts have a contrary effect on t_{GP}. t_{GP} increases as the T_j rises, whereas t_{GP} decreases with the bond-wire degradation develops. Therefore, the only effect responsible for the reduction of the Miller plateau width in the aging test is the bond-wire degradation.

Since $V_{CE(on)}$ is a well-accepted indicator for IGBT condition monitoring, it is shown in the above results that the proposed parameter, i.e., the Miller plateau width, can be employed in a similar way as the new precursor for aging detection of IGBT, as well as for remaining life prediction.

VI. POST-FAILURE ANALYSIS

A post-aged device is examined to present the physics-of-failure underlying the decrease of the Miller plateau width.

Fig. 13 shows the scanning acoustic microscopy (SAM) graphs of the IGBTs. It can be observed that the interconnection of the die area in the post-aged device is brighter than that of the pre-aged device, indicating the degradation of the bond wire and emitter metallization.

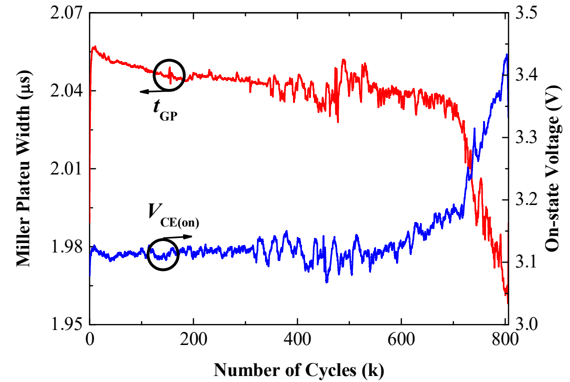


Fig. 11. t_{GP} and $V_{CE(on)}$ variations during aging test.

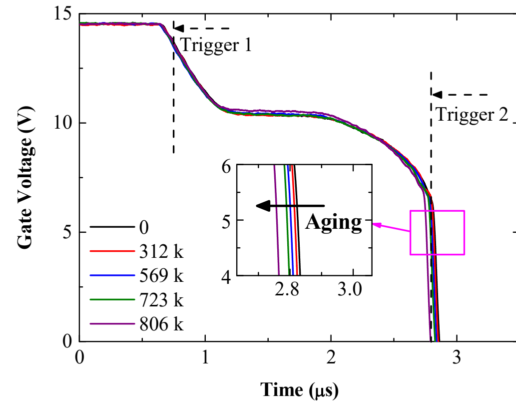


Fig. 12. Gate voltage waveforms at various aging stages.

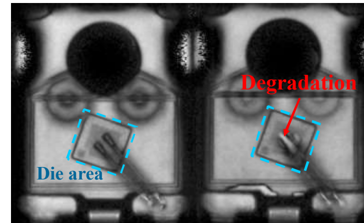
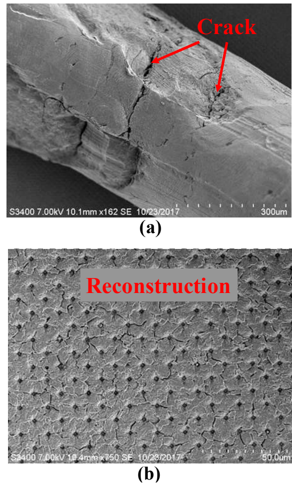


Fig. 13. SAM graphs of IGBTs. (left: pre-aged, right: post-aged)

Fig. 14 shows the scanning electron microscopy (SEM) graph of DUT. In Fig. 14(a), cracks of the bond wire are formed, and in Fig. 14(b), metallization reconstruction is visible. As a result, the effective gate area of the aged device is reduced, leading to a decreased Miller capacitance and thereby a decreased Miller plateau width.

Fig. 15 shows the SEM graph of the cross-sectioned DUT. Note that no visible degradation of the solder layer appears in the aged devices, so the thermal path (thermal resistance) from junction to case of the DUT remain unchanged. As a result, T_j



(a)

(b)

Fig. 14. SEM graphs of the (a) de-capsulated DUT, and (b) zoom of the emitter metallization area.

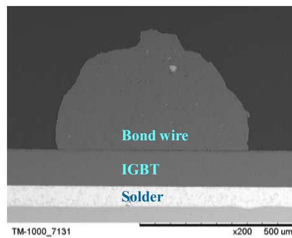


Fig. 15. SEM micrographs of the cross-sectioned DUT.

increases as $V_{CE(on)}$ increases during aging test. As discussed in Section V, the decreased Miller plateau width is the outcome of the bond-wire degradation.

VII. Conclusion

In this paper, the online junction temperature extraction system of IGBT is realized, by applying the Miller plateau width as a TSEP. Comparing to 3 other TSEPs, the advantages of the Miller plateau width are its implementation at the gate driver side and its simplicity of the measurement circuit. A power cycling test has been performed to observe t_{GP} and $V_{CE(on)}$ variations during entire life. Results show that t_{GP} has an opposite trend of $V_{CE(on)}$ in the aging process. The degradation mode determined by the post-failure analysis is the bond-wire fatigue, indicating the feasibility of using the Miller plateau width as the new condition monitoring parameter.

More IGBT devices of different technologies should be tested to determine the end-of-life criterion indicated by the Miller plateau width. In addition, the proposed method can be applied to all types of MOS-gated device, which is a potential technique for online junction temperature extraction and condition monitoring of silicon carbide (SiC) power MOSFET.

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References

[1] H. Oh, B. Han, P. Mccluskey, C. Han, and B. D. Youn, “Physics-of-Failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: a review,” IEEE Trans. Power Electron., vol. 30, no. 5, pp. 2413–2426, 2015.

[2] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, “An industry-based survey of reliability in power electronic converters,” IEEE Trans. Ind. Appl., vol. 47, no. 3, pp. 1441–1451, 2011.

[3] U. Choi, F. Blaabjerg, and S. Jørgensen, “Study on effect of junction temperature swing duration on lifetime of transfer molded power IGBT modules,” IEEE Trans. Power Electron., no. January, 2017.

[4] N. Baker, M. Liserre, L. Dupont, and Y. Avenas, “Improved reliability of power modules: a review of online junction temperature measurement methods,” IEEE Ind. Electron. Mag., vol. 8, no. 3, pp. 17–27, 2014.

[5] Y. Avenas, L. Dupont, and Z. Khatir, “Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters—a Review,” IEEE Trans. Power Electron., vol. 27, no. 6, pp. 3081–3092, 2012.

[6] H. Kuhn and A. Mertens, “On-line junction temperature measurement of IGBTs based on temperature sensitive electrical parameters,” in 2009 13th European Conference on Power Electronics and Applications, pp. 1-10, 2009.

[7] H. Luo, Y. Chen, P. Sun, W. Li, and X. He, “Junction temperature extraction approach with turn-off delay time for high-voltage high-power IGBT modules,” IEEE Transactions on Power Electronics, vol. 31, no. 7, pp. 5122-5132, 2016.

[8] L. Li et al., “A turn-off delay time measurement and junction temperature estimation method for IGBT,” in 2017 IEEE Appl. Power Electron. Conf. Expo., pp. 2290–2296, 2017.

[9] A. Bryant et al., “Investigation into IGBT dV / dt during turn-off and its temperature dependence,” IEEE Trans. Power Electron., vol. 26, no. 10, pp. 3019–3031, 2011.

[10] N. Baker, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, “IGBT junction temperature measurement via peak gate current,” IEEE Trans. Power Electron., vol. 31, no. 5, pp. 3784–3793, 2016.

[11] V. K. Sundaramoorthy et al., “A study on IGBT junction temperature (Tj) online estimation using gate-emitter voltage (Vge) at turn-off,” Microelectron. Reliab., vol. 54, no. 11, pp. 2423–2431, 2014.

[12] B. Baliga, Fundamentals of Power Semiconductor Devices. New York: Springer Verlag, 2008, pp.440-443.

[13] K. Wei, M. Du, L. Xie, and J. Li, “Study of bonding wire failure effects on external measurable signals of IGBT module,” IEEE Trans. Device Mater. Reliab., vol. 14, no. 1, pp. 83–89, 2014.

[14] U. Scheuermann and S. Schuler, “Power cycling results for different control strategies,” Microelectron. Reliab., vol. 50, no. 9–11, pp. 1203–1209, 2010.

[15] B. Tian, W. Qiao, Z. Wang, T. Gachovska and J. L. Hudgins, "Monitoring IGBT's health condition via junction temperature variations," in 2014 IEEE Appl. Power Electron. Conf. Expo., pp. 2550-2555, 2014.

[16] S. Dusmez, S. H. Ali, M. Heydarzadeh, A. S. Kamath, H. Duran, and B. Akin, “Aging precursor identification and lifetime estimation for thermally aged discrete package silicon power switches,” IEEE Trans. Ind. Appl., vol. 53, no. 1, pp. 251–260, 2017.

[17] H. Niu and R. D. Lorenz, “Evaluating different implementations of online junction temperature sensing for switching power semiconductors,” IEEE Trans. Ind. Appl., vol. 53, no. 1, pp. 391–401, 2017.