Active Power Cycling and Condition Monitoring of IGBT Power Modules using Reflectometry

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Abstract— High thermal and electrical stress, over a period of time tends to deteriorate the health of power electronic switches. Being a key element in any high-power converter systems, power switches such as Insulated Gate Bipolar Junction Transistors (IGBTs) and Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are constantly monitored to predict when and how they might fail. A huge fraction of research efforts involves the study of power electronic device reliability and development of novel techniques with higher accuracy in health estimation of such devices. Through this paper, a new method for online condition monitoring of IGBTs and IGBT modules using spread spectrum time domain reflectometry (SSTDR) has been proposed. Unlike traditional methods, this research work concentrates at the gate terminals (low voltage) of the device instead of looking at the collector side. The IGBT collector-emitter ON voltage or V_{CEON} was chosen as the failure precursor parameter as the reference, and the auto-correlated magnitudes of the SSTDR signal for the new and the aged IGBTs were plotted and compared.

Keywords— Condition monitoring, IGBT, SSTDR, power cycling.

I. INTRODUCTION

There has been a substantial growth in the use of power electronic switching devices in recent years. The most routinely used power switches are IGBTs and MOSFETs. IGBTs are typically used in various vehicular applications, variable-frequency drives (VFDs), electronic ballasts and commercial cooling units [1]. Larger IGBTs (1200V, 900A) are used in large low-voltage industrial motor drives, vehicular propulsion systems and large photovoltaic (PV) inverters [1]. Like any other switch, IGBTs go through aging and failure, bringing down the system efficiency and often causing an entire system failure. Therefore, monitoring the state-of-health of IGBTs can be profitable in the long-run by ensuring higher system availability.

For wider applications, IGBTs are manufactured in modules, and an IGBT module can be further classified either as a press-pack or a wire-wound packaging type. Single IGBT devices are connected by direct press-pack contacts in a press-pack module, which provides higher reliability, higher power density and better cooling capabilities than a traditional wire-wound IGBT module [2]. IGBT failures as like any other power electronic device failures can be categorized into package-related (extrinsic) failures and chip-related (intrinsic) failures [3]. An IGBT module can be aged under practical conditions, and its physical and electrical parameters can be monitored, analyzed and compared to predict its level of aging. The most frequently monitored failure precursor parameters of an IGBT are transistor case temperature, collector-emitter current, threshold voltage, collector-emitter ON voltage and steady-state collector voltage [1][4].

The health of an IGBT module can be monitored through accelerated power cycling or accelerated thermal cycling tests. Various methods to measure the V_{CEON} have been proposed in [5-10], each having their advantages and limitations. In [6], a reed relay has been used to connect an ADC to the IGBT to measure its V_{CEON}, which in comparison is not fast enough for measurements during a live converter monitoring. Measurement time is a key factor for condition monitoring of power electronic devices, and this is the one which accounts for an error in test data analysis in most cases. In [7], the authors have proposed a method to measure V_{CEON} using a Zener diode. Due to long settling time, this method is not convenient for applications having switching frequency in the range of several kHz.

In [8], the authors proposed connecting a MOSFET in parallel with the device under test (DUT). This method is only good enough as the health of the MOSFET used, as any kind of failure to the MOSFET can lead to short-circuit failure of entire converter. A circuit based on a traditional de-saturation protection circuit and having two diodes has been proposed in [9]. Although this method is suitable for V_{CEON} measurement during live converter operation, yet a slight difference in either of the diodes parameters can give a measurement error.

In this paper, a condition monitoring method of IGBT modules using reflectometry is proposed. In addition to that, the active power cycling method used for the tests has been elaborately explained throughout this paper. A 1200V, 450A Si IGBT module (FF450R12ME4) was used as the DUT, and test results were obtained to support the feasibility of the proposed method.

II. SSTDR TECHNIQUE: AN EQUIVALENT IMPEDANCE APPROACH

Reflectometry needs no introduction and has been used for many years for various fault detection and health estimation applications. From locating faults on electrical wirings to measuring the electrical characteristics of various materials, reflectometry has found a wide range of applications in day to

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day life. Reflectometry could be one of the best approaches to detect open circuit and short circuit faults, but cannot be fully trusted while detecting soft faults (such as insulation failure, etc.) [10]. There are several reflectometry methods being used, and some of the most widely used methods are Frequency Domain Reflectometry (FDR), Sequence Time Domain Reflectometry (STDR), Spread Spectrum Time Domain Reflectometry (SSTDR).

This paper uses the SSTDR technique to monitor the impedance variation at the gate-emitter interface as well as at the collector-emitter junction, and therefore, the V_{CEON} of the IGBT module. Being less immune to noise and interference, SSTDR systems are advantageous than any other reflectometry methods for in-situ condition monitoring of IGBT modules. By expanding the effective bandwidth of the system with the use of longer PN codes, its accuracy and precision in both space and time can be further increased [11-13]. Similar to any other reflectometry method, SSTDR magnitude or the reflection coefficient Γ can be expressed as:

$$\Gamma = \frac{V_{reflected}}{V_{incident}} = \frac{Z_L - Z_o}{Z_L + Z_o} \qquad (1)$$

where, Z_O refers to the characteristic impedance of the line, and Z_L is the impedance of the discontinuity [3]. Using this same principle, the aging inside the IGBT module can be identified. The DUT selected for this experiment is a dual pack module. It has two IGBTs connected in series by means of 48 bond wires. These bond wires are connected in such a fashion that the module can be considered as a complex transmission network. With degradation, the ON-state resistance or R_{ON} of each device will increase over the course of operation and will be different than that of the healthy device. This reflection coefficient Γ will give the impression of this difference between the two R_{ON} values when measured by SSTDR hardware, and a non-zero value between the two readings will illustrate the aging of the device.

III. ACTIVE POWER CYCLING OF IGBT

The DUT, shown in Fig 1, was placed in an accelerated aging station (shown in Fig 2) to apply electrical and thermal stress. The simultaneous stress was achieved by stopping the coolant flow during the ON-state (electrical) of the DUT. This active power cycling technique helps to induce aging in the device in a more efficient way than stressing it either electrically or thermally. A 600A Lambda-TDK (EMS 7.5-600-2-D-RSTL) power supply was used to push current through the device, and 313A DC current was supplied between the collector and emitter terminals during this aging process. The number of cycle was counted based on the temperature swing of the device. The swing in temperature was 100°C (ΔT) starting from 50°C and ending at 150°C of case temperature. A k-type thermocouple was used to monitor the temperature.

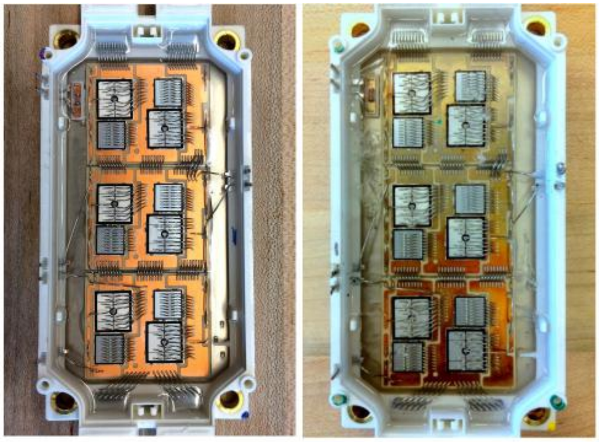


Fig 1: Infineon IGBT power module (FF450R12ME4)

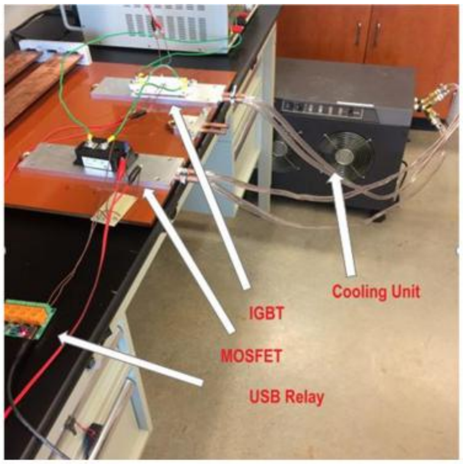


Fig 2: Active power cycling setup

A Lab-Jack T7-Pro DAQ was used to record V_{CEON}, collector current (I_C) and case temperature (T). Once the temperature reached 150°C, the power supply automatically stopped sending power to the device, and the coolant flow was activated. Similarly, when the device's case temperature went down to 50°C, the power supply started pushing current to the collector, and the coolant pump stopped the coolant flow. This control of the power supply was incorporated by using a power MOSFET in series with the DUT at the collector side, and this switch was turned ON and OFF in order to activate or deactivate the power supply. In order to make the cooling efficient, a heat sink was attached underneath the IGBT module and Ethylene-glycol was used as the cooling agent.

IV. EXPERIMENTAL SETUP AND TEST RESULTS

The SSTDR signal was applied at both the gates of top and bottom IGBTs, and the DAQ was recording the V_{CEON} data (plotted and shown in Fig 4) simultaneously. Fig 3 illustrates the simplified Infineon module and shows the SSTDR contact points: G1, E1 (1b), G2, and E2 (2b). The device was aged at two different levels, and data obtained at each level was compared with the measurements consistent to the device with no aging. The SSTDR data was recorded for frequencies 6MHz, 12MHz, and 48MHz for current levels of 0A, 25A, and 50A.

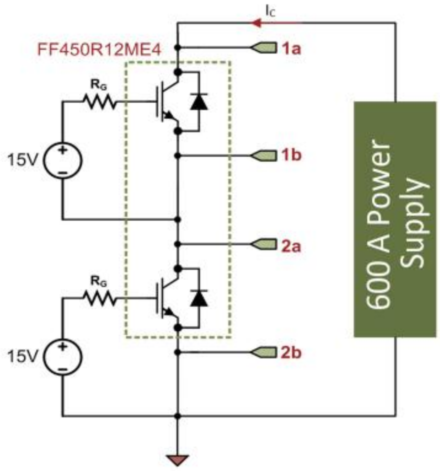


Fig 3: Simplified SSTDR test schematic

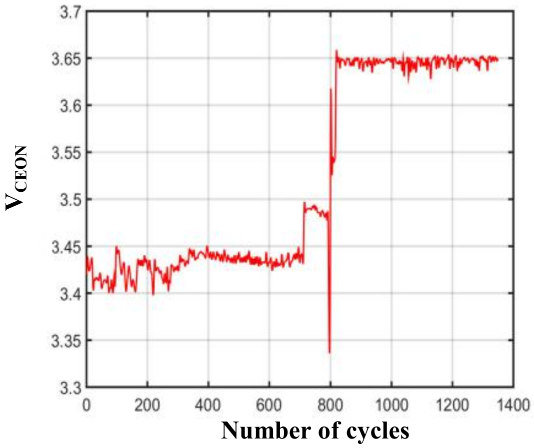


Fig 4: V_{CEON} vs number of thermal cycles

From Fig 4, it is apparent that V_{CEON} keeps increasing with aging and gives a sharp spike at around 800 cycles and holds that value. At this point the IGBT is considered as failed. This pattern of IGBT's V_{CEON} is very common and can be found in condition monitoring literatures [5][14]. According to equation 1, it is expected that the auto-correlated amplitude of SSTDR will produce a lower magnitude when the IGBT goes through aging indicating higher ON-resistance. Hence with the increase in R_{ON} value the equivalent impedance, Z_L for the SSTDR hardware will also increase when seen from the gate terminals. Fig 5 shows the auto-correlated amplitude of SSTDR signal recorded between the gate and emitter terminals of the top and bottom IGBT respectively. The zoomed version of this plot (shown in Fig 6) at their maximum amplitude clearly shows that there is a significant distinction between the healthy and aged device. As the level of aging increases i.e., R_{ON} increases, the amplitude of the auto-correlated amplitude keeps falling, which supports the reflectometry theory stated in equation 1.

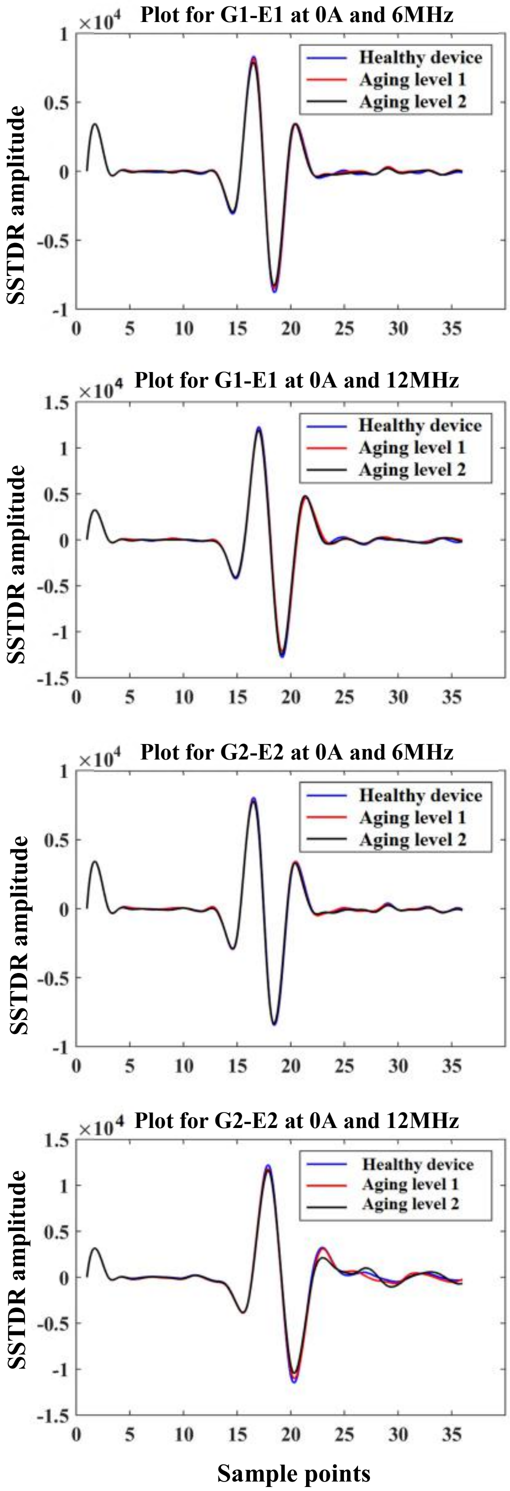


Fig 5: SSTDR auto-correlated amplitude plot with SSTDR applied across the gate-emitter terminals

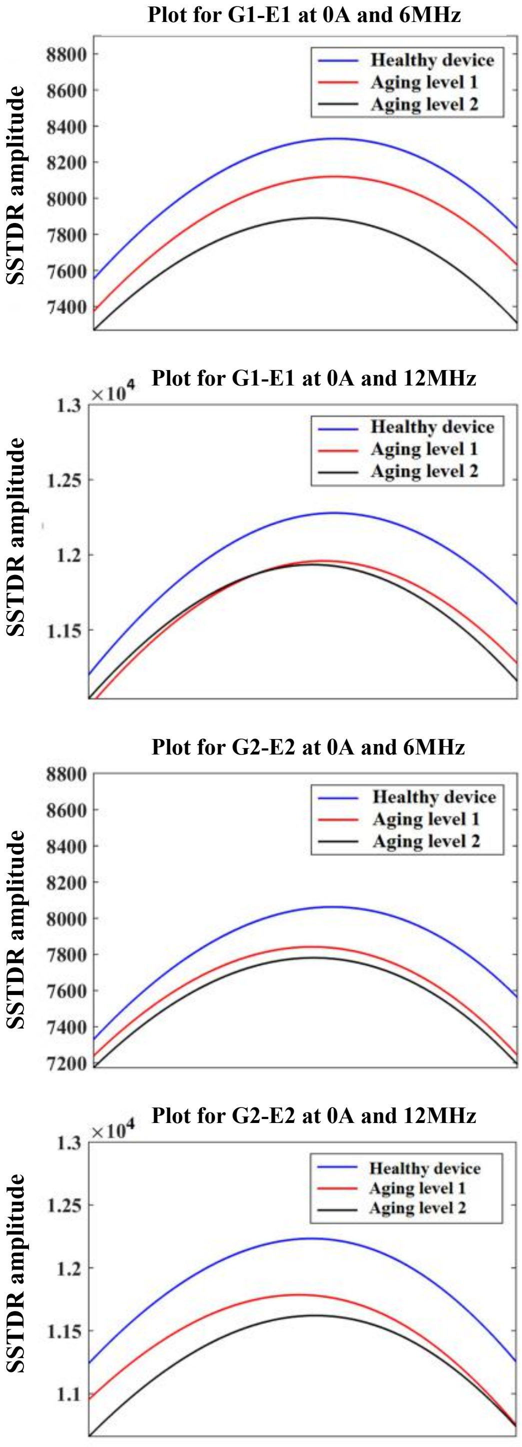


Fig 6: SSTDR auto-correlated amplitude plot with SSTDR applied across the gate-emitter terminals

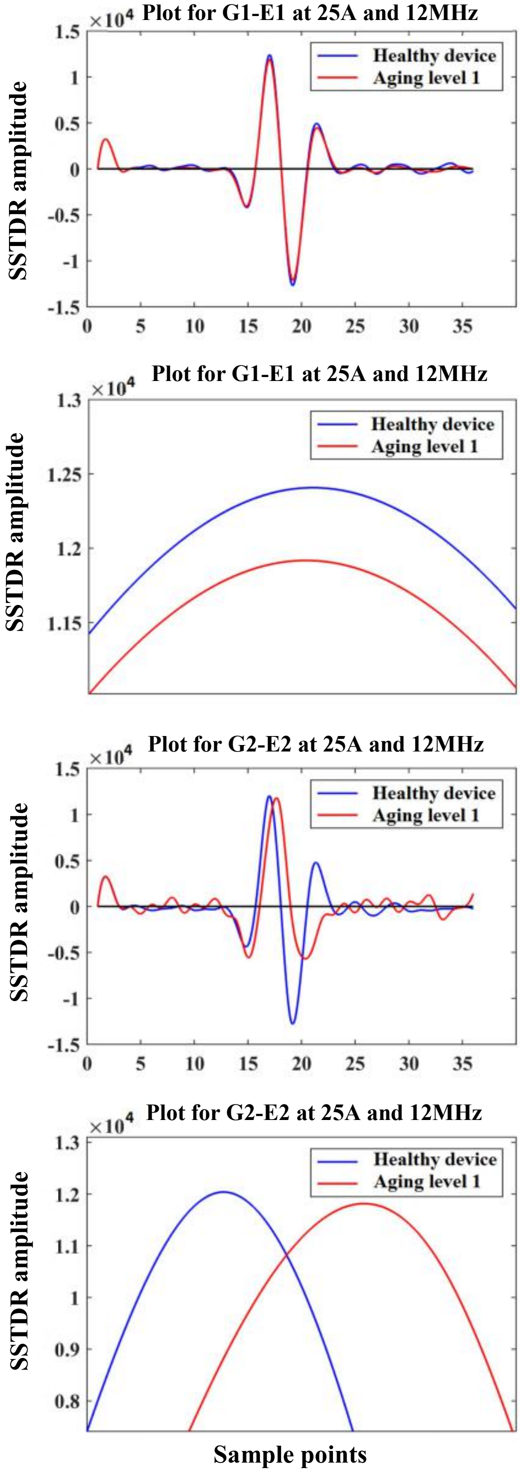
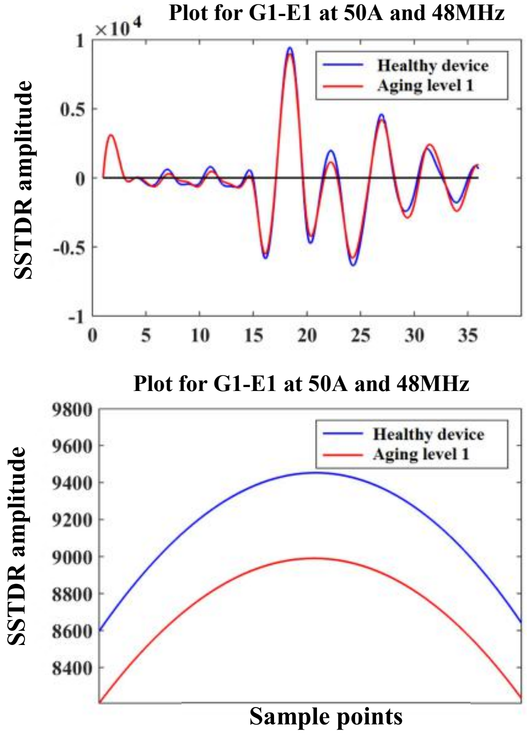


Fig 7: SSTDR auto-correlated amplitude plot with SSTDR applied across the gate-emitter terminals

At this point it is necessary to find a correlation between the V_{CEON} and the auto-correlated SSTDR amplitude in order to reach a conclusion. Table I presents the comparison between the above mentioned quantities which were recorded by the DAQ and SSTDR hardware respectively (also can be obtained from Fig 4, 5, and 6). From this table, it is apparent that the percent change in the V_{CEON} of healthy and failed device is about 5.49%. Similarly, the percent change in the amplitude of SSTDR reading between the healthy and failed device recorded at the gate terminals are 5.53% and 5.33% respectively. These values are very close to each other and hence it can be concluded that the SSTDR measurement at the gate terminals are sufficient to identify the failure or aging of the IGBT power module. In order to verify that the SSTDR technique is able to provide aging information independent of current levels, data points were recorded between the gate and emitter interface for 25A and 50A collector currents at 12MHz and 48MHz of SSTDR frequencies. These data have been plotted in Fig 7, Fig 8, and Fig 9. All of these plots show the similar pattern with 0A data. None of these figures contain the data associated to aging level 2 because the device failed by that time, and IGBT was not conducting any current at that point. Therefore, the SSTDR measurement is independent of the current through the device, and a single measurement is enough to identify aging related information inside the IGBT power module.

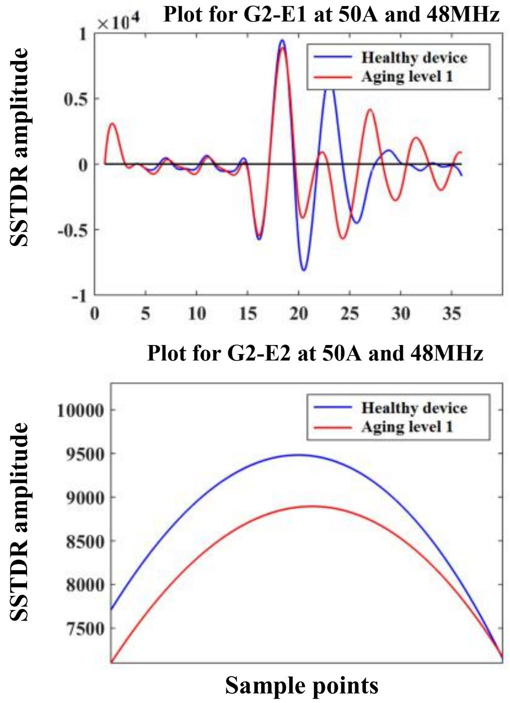
TABLE I: CORRELATION BETWEEN V_{CEON} AND SSTDR AMPLITUDE

	V_{CEON} (V)	SSTDR auto-correlated amplitude at I_C = 0A			
		Between terminal G1-E1		Between terminal G2-E2	
Healthy device	3.64	6MHz	12MHz	6MHz	12MHz
		8350	12250	8100	12200
Aged device (failed)	3.44	7800	11700	7700	11500
Percent change (%)	5.49	6.58	4.48	4.93	5.73
Average (%)	5.49	5.53		5.33	


Plot for G1-E1 at 50A and 48MHz

Plot for G1-E1 at 50A and 48MHz

Fig 8: SSTDR auto-correlated amplitude plot with SSTDR applied across the gate-emitter terminals


Plot for G2-E1 at 50A and 48MHz

Plot for G2-E2 at 50A and 48MHz

Fig 9: SSTDR auto-correlated amplitude plot with SSTDR applied across the gate-emitter terminals

In addition to the monitoring at the gate terminals, SSTDR were applied between the collector, C1 (1a) and emitter, E2 (2b) interface (nodes are shown in Fig 3) of the IGBT at different current levels (25A and 50A) and SSTDR frequencies (12MHZ and 48MHz). These data were plotted in Fig 10, and Fig 11 represents the zoomed versions to have a better clarity. Interestingly these plots show the similar pattern of aging as depicted in previous plots. This matching information proves that SSTDR based condition monitoring is independent of nodes and frequency at which the signal is applied. However, it is advantageous to apply SSTDR at the gate side because it involves lower voltage level and ease of access.

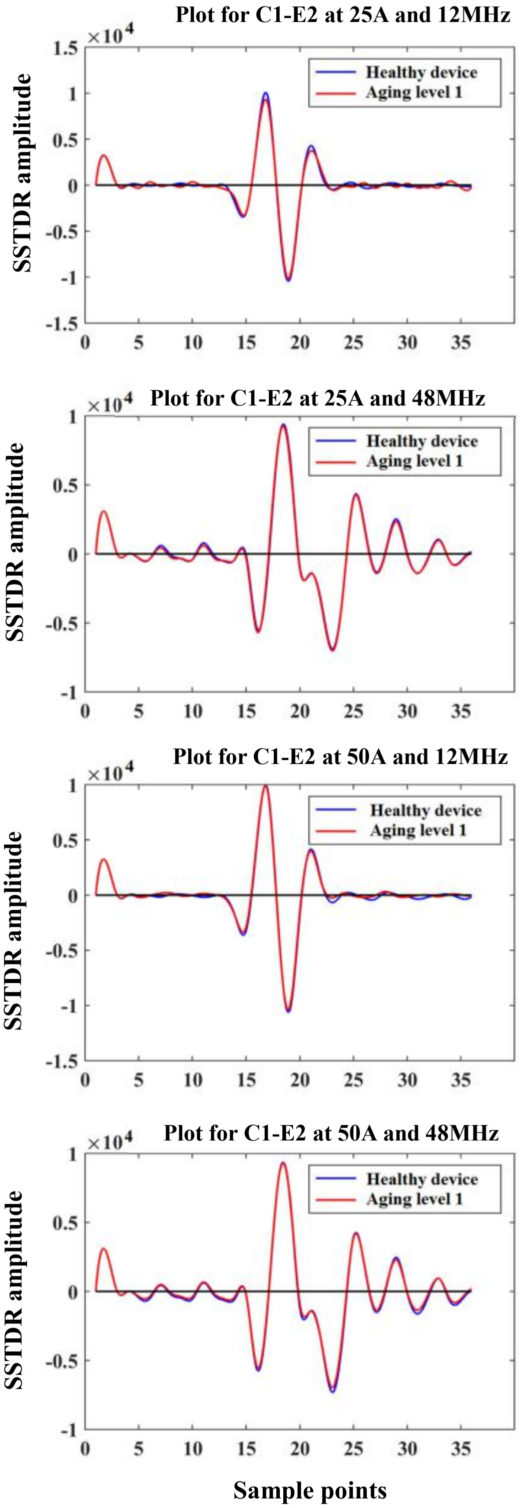


Fig 10: SSTDR auto-correlated amplitude plot with SSTDR applied across the collector-emitter terminals.

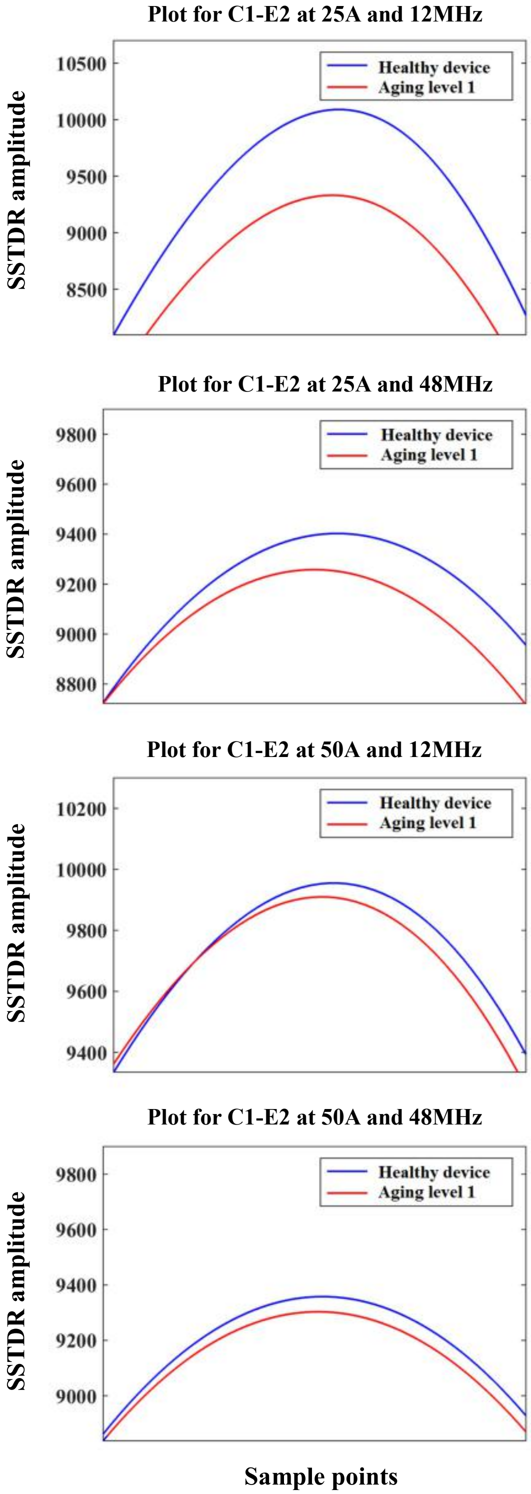


Fig 11: Zoomed SSTDR auto-correlated amplitude plots while SSTDR applied across the collector-emitter terminals.

V. CONCLUSIONS

Through the experimental results and associated plots, we are able to report that the SSTDR based technique can identify degradation inside an IGBT module by taking a single measurement from the gate-emitter terminals. This technique enables safe handling because of the lower potential level present at the gate, and it reduces the risk of personal injuries or damaging the equipment. In addition, the collector side of the module may not be available to the user in field operations. The auto correlation plots show a clear difference between the healthy and aged device in. These non-zero values are the evidence of the aging of the device; higher the difference, more the device has degraded. V_{CEON} plot also supports the aging and failure of the DUT. . This research idea can be extended to any power electronic module as well as for the full bridge converter module. In future, this reflectometry technique can also be incorporated into the gate driver circuit in order to automate the state-of-health estimation process, making it more user-friendly as well as reducing the human error during measurement.

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