A Scalable Drain Current Model of AlN/GaN MIS-HEMTs with Embedded Source Field-Plate Structures

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***Abstract*— A scalable drain current model of AlN/GaN MIS-HEMTs has been developed for embedded source field-plate structures. The physically derived model is scalable to the length, width, and the number of fingers, and then implemented in a circuit simulator with Verilog-A source codes. To apply the models to simulate power switching applications including DC-DC converters, the weak inversion to linear characteristics and the maximum drain current are important. The model is verified with measured data of three dimensions and two sets of multi-finger transistor TEGs that we fabricated with an embedded source field plate technology. The results show good agreements between measurements and simulations.**

Keywords— GaN, MISFET, HEMT, Modeling, Gate finger, Source field plate, Scaling

I. INTRODUCTION

GaN-based metal-insulator-semiconductor (MIS)-high-electron-mobility-transistors (HEMTs) are fabricated with an embedded source field plate (ESFP) located near the bottom of a gate using a self-alignment process [1] as shown in Fig. 1. There are mainly two advantages to employ ESFP. One is that the ESFP MIS-HEMTs achieve a lower gate-to-drain capacitance (C_{gd}) and gate-to-source capacitance (C_{gs}) than those of GaN MIS-HEMTs with a gate field plate (GFP). The other is that the maximum electric field along the channel becomes lower than in normal and GFP structures [2]. To apply the model to any power integrated circuit design, geometry scaling is necessary. Although some accurate models of GaN-based depletion mode HEMTs are published [3] and [4], these models do not support metal-insulator-semiconductor (MIS) gate structures. We also found that transistor model couldn't be applied to active drain and source resistances because of a convergence problem for small and large signal AC simulations, which is used in MVS model [3]. Although an useful compact model was reported at CSICS 2016 [5], gate geometry scaling was not implemented in the model.

In this research, dependencies of the gate length, width, and the number of fingers are developed and implemented in HSPICE with Verilog-A language. To simulate a maximum drain current at each gate bias voltage, the gate finger-number independent self-heating (SH) models have been derived based on isothermal current formulations [6]. A scalable drain/source active resistance model is also newly developed. In addition, the electric field reduction induced by the area of the ESFP is considered in the model, which has been verified with measurements of our dedicated test structures.

II. DEVICE STRUCTURE

The unit-transistor structure of the fabricated AlN/GaN MIS-HEMTs with ESFP is shown in Fig.1. The epitaxial layers with SiN passivation grown by metal organic chemical vapor deposition are as shown in Figs. 1 and 2. A sheet carrier density, sheet resistance, and mobility of 2DEG were 1.4×1,013 cm^2, 382 W/square, and 1,203 cm^2V/s, respectively. A 500-nm-thick SiO_2 film was formed on Mo films as inter-metal dielectric (IMD) films to extend the gate electrode over the passivation films and well above the ESFP and 2DEG to decrease C_{gs}. In Process 1 of our experiments, T_1 is made of SiO_2 of 40 nm in size, while T_2 is made of oxidized AlON of 3~5 nm in size. In Process 2 of our experiments, only T_1 is made of SiO_2 of 15 nm (T_2 = 0). The ESFP structure has the drain-side extension of the gate electrodes facing ESFP whose potential is fixed by source voltage, thus reducing C_{gd}.

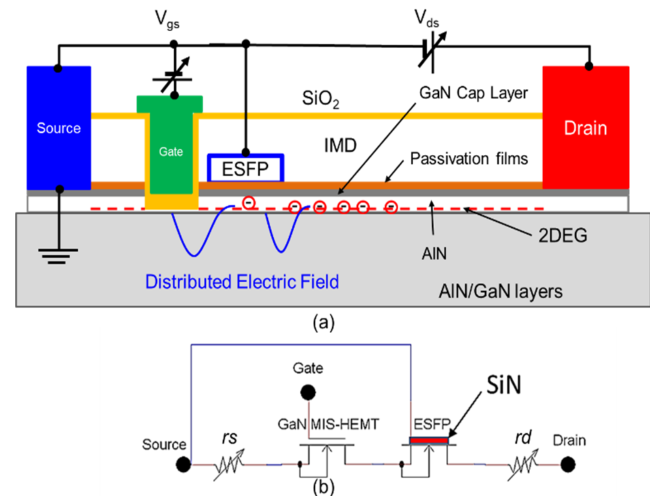

Fig. 1. Simplified (a) test structure and (b) the equivalent circuit model of the fabricated AlN/GaN MIS-HEMTs with ESFP. The source-to-gate and the gate-to-drain distance are 0.9 µm and 3.5 µm, respectively. The gate and drain biases (V_{gs} and V_{ds}) are applied to operate the device in active regions.

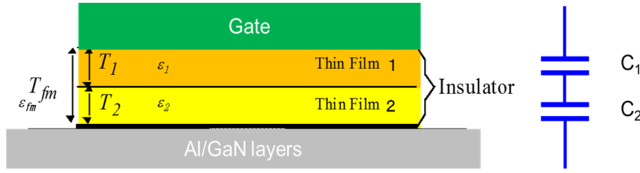

Fig. 2. Enlarged illustration of gate insulator capacitance beneath the gate region and the equivalent capacitance for the structure of double insulator-layer in Process 1, which was applied to previous experiments [5].

Since the gate-to-drain electric field distribution is divided into two peaks by adding ESFP, the strength of the electric field under the gate edge is decreased. As with MOSFETs, electron density under the gate insulator films becomes high in active biases. The electron density beneath the ESFP is low due to negative biases.

III. Model Equations

A. Gate Oxide Capacitance

As shown in Fig. 2, the total gate insulator film capacitance, C_{fm}, can be calculated as [7]

$$C_{fm} = \frac{C_1 \cdot C_2}{C_1 + C_2}, C_1 = \frac{\varepsilon_0 \cdot \varepsilon_1}{T_1}, C_2 = \frac{\varepsilon_0 \cdot \varepsilon_2}{T_2}, \quad (1) - (3)$$

$$T_{fm} = T_1 + T_2, \varepsilon_{fm} = C_{fm} \cdot T_{fm}, \quad (4), (5)$$

where ε_0, is free space vacuum permittivity, and ε_1, ε_2, *and* ε_{fm} are the dielectric constants of thin films 1, 2, and double layer insulators. The model can be applied to either of Process 1 or 2.

B. Threshold Voltage

Unlike MOSFETs, a gate channel area is not so dominant, compared to the two-dimensional electron gas (2DEG) layer (see Fig. 1) to drive drain current. In fact, the threshold voltage, V_{th}, dependencies on the gate length and width are weak as shown in Figs. 6-9. Using MOSFET's scaling theory, V_{th} is derived from threshold voltage at $V_{ds} = 0$, V_{TO}, as

$$V_{th} = V_{TO} + WDEP \cdot \frac{T_{fm}}{W_{eff}} - LDEP \cdot \frac{T_{fm}}{L_{eff}}, \quad (6)$$

where T_{fm}, W_{eff}, and L_{eff} are the thickness of the gate insulator film, effective width, and length, respectively.

C. Electron Mobility

The effective mobility, μ_{eff}, which is related to 2DEG mobility, is formulated regarding the low field mobility, μ_0. Since μ_{eff} is reduced by the gate electric field and SFP is modulated by L_{eff} of the device, μ_{eff} can be written as

$$\mu_{eff} = \frac{\mu_0 \cdot U_{Leff}}{1 + U_{Gate} \cdot U_{SFP}}. \quad (6)$$

Surface mobility, μ_s, is derived by the drain-to-source surface potential, ψ_{ds}, and the coefficient, θ_{sat}, as

$$\mu_s = \frac{\mu_{eff}}{\sqrt{1 + \theta_{sat}^2 \cdot \psi^2{}_{ds}}}. \quad (7)$$

The effect of gate voltage mobility modulation, U_{Gate}, in Eq. (6) is similar to that of MOSFET's [8], which is written as

$$U_{Gate} = UA\left(\frac{V_{gs} + 2 \cdot V_{th}}{T_{fm}}\right) + UB\left(\frac{V_{gs} + 2 \cdot V_{th}}{T_{fm}}\right)^2. \quad (8)$$

The mobility reduction induced by the SFP, U_{SFP}, is also normalized by the width of ESFP as

$$U_{SFP} = 1 + \frac{USFP}{W_{eff}} \cdot V_{ds}. \quad (9)$$

The mobility modulation, which depends on effective channel length, U_{leff}, in Eq. (2), is written as

$$U_{Leff} = 1 - UP \cdot e^{-L_{eff}/LP}. \quad (10)$$

USFP, *UP*, and *LP* are the fitting model parameters.

D. Drain/Source Resistance

The drain resistance (*RD*) and source resistance (*RS*) are increased with the number of fingers, N_{GF}, as

$$RD(S) = RD(S)_{ref} + N_{GF} \cdot RD(S)_{fin}, \quad (11)$$

where $RD(S)_{ref}$ and $RD(S)_{fin}$ are the normalized drain (source) resistance and parasitic resistance of each fin, respectively.

Although Eq. (11) is empirically correct, the drain/source resistance distributes bias-independent diffusion (sheet) resistance, bias-independent contact resistance, and bias-dependent resistance. The bias-independent resistance of drain (rd_{fix}) and source (rs_{fix}) are dependent on device and ambient temperatures (T_{dev} and T_{nom}), respectively. *RCD(S)* are the drain (source) contact resistance. They are reversely proportion to N_{GF} and W_{eff} as

$$rd(s)_{fix} = \frac{RCD(S)}{W_{eff} \cdot N_{GF}} \quad (12)$$
$$\left(1 + RCT1 \cdot (T_{dev} - T_{nom}) + RCT2 \cdot (T_{dev} - T_{nom})^2\right).$$

The drain and source resistance should be external and asymmetric, which makes accurate RF and power MISFETs simulation possible. Bias-dependent drain and source resistance can be connected between the external and internal drain and source nodes. The gate bias dependent resistance of drain and source are appended to the rd_{fix} and the rs_{fix} as

$$rd(s) = rd(s)_{fix} + \frac{RD(S)W \cdot N_{GF} \cdot RD(S)_{fin}}{\left(1 + PRWG\left(V_{gd(s)} - V_{th}\right)\right) \cdot \left(W_{eff} \cdot 10^{-6}\right)^{W_{RE}}}, \quad (13)$$

where $RD(S)W$ are the drain (source) resistance per unit gate width. $PRWG$ is a fitting coefficient of active resistance and W_{RE} is an exponent of gate width scaling.

E. Self-Heating

DC and Isothermal currents can be explicitly written as

$$I_{ds}\left(V_{ds}, T_{dev}\right) = I_{iso}\left[V_{ds}, R_{th} \cdot V_{ds} \cdot I_{ds}\left(V_{ds}, T_{dev}\right) + T_{dev}\right]. \quad (14)$$

A rise in temperature of the channel due to SH is given by

$$\Delta T = T_{dev_\max} - T_{dev}. \quad (15)$$

Here, T_{dev_max} is the maximum channel temperature, and T_{dev} is the ambient temperature. ΔT is defined as

$$\Delta T = I_{ds} \cdot V_{ds} \cdot \left(R_{th} + R_{th_fin} \cdot N_{GF}\right), \quad (16)$$

where R_{th} is increased by the N_{GF} with a coefficient R_{th_fin}, which is described in [6].

To solve a complete heat generation flow, 3-D calculations with the transistor structure are required. However, we only need to obtain the rise of temperature which is the relative amount in a closed box. Hence, we assume a rectangle material, and then solve linear equations.

R_{th} can be written as Eq. (17) using an electrical resistance equation,

$$R_{th} = \rho \frac{l}{S}, \quad (17)$$

whose temperature dependency is given by

$$R_{th}\left(T_{dev} + \Delta T\right) = \rho\left(T_{dev} + \Delta T\right)\frac{l}{S}, \quad (18)$$

where ρ is the thermal resistivity, l is the effective length, and S is the cross section area of a sample material. Since ρ is linearly proportional to the rise of temperature, we have the following equation:

$$\rho\left(T_{dev} + \Delta T\right) = \rho\left(T_{dev}\right) + c \cdot \Delta T, \quad (19)$$

where c is the slope of ρ - T. By plugging Eq. (19) into Eq. (18),

$$R_{th}\left(T_{dev} + \Delta T\right) = R_{th0} + c \cdot \frac{l}{S} \cdot \Delta T, \quad (20)$$

where R_{th0} is the thermal resistance at ambient temperatures. Now, we define K_{th} as

$$K_{th} = c \cdot \frac{l}{S}. \quad (21)$$

Using Eqs. (20) and (21), R_{th} can be simply expressed as

$$R_{th} = R_{th0} + K_{th} \cdot \Delta T. \quad (22)$$

Here, K_{th} is a fitting model parameter. For AC analysis, thermal capacitance, C_{th}, should be included in parallel with R_{th}. Then, thermal impedance, Z_{th}, is written with Eq. (16) as

$$Z_{th} = \frac{R_{th} + RFIN \cdot N_{GF}}{1 + j \cdot \omega \cdot C_{th} \cdot \left(R_{th} + RFIN \cdot N_{GF}\right)}. \quad (23)$$

Now, Eq. (16) is rewritten as

$$\Delta T = I_{ds} \cdot V_{ds} \cdot Z_{th}. \quad (24)$$

To derive a drain current with SH, I_{ds_th}, we first refer to the temperature dependency of effective mobility that is

$$\mu_{eff}(T) = \mu_{eff}\left(T_{dev}\right)\frac{T}{T_{dev}}. \quad (25)$$

Effective mobility with SH can be

$$\mu_{eff}\left(T_{dev} + \Delta T\right) = \mu_{eff}\left(T_{dev}\right)\left(1 + {\Delta T}/{T_{dev}}\right). \quad (26)$$

Then, the drain current with SH of an AlN/GaN MIS-HEMT is written as

$$I_{ds_th} = I_{ds}\left(T_{dev}\right)\left(1 + {\Delta T}/{T_{dev}}\right). \quad (27)$$

F. ESFP Scaling

Since an ESFP operates as a MISFET as shown in Fig. 1 (b), the model equations of the ESFP transistor are the same as those of the main MISFET. Process and model parameters used in the ESFP transistor are extracted from measured data of scaled devices. The length (fixed to 0.5 µm in the process) and the width (the same size as the gate width) are set.

G. MVS Model Equations

MVS model [3] has been applied to drain current equations at the saturation region as

$$I_{ds} = W_{eff} \cdot Q_{i,x0} \cdot v_x \cdot F_{sat}, \quad (28)$$

$$Q_{i,x0} = C_{fm} \cdot n \cdot \varphi_t \ln\left(1 + e^{\frac{V_{gs} - \left(V_{th} - \alpha \cdot \varphi_t \cdot F_f\right)}{n \cdot \varphi_t}}\right), \quad (29)$$

$$n = \frac{SS}{\varphi_t \cdot \ln(10)} + n_d \cdot V_{ds}, \quad (30)$$

$$V_{th} = V_{to} - V_{ds}\left(\delta - \delta_1 \cdot V_{ds}\right), \quad (31)$$

$$F_{sat} = \frac{V_{ds}/\theta_{sat}}{\left(1+\left(V_{ds}/\theta_{sat}\right)^{\beta}\right)^{1/\beta}}, \quad (32)$$

$$v_x = \frac{v_{x0}}{1+\theta \frac{Q_{i,x0}}{C_{fm}}}, \quad (33)$$

where φ_t is the thermal voltage. α, SS, δ, δ_l, β, and θ are model parameters. Eq. (33) is the modified equation to neglect the SH term to use our model.

IV. Test Structure Design

As shown in Figs. 3, 4, and 5, dedicated test structures including 2- and 6- gate finger devices are fabricated with Process 2 for measurement and parameter extractions. The 2-finger devices include gate length and width variations as listed in TABLE I.

TABLE I. GEOMETRIES OF FABRICATED TEST DEVICES

Number of Fingers	Gate Width [µm]	Gate Length [µm]
2	100	0.8
6	100	0.8
2	66	0.8
2	33	0.8
2	100	1.0

As shown in Fig. 3, the source terminals and interconnects are designed as thick as possible to obtain small resistance and better grounding performance for future small and large signal AC measurements. In the same reason, pad assignments follow a ground-signal-ground (G-S-G) probe pattern.

V. Experiments and Discussions

DC measurements of our 2- and 6-finger transistor structures are performed in the pulse measurement mode with a curve tracer. The supplied biases with pulse width 100 µs and duty cycle 50 % are used. In Figs. 6, 7, and 8, gate length and width dependency on V_{th} is too small to distinguish from the process characteristic deviation of devices. Model parameters for threshold voltage, linear and saturation drain currents, and gate channel length and width dependencies are extracted with multi-gate length and width device measurements, accurately in advance. In Figs. 10 and 13, self-heating effect, which is supported in Eqs. (26) and (27), is shown in wide and 6-finger devices (W_{eff} = 100 µm). Since the peak electric field is driven by the main and ESFP transistors in Fig. 1 (b), the gate area in main transistor and the bottom area of the ESFP should be accurately scaled.

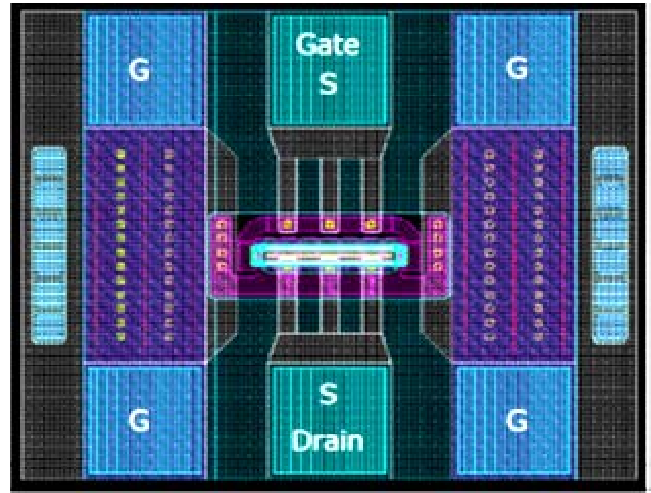

Fig. 3. Overview of the G-S-G pad connection to the measurement test structure of our GaN MIS-HEMT. Here, L=0.8 µm and W=100 µm. The source terminal is connected to thick ground pads.

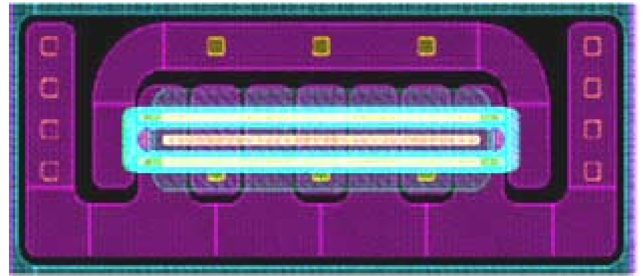

Fig. 4. Enlarged illustration of 2-finger gate test structure of a GaN MIS-HEMT in Fig. 3.

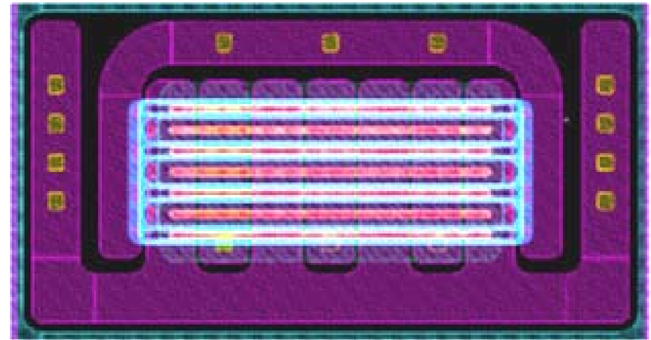

Fig. 5. 6-finger gate test structure of a GaN MIS-HEMT. Here, L=0.8 µm and W=100 µm.

The modeling results in Figs. 10 through 13 show the scaling performance by comparing with measurements. Figs. 6 through 13 show that the model has reasonable accuracy to simulate static drain currents in the linear and saturation regions.

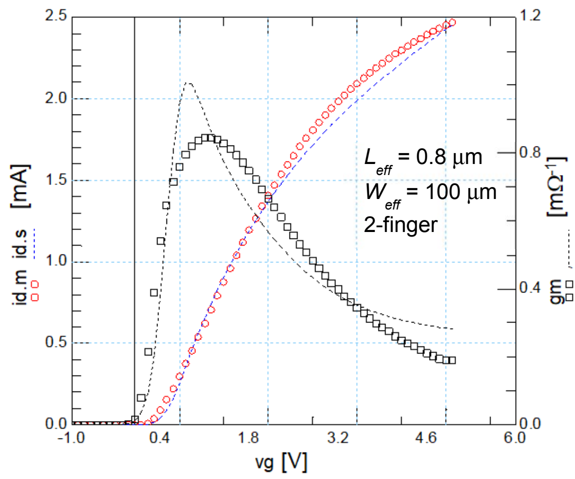

Fig. 6. Measured (marked) and simulated (break lines) I_{ds}-V_{gs}

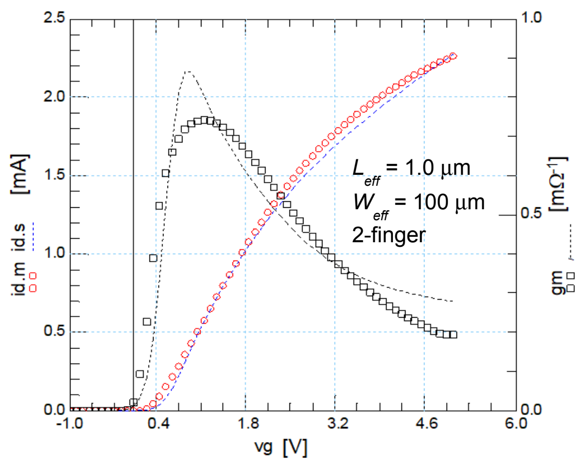

Fig. 7. Measured (marked) and simulated (break lines) I_{ds}-V_{gs}

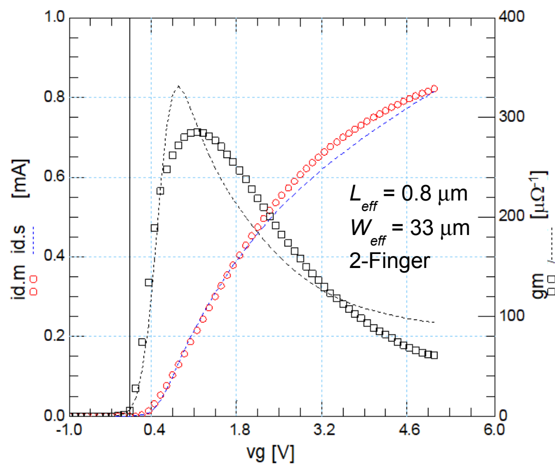

Fig. 8. Measured (marked) and simulated (break lines) I_{ds}-V_{gs}

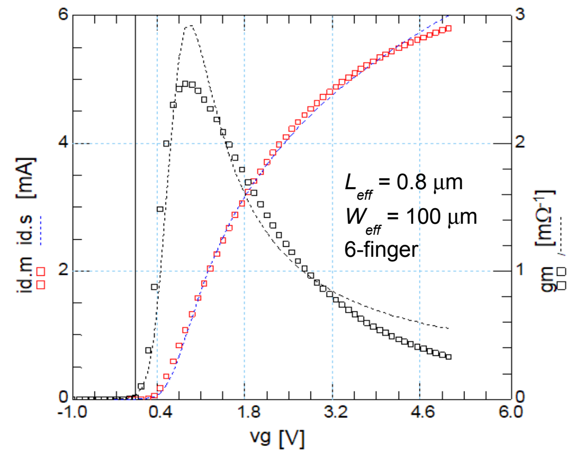

Fig. 9. Measured (marked) and simulated (break lines) I_{ds}-V_{gs}

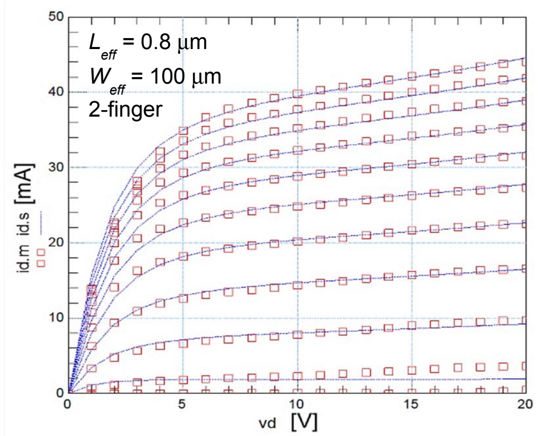

Fig. 10. Measured (marked) and simulated (break lines) I_{ds}-V_{ds}

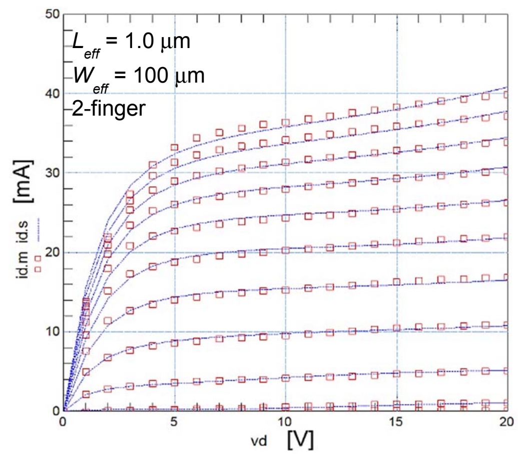

Fig. 11. Measured (marked) and simulated (break lines) I_{ds}-V_{ds}

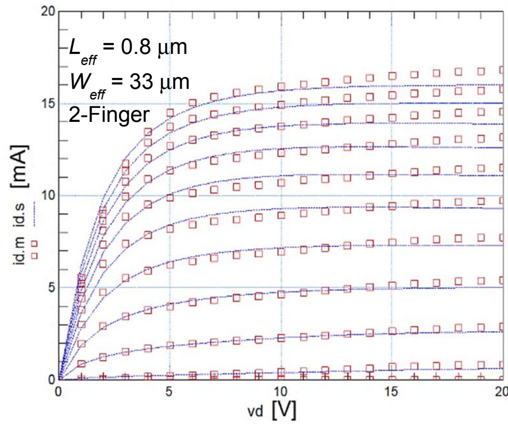

Fig. 12. Measured (marked) and simulated (break lines) I_{ds}-V_{ds}

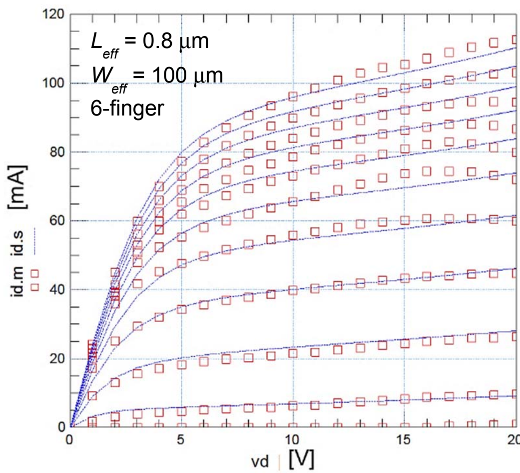

Fig. 13. Measured (marked) and simulated (break lines) I_{ds}-V_{ds}

VI. CONCLUSIONS

Gate width and length, and gate finger-number scalabilities of our AlN/GaN MIS-HEMT model were presented. Dedicated test structures including 2- and 6- gate finger devices are fabricated for measurement and parameter extractions. The new model and parameter extraction demonstrated good agreement with the measurements of our fabricated test structures.

We are now in the process of developing an enhanced RF scalable model. Since the capacitance of a MIS-HEMT causes a large power loss at light load, input capacitance, C_{iss}, reverse transfer capacitance, C_{rss}, and output capacitance, C_{oss}, will be accurately characterized.

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