

# Inverter Power Module Parasitics Modeling with Cross-coupling Simplification for Fast Model Extraction and Switching Characteristics Simulation

Thomas D. Bayer  
General Electric, Aviation  
Dayton, OH 45479  
bayert@ge.com

**Abstract**—Inverter power module parasitics models are commonly used for inverter switching analysis, gate drive tuning, and EMI characterization. This paper investigates the parasitics modeling and simplification of an inverter power module. The circuit cross-coupling is characterized by Z-parameter matrix. Three types of cross-coupling modeling/simplification methods are studied in this research. The effect of cross-coupling simplification on model extraction time and circuit simulation time are evaluated. To validate the accuracy of the parasitics models, the circuit simulations are compared with the experimental results.

**Keywords**—power module; parasitics; cross-coupling; simulation

## I. INTRODUCTION

### A. The Effect of Parasitics on Semiconductor Switching Characteristics

The switching characteristics of power semiconductors are essential to the efficiency of power converters and the power integrity of pulse width modulation (PWM). Studies on power semiconductor switching characteristics mainly focus on voltage/current transient time [1-3], overshoot and plateau in the waveforms, switching loss [4], and delay time. Dominant factors that affect the semiconductor switching characteristics include the electrical dynamic properties of semiconductor dies [5, 6], the converter load conditions [7], the gate drive transient output [8, 9], the parasitics in the converter commutating loop [10]. The switching transient time of power semiconductor has been reducing for decades because of the improvement of semiconductor fabrication [11].

The effect of parasitics on switching characteristics has been investigated on Si devices [12, 13], SiC devices [14, 15] [16-19], and GaN devices [20-22]. Generally, the capacitive parasitics that affect the switching characteristics is from the device intrinsic capacitance [23]. The inductive parasitics that affect the switching characteristics is from the conductors' loop inductance [24]. Because of the fast switching speed of most of the power semiconductors, the resistive parasitics in the power converter has a modest effect on the semiconductor switching characteristics [25]. State-of-the-art studies on resistive

parasitics mostly focus on the thermal characteristics and the loss of the conductors in the power converter.

### B. The Physics of Power Converter Parasitics

In a power converter circuit setup, the circulating loops can be categorized into gate drive loops and power loops. In most of the hard-switching circuitry, small gate drive loop is desired to reduce the loop inductance. The layout of the power loops in a power converter compromises to the converter parasitics control, EMI design, heat transfer, insulation, and component mechanical properties [11]. Minimizing the parasitic inductance in a commutating power loop is one of the key strategies to reduce device's switching transient time and current/voltage overshoots [26, 27].

The loop inductance includes mutual inductance and self-inductance. Due to mutual inductance, the switching transient in one circulating loop will induce transient voltage potential in all the coupled circulating loops. Optimized cross-coupling in an integrated power module is desired during the power module layout design [11].

The parallel-die strategy is commonly used in high current rating semiconductor power modules. Equivalent current sharing among the paralleled dies is desired in power module integration design. The switching transient current sharing of paralleled dies is directly related to the self-inductance of each sharing branch, and the mutual inductance/cross-coupling among branches. State-of-the-art literatures have evaluated the effect of paralleling layout on power module switching characteristics [28].

### C. Parasitics Modeling and Extraction

The parasitics in a simple circuit layout, such as a straight conductor trace or a square conductive layer, can be calculated by the formulas in [29, 30]. The parasitics in a complex layout can be evaluated with finite element analysis (FEA) where the input/output characteristics can be modeled as a multi-port linear system [31]. With more ports included, the system matrix has higher order. The system matrix extracted by FEA is commonly used for circuit simulation.

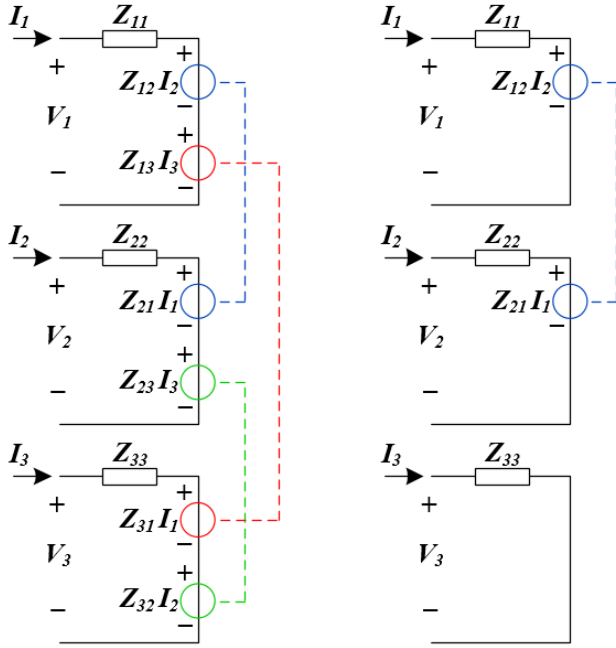
Extracting the system matrix from the CAD model and using the system matrix for circuit simulation both can require great computing time. [31] studied model simplification; [32] investigated improving simulation speed.

#### D. Research Opportunities

The balance of detailed parasitics modeling and reducing model extraction/simulation time is essential for the model-based power electronics design/analysis; however, this topic has not been fully investigated by existing studies based on an industry standard design platform. This paper presents the parasitics modeling and simplification of a two-level, three-phase inverter power module. The mechanism of cross-coupling simplification is demonstrated with the circuit Z-parameter matrix. Three types of cross-coupling modeling/simplification methods are evaluated based on model extraction time, circuit simulation time, and simulation accuracy. The simulation and experimental results are compared.

## II. POWER MODULE PARASITICS MODELING AND SIMPLIFICATION

### A. Circuit Cross-coupled Model Simplification



(a) Fully coupled (b) Simplified  
Fig. 1 3x3 circuit and its simplification

A Z-parameter matrix describes the behavior of any linear electrical network that can be considered as a black box with a number of ports. A port in this context is a pair of electrical terminals carrying equal and opposite currents into and out of the network, and having a particular voltage between them. For all ports, the voltages may be defined in terms of the Z-parameter matrix and the currents by the following matrix equation.

$$V = Z I \quad (2.1)$$

The Z-parameter matrix for a three-port network is shown in (2.2), and the equivalent circuit for this  $3 \times 3$  matrix is shown in Fig. 1(a). In this case,  $Z_{11}$ ,  $Z_{22}$ , and  $Z_{33}$  are self-impedance.  $Z_{12}$ ,  $Z_{13}$ ,  $Z_{23}$ ,  $Z_{21}$ ,  $Z_{31}$ ,  $Z_{32}$  are mutual-impedance. In this research, self-impedance includes resistance, self-inductance, and self-capacitance. Mutual impedance is dominated by mutual inductance. The effect of mutual capacitance on circuit simulation is subtle.

Mutual impedance is commonly used to characterize the cross-couplings between different ports in a circuit network. Circuit analyzer can choose not to characterize the weak cross-couplings in the circuit modeling. As a result, the Z-parameter matrix for a circuit can be de-ordered. Take the circuit in Fig. 1(a) as an example. If the port 3 is weakly coupled to port 1 and port 2,  $Z_{13}$ ,  $Z_{31}$ ,  $Z_{23}$ , and  $Z_{32}$  can be approximated to 0 as shown in (2.3). By re-writing (2.3) to (2.4) and (2.5), the equivalent circuit in Fig. 1(a) will be simplified to the circuit as shown in Fig. 1(b).

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ Z_{31} & Z_{32} & Z_{33} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \quad (2.2)$$

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & 0 \\ Z_{21} & Z_{22} & 0 \\ 0 & 0 & Z_{33} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \quad (2.3)$$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (2.4)$$

$$V_3 = Z_{33} I_3 \quad (2.5)$$

### B. Inverter Circuitry

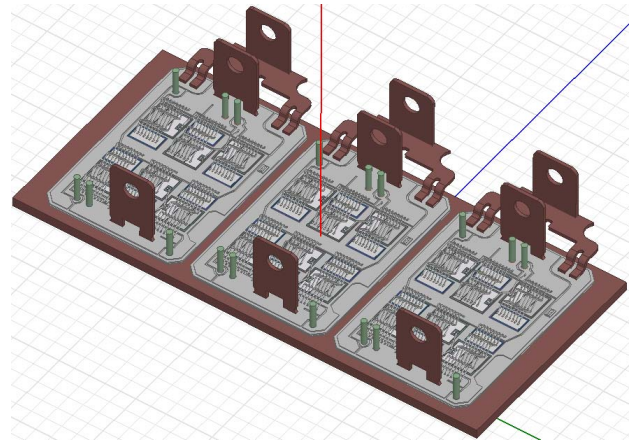


Fig. 2 Inverter power module layout (open sample)

This paper studies a two-level, three-phase inverter power module. The open-module layout is shown in Fig. 2. It can be seen that the three phases in the power module have identical layout. This research focus on the parasitics and cross-coupling within one phase and the cross-coupling between different phases are not discussed. The schematic for a single phase is shown in Fig. 3, where the dies of IGBTs and diodes are paralleled in groups of three respectively.

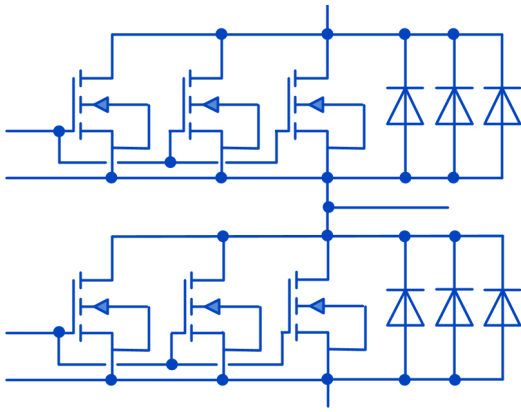


Fig. 3 Inverter power module single phase schematic

C. Power Module Parasitics Modeling

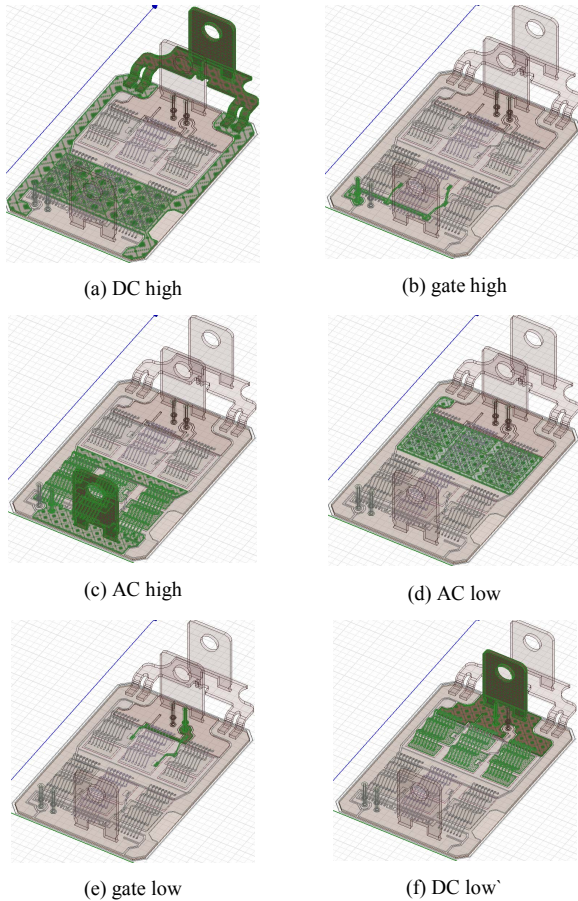


Fig. 4 Identified nets for the power module single phase: nets shown in the layout

In the power module parasitics analysis, each group of the connected conductive components is modeled as a “net”. The identified nets for the single phase of the power module is shown in Fig. 4 (a) to (f), and the corresponding parts in the schematic is shown in Fig. 4 (g) to (l). By modeling all the mutual impedance in the single phase layout, a fully cross-coupled model (also referred to as the “FC model”) can be derived as shown in the schematic in Fig. 5. Note that all the

nets shown in Fig. 5 are cross-coupled, and a  $34 \times 34$  Z-parameter matrix is derived.

The aforementioned cross-coupled model simplification (part A of section II) is applied to the single phase of the power module. By splitting the fully cross-coupled model to a high-side model (a  $17 \times 17$  matrix) and a low-side model (a  $16 \times 16$  matrix) as shown in Fig. 6, the mutual impedance across the high-side model and the low-side model are set to zero. As a result, any circuit behavior on the high-side model will not affect the low-side model and vice versa. These two split models together are also referred to as the half-split model (the HS model).

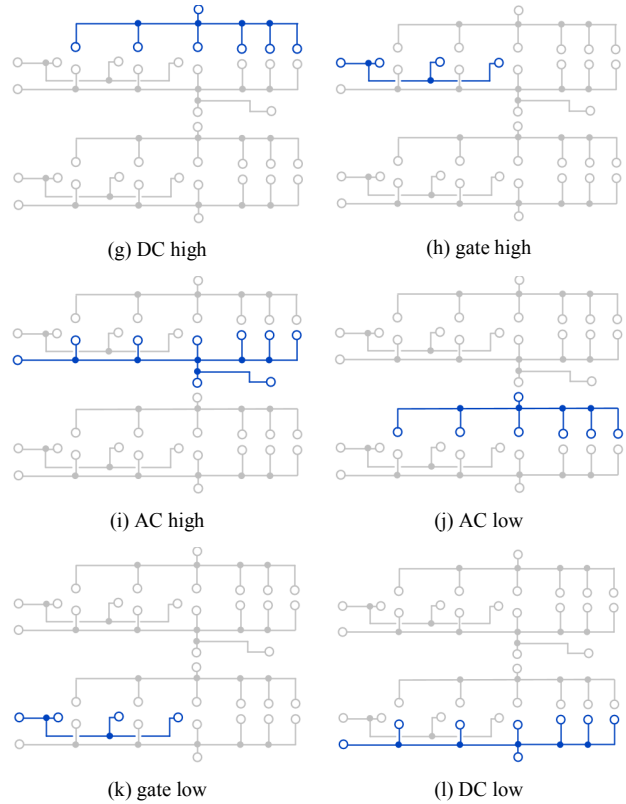


Fig. 4-continued Identified nets for the power module single phase: nets shown in the schematic

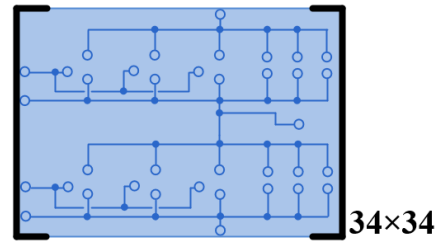


Fig. 5 Fully coupled model (FC model)

By completely removing the cross-coupling between/among any nets in Fig. 4, six independent parasitic models can be derived as shown in Fig. 7. The six parasitic models correspond to one  $8 \times 8$  matrix, one  $7 \times 7$  matrix, two  $6 \times 6$  matrices, and two

3×3 matrices. These six models are also referred to as independent-parasitic model (IP model).

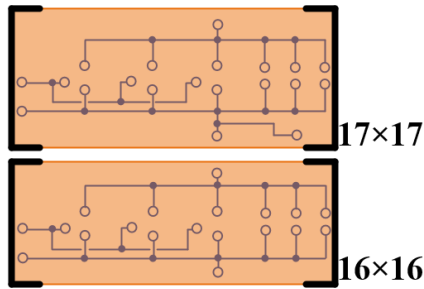


Fig. 6 Half-split model (HS model)

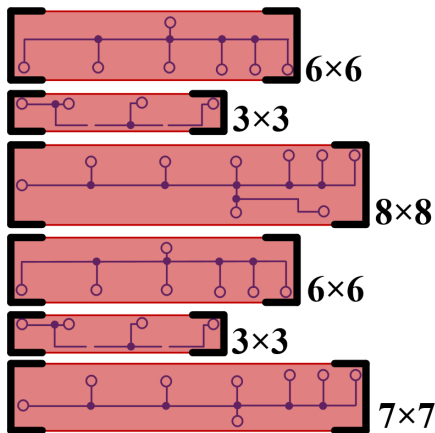


Fig. 7 Independent-parasitic model (IP model)

### III. MODEL EXTRACTIN TIME AND CIRCUIT SIMULATION TIME

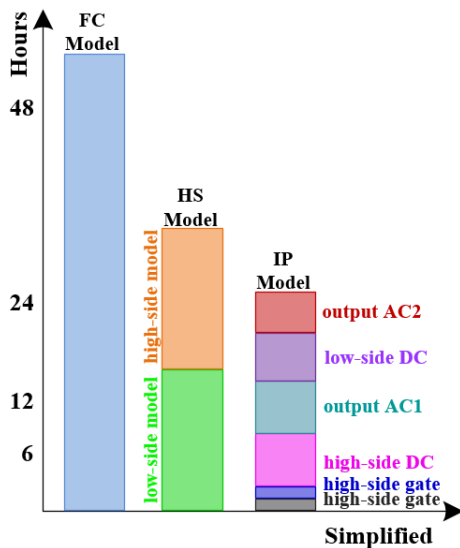


Fig. 8 Model extraction time

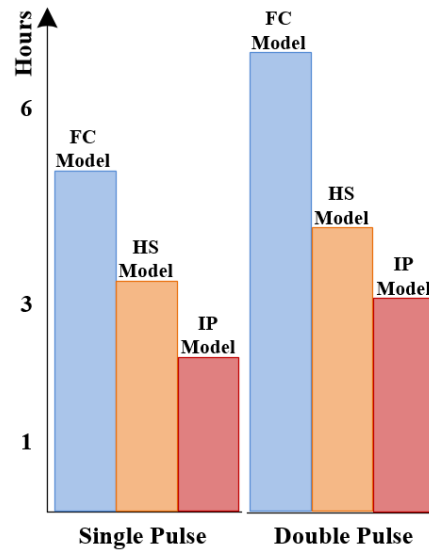


Fig. 9 Circuit simulation time

In this research, all the analysis are conduct on an independent workstation. The model extraction for the three types of parasitics model (the FC model, the HS model, and the IP model as discussed in part C, section II) is conducted under ANSYS Q3D. The model extraction time for the FC model, the HS model, and the IP model is shown in Fig. 8. It can be seen that with more cross-coupling included in the model, the overall model extraction time is longer.

The extracted single phase parasitics model are configured into simulation circuitry for inverter turn-off transient analysis (single-pulse simulation) and turn-on transient analysis (double-pulse simulation). The circuit simulation time for single-pulse testing and double-pulse testing are shown in Fig. 9. It can be seen that with more cross-coupling included in the model, both the turn-off transient and the turn-on transient take longer circuit simulation time.

Note that model extraction tools like ANSYS Q3D have functions to simplify the Z-parameter matrix of the extracted model. However, the physics behind the matrix simplification is not always explicit to the users.

### IV. SIMULATION AND EXPERIMENTAL RESULT

In this paper, the experimental results are derived from a two level three-phase prototype inverter setup with the DC bus voltage at 380-Volt. The simulation results are based on the FC model, the HS model, and the IP model. The setup of the simulation model is the same as the prototype inverter setup.

Fig. 10 shows the simulation result for the turn-on transient analysis (double-pulse simulation). To compare the details of the three models, waveforms in the dashed box in Fig. 10 are zoomed in and shown in Fig. 11, Fig. 12, and Fig. 13. It can be seen that the FC model captures more transient details while the result from the IP model is smoother. Subtle difference can be observed in  $V_{CE}$  and  $V_{GE}$  by comparing the simulation result from the aforementioned three models. In the simulated  $I_C$  waveforms, the overshoot generated by the FC model is more

accurate when comparing to the experimental waveform in Fig. 14.

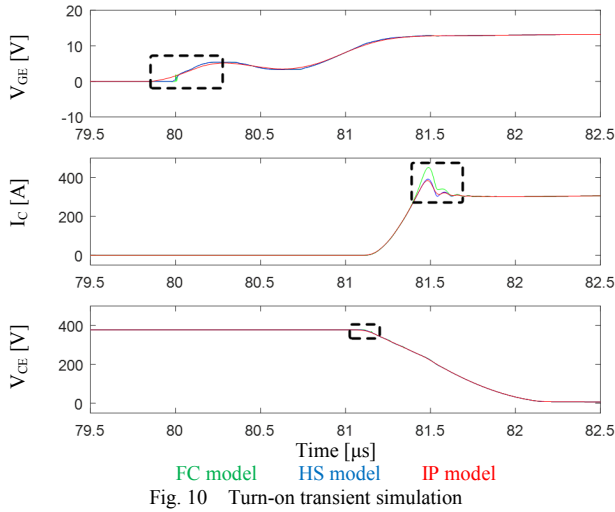


Fig. 10 Turn-on transient simulation

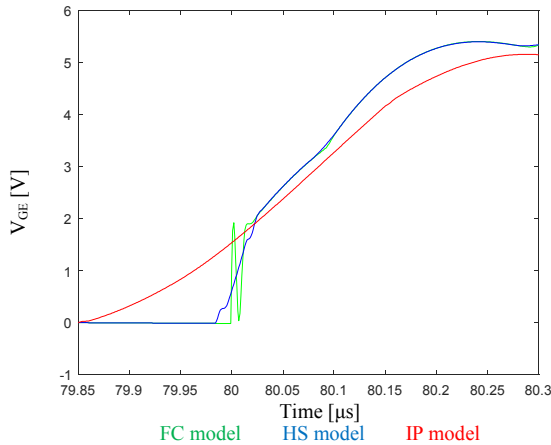


Fig. 11 Turn-on transient simulation, zoomed in  $V_{GE}$

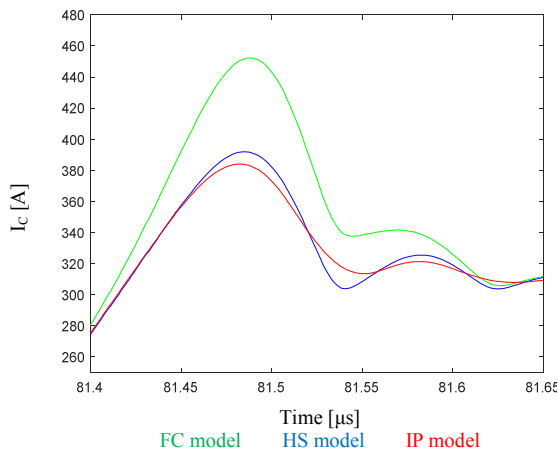


Fig. 12 Turn-on transient simulation, zoomed in  $I_C$

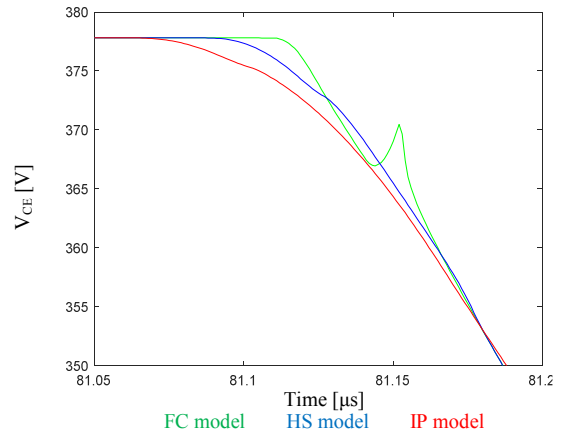


Fig. 13 Turn-on transient simulation, zoomed in  $V_{CE}$

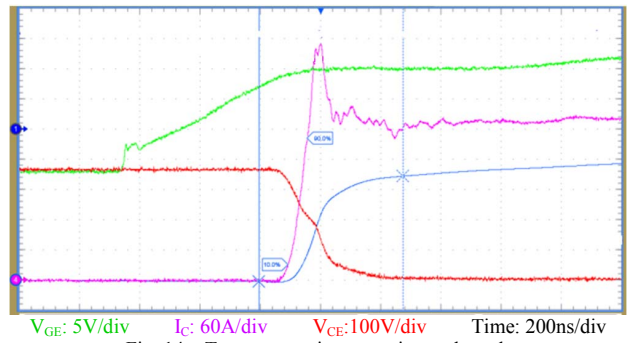


Fig. 14 Turn-on transient experimental result

Fig. 15 shows the simulation result for the turn-off transient analysis (single-pulse simulation). To compare the details of the three models, waveforms in the dashed box in Fig. 15 are zoomed in and shown in Fig. 16, Fig. 17, and Fig. 18. It can be seen that the FC model generates waveforms with more details. The details from the HS model is slightly less when compared with the FC model. The transient details from IP model are modest. Subtle difference can be observed in  $V_{GE}$  and  $I_C$  by comparing the simulation result from the aforementioned three models. In the simulated  $V_{CE}$  waveforms, the overshoot generated by the FC model is more accurate when comparing to the experimental waveform in Fig. 19.

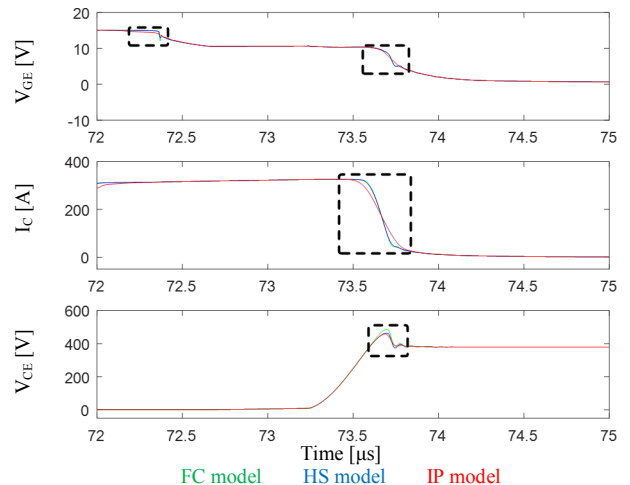


Fig. 15 Turn-off transient simulation

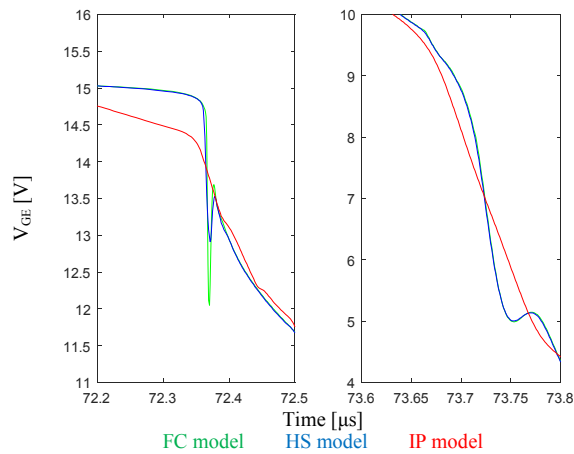


Fig. 16 Turn-off transient simulation, zoomed in  $V_{GE}$

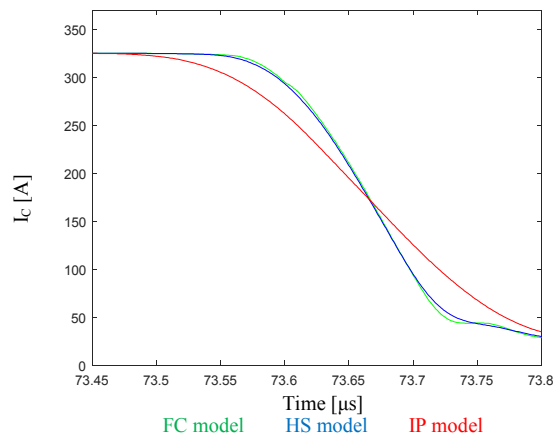


Fig. 17 Turn-off transient simulation, zoomed in  $I_C$

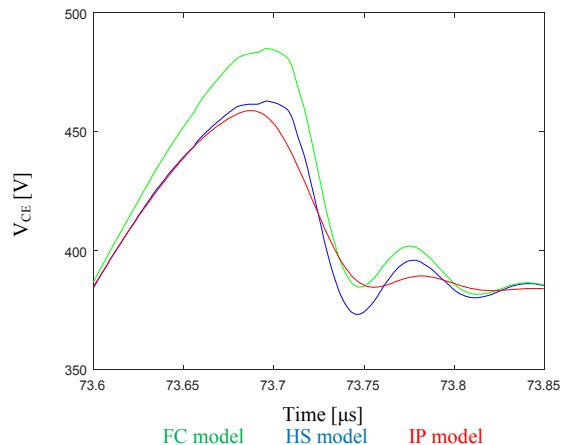


Fig. 18 Turn-off transient simulation, zoomed in  $V_{CE}$

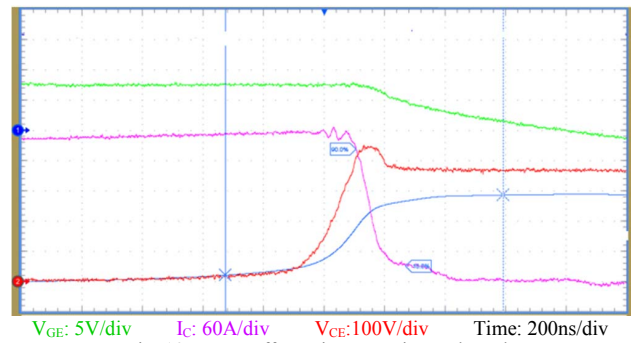


Fig. 19 Turn-off transient experimental result

## V. CONCLUSIONS

The key conclusions of the paper are summarized as follows:

- By simplifying the cross-coupling in the parasitics model, the Z-parameter matrix for a circuit can be de-ordered.
- Parasitics cross-coupling simplification can effectively reduce the model extraction time and circuit simulation time.
- Parasitics models with properly simplified cross-coupling can be used simulate the inverter switching properties.

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## REFERENCES

- [1] R. Pittini, Z. Zhang and M. Andersen, "Switching Performance Evaluation of Commercial SiC Power Devices (SiC JFET and SiC MOSFET) in Relation to the Gate Driver Complexity", *ECCE Asia Downunder*, Melbourne, Australia, 2013, pp. 233-239.
- [2] H. Niu, R.D. Lorenz, "Sensing Power MOSFET Junction Temperature Using Circuit Output Current Ringing Decay", *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1763-1773, Jul., 2014.
- [3] H. Niu, R.D. Lorenz, "Sensing Power MOSFET Junction Temperature Using Circuit Output Current Ringing Decay", *2013 IEEE Energy Conversion Congress and Exposition (ECCE)*, Denver, CO, Sept. 2013.
- [4] Y. Xiong, et al., "New Physical Insights on Power MOSFET Switching Losses", *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 525-531, Feb., 2009.
- [5] H. Niu, R.D. Lorenz, "Evaluating Different Implementations of Online Junction Temperature Sensing for Switching Power Semiconductor", *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, Canada, Sept. 2015.
- [6] Y. Xia, J. Roy and R. Ayyanar, "A Capacitance-Minimized, Doubly Grounded Transformer less Photovoltaic Inverter With Inherent Active-Power Decoupling," in *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5188-5201, July 2017.
- [7] H. Niu, "The effect of load properties on the reliability of machine drives — The temperature and stress analysis of power module bond wires", *2017 IEEE Energy Cons. Congress and Expo. (ECCE)*, Cincinnati, Oct. 2017.
- [8] H. Niu, R.D. Lorenz, "Sensing Power MOSFET Junction Temperature Using Gate Drive Turn-on Current Transient Properties", *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1677-1687, Nov. 2, 2015.
- [9] H. Niu, R.D. Lorenz, "Sensing Power MOSFET Junction Temperature Using Gate Drive Turn-on Current Transient Properties", *2014 IEEE*

- Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh, PA, Sept. 2014.
- [10] J. Wang, *et al.*, "Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance", *IEEE Trans. Power Electron.*, vol. 28, no.1, pp. 573-590, Jan., 2013.
- [11] D. Ward, *et al.*, "Fundamentals of Semiconductors for Hybrid- Electric Powertrain", Infineon Technology North America Corp, Livonia, MI, 2013.
- [12] Y. Shen, *et al.*, "Parasitic Inductance Effects on the Switching Loss Measurement of Power Semiconductor Devices", *IEEE International Symposium on Industrial Electronics*, Montreal, Canada, 2006, pp. 847-852.
- [13] H. Niu, R.D. Lorenz, "Sensing IGBT Junction Temperature Using Gate Drive Output Transient Properties", *IEEE Applied Power Electronics Conf. and Expo (APEC)*, Charlotte, NC, Mar. 2015.
- [14] X. Lyu, N. Ren, Y. Li and D. Cao, "A SiC-Based High Power Density Single-Phase Inverter With In-Series and In-Parallel Power Decoupling Method," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 893-901, Sept. 2016.
- [15] H. Zeng and F. Z. Peng, "SiC-Based Z-Source Resonant Converter With Constant Frequency and Load Regulation for EV Wireless Charger," in *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8813-8822, Nov. 2017.
- [16] H. Niu, R.D. Lorenz, "The Effect of Gate Drive Topology on Online Silicon-Carbide MOSFET Junction Temperature Sensing", *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, Canada, Sept. 2015.
- [17] Q. Zhu, L. Wang, D. Chen, L. Zhang and A. Q. Huang, "Design and implementation of a 7.2kV single stage AC-AC solid state transformer based on current source series resonant converter and 15 kV SiC MOSFET," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, USA, 2017, pp. 1288-1295.
- [18] N. Ren, K. Sheng, J. Zhang and F. Peng, "Gate drive investigations of IGBT modules with SiC-Schottky freewheeling diodes," *2013 IEEE Energy Conversion Congress and Exposition*, Denver, CO, 2013, pp. 2871-2876.
- [19] H. Niu, R.D. Lorenz, "Real-time Junction Temperature Sensing for Silicon Carbide MOSFET with Different Gate Drive Topologies and Different Operating Conditions", *IEEE Trans. Power Electronics*, early access article, May 2017.
- [20] Z. Liu, *et al.*, "Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT", *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1977-1985, Apr., 2014.
- [21] Y. Xia, J. Roy and R. Ayyanar, "A GaN based doubly grounded, reduced capacitance transformer-less split phase photovoltaic inverter with active power decoupling," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, USA, 2017, pp. 2983-2988.
- [22] H. Niu, R.D. Lorenz, "Sensing Gallium Nitride HEMT junction temperature using gate drive output transient properties", *IEEE Applied Power Electronics Conf. and Expo (APEC)*, Long Beach, CA, Mar. 2016.
- [23] Z. Chen, *et al.*, "Modeling and simulation of 2 kV 50 A SiC MOSFET/JBS power modules", *European Conference on Power Electronics and Applications*, Barcelona, Spain, 2009, pp. 1-10.
- [24] Y. Xiao, *et al.*, "Analytical Modeling and Experimental Evaluation of Interconnect Parasitic Inductance on MOSFET Switching Characteristics", *Applied Power Electron. Conf. and Expo (APEC)*, Anaheim, CA, 2004, pp 516-521.
- [25] H. Niu, R.D. Lorenz, "Evaluating Different Implementations of Online Junction Temperature Sensing for Switching Power Semiconductor", *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 391-401, Oct., 2016.
- [26] K. Siu, *et al.*, "Performance Analysis of Package Parasitic Inductances for Fast Switching MOSFET in Converter", *Intl. Power Electronics and Application Conference and Exposition*, Antalya, Turkey, 2014, pp 314-319.
- [27] M. Meisser, *et al.*, "Parasitics in Power Electronic Modules: How parasitic inductance influences switching and how it can be minimized", *Intl. Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy*, Nuremberg, Germany, 2015, pp 1-8.
- [28] H. Niu, "A Review of Power Cycle Driven Fatigue, Aging, and Failure Modes for Semiconductor Power Modules", *IEEE International Electric Machines and Drives Conference (IEMDC)*, Miami, FL, May 2017.
- [29] [http://www.calctool.org/CALC/eng/electronics/parallel\\_plate](http://www.calctool.org/CALC/eng/electronics/parallel_plate)
- [30] <https://www.allaboutcircuits.com/tools/parallel-wire-inductance-calculator/>
- [31] L. Van Thielen, *et al.*, "Fast method to include parasitic coupling in circuit simulations", *Proceedings 2002 Design, Automation and Test in Europe Conference and Exhibition*, Paris, France, 2002, pp 1033-1037.
- [32] L.M. Silveira, *et al.*, "Improving the Efficiency of Parasitic Extraction and Simulation of 3D Interconnect Models", *IEEE Intl. Conf. on Electronics, Circuits and Systems*, Pafos, Cyprus, 1999, pp 1729-1732.