Finite Element Model Optimization and Thermal Network Parameter Extraction of Press-Pack IGBT

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***Abstract*—The junction temperatures of multiple chips in a press-pack IGBT device cannot be all measured directly. Finite element modeling is a powerful tool to investigate internal temperature distribution. In order to evaluate the performance of the press-pack structure, a computationally more efficient thermal network can be extracted to analyze coupled electro-thermal behavior under variable ambient and operating conditions. This paper describes an approach to derive such a thermal network model, based on superimposition using a series of FE modeling results. As a result, it is possible to establish a multiple input multiple output (MIMO) thermal network model, given the dimensions of a press-pack design and the material property. The paper illustrates the accuracy of the FE modeling approach using experiment on a single-chip device. In addition, this paper also proposes an improved Foster model of press-pack IGBT devices, taking into account the thermal coupling effect between chips. A relationship between the coupling thermal impedance and chip distance is established to simplify the calculation of some model parameters. The comparison between the thermal network model and FE model of a six-chip device under power cycling condition demonstrates the validity of the proposed model.**

***Keywords*—press-pack IGBT; finite element modeling; thermal network; thermal coupling; curve fitting**

I. INTRODUCTION

Finite element method is widely used in thermal analysis and thermal design of press-pack power modules [1-5], as it is difficult to measure the junction temperatures of all chips directly. Although the heat conduction process in the device can be simulated accurately and the temperature distribution of paralleled chips can be obtained using this FE method, a computationally efficient thermal network model is more desirable to analyze different ambient and operating conditions. This study is concerned about deriving a thermal network model of press-pack IGBT from FE analysis.

In FE analysis a chip is usually simplified as an evenly distributed heat source without considering the internal structure. However, there is almost no power loss in the termination region actually, and due to the different doping concentration of regions inside cells [6], the power loss distribution inside the chip can be uneven, thus the model of chips may need to be refined to improve the accuracy. Thermal coupling exists between multiple chips in parallel, but a Foster model which is computationally efficient does not usually consider this effect because it does not physically represent any point of common coupling, which can cause error [7].

In this paper, the loss distribution inside the chip is considered, and the surface temperature distribution obtained from FE analysis with such an internal loss distribution agrees well with infrared imaging. The paper proposes an improved Foster model of a multiple chip press-pack IGBT device considering the coupling, while each chip is still to be modelled as a single point of the maximum junction temperature with the total power loss injected into the thermal network from that point. A relationship between the coupling thermal impedance and the chip distance is established to reduce calculation.

II. THE STRUCTURE OF SINGLE CHIP PRESS-PACK IGBT

In China, the press-pack IGBT chips adapted so far have mainly been of the NPT (non-punch through) structure. When the NPT-type IGBT operates in the on-state, it can be simplified to an equivalent model comprising a P-i-N diode connected in series with a MOSFET operating in the linear region, as shown below in Fig.1. The conduction voltage of IGBT mainly drops across the N-base region, P^+ collector/N-base junction and MOSFET [8], and the sum of P^+/N- junction voltage and N- base voltage is namely the conduction voltage of P-i-N diode in the equivalent circuit model.

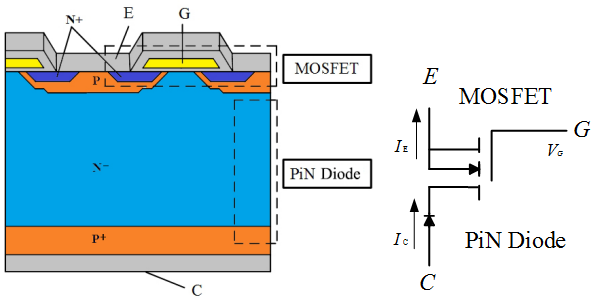

Fig. 1 Structure of NPT IGBT and its on-state equivalent circuit model

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The NPT-type IGBT chip can be divided into the active, gate, termination, N-base and collector regions, corresponding to the chip structure and its on-state equivalent circuit model. Since NPT IGBT can be equivalent to a MOSFET/P-i-N rectifier model during the on-state, the N-base and collector regions can be merged as P-i-N region, as shown in Fig.2.

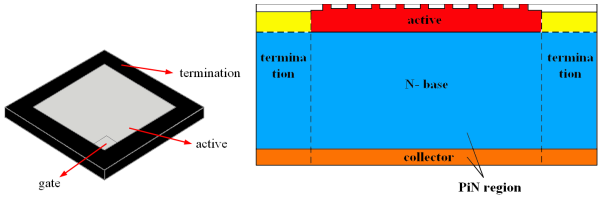


Fig. 2 Structure diagrams of NPT-type IGBT chip in on-state

Since press-pack IGBT is mainly used in high-power grid equipment such as modular multilevel converter submodules, and due to the low switching frequency of the device, the switching loss of IGBT accounts for only about 15 percent of the total power loss, which is far less than the conduction loss [9]. Therefore, the heat source distribution inside the IGBT chip mainly depends on the conduction loss distribution. Assuming that the current densities in the termination and gate regions are zero, and since the conduction resistivities of the active region and P-i-N region are different due to their different doping concertation, the active and P-i-N regions may need to be considered as two heat sources of the IGBT chip. The power loss proportions of these two sources can be derived from their on-state voltage proportions under the test condition, assuming their conduction current densities are the same, and their conduction voltages can be acquired by establishing the NPT-type IGBT equivalent circuit model in PSpice [10-12]. Thus, the equivalent FE model of press-pack IGBT chips considering the uneven loss distribution can be finally obtained.

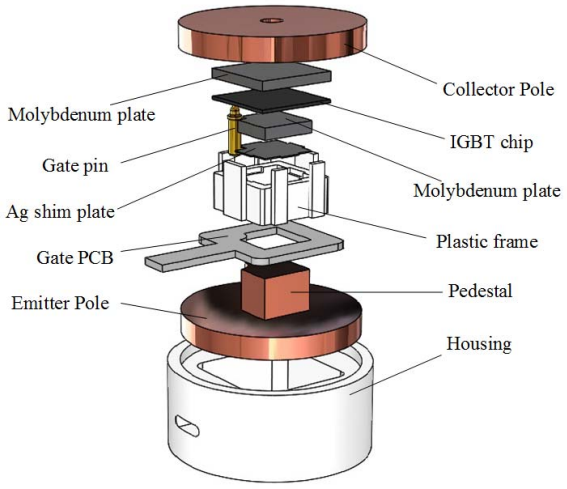


Fig. 3 Structure diagram of a press-pack IGBT single-chip device

The press-pack IGBT studied in this paper adopts the full pressure structure represented by WESTCODE and TOSHIBA, and a single-chip device is shown in Fig.3. The copper poles are used as the collector and emitter terminals of the press-pack IGBT. Two molybdenum plates act as buffer layers since the coefficients of thermal expansion (CTE) of copper and silicon are different. The Ag shim plate is used to make uniform the pressure distribution of the paralleled chips in a multi-chip device, and the gate pin is used to connect the gate of IGBT chip from the gate PCB. All components in the structure are pressed together directly by a clamp.

III. Finite Element Modeling of Press-pack IGBT and Experimental Verification

On the basis of the proposed model of IGBT chips, the temperature field FE model of a press-pack IGBT device is established to derive the thermal network model.

The modeling method is illustrated by the case of a press-pack IGBT single-chip module (3300V, 50A), and the boundary condition of the device is shown in Fig.4. The device is assumed to operate in constant turn-on state. Since the gate pin, gate PCB and housing has less effect on heat dissipation capability of the device, these structures are omitted to simplify the FE model.

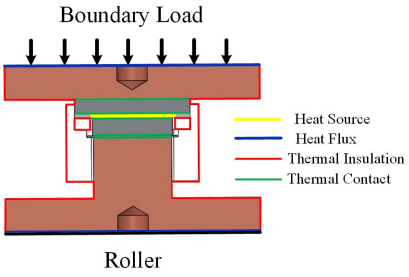


Fig. 4 Boundary Condition of press-pack IGBT FE model

At the surfaces of collector pole and emitter pole, the boundary load and roller are respectively set to simulate the clamp, and the heat fluxes are also set to represent the heatsink. The value of boundary load and convective heat transfer coefficient are 1200N (10.32N/mm^2) and 3200W/(m^2·°C) respectively. The effect of pressure on heat conduction at the interface of neighboring layers is considered by setting thermal contact at the interface. The thermal radiation of other outside surfaces is neglected and these surfaces are set as heat insulation.

Two FE models, which have the same geometry structures, material properties and boundary conditions except for the chip model, are built to show the effect of the chip model on FE simulation results of the device. In the traditional model 1, the IGBT chip is simplified as an evenly distributed heat source with the total loss 160W, since the nominal conduction voltage of the device is 3.2V measured at room temperature and 50A. While in the refined model 2, the proposed equivalent circuit chip model in Section II is applied. According to the simulation result of the PSpice model, the proportions of the conduction voltage dropping across the active and N- regions of IGBT

chip are 53.6% and 46.4% of the total, hence the loss power of these two heat sources are 85.7W and 74.3W respectively.

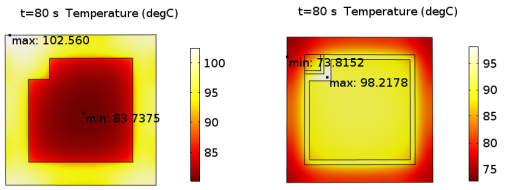


Fig. 5 Chip temperature distribution of two models

The chip temperature distribution is shown in Fig.5 for the two models, when the device reaches heat balance. It is clearly that the temperature distribution of model 1 is very different from that of model 2. In model 1, the temperature of the termination region is the highest, whereas the termination region has the lowest temperature in model 2. The position and value of the maximum temperature point of the chip in the two models are also different, which results in the difference of the derived junction-case thermal resistance, as shown in TABLE I. The junction-case thermal resistance on the emitter side obtained from model 1 is 34.99% higher than that from model 2. This means that the loss distribution inside the IGBT chip affects not only the chip temperature distribution but also the derived junction-case thermal resistance significantly.

TABLE I. SIMULATION RESULTS OF TWO MODELS

Variables	model 1	model 2	Percentage difference (model 2)
The highest temperature of IGBT chip (°C)	102.56	98.22	4.42%
The lowest temperature of IGBT chip (°C)	83.74	73.82	13.44%
Junction temperature (°C)	91.96	88.19	4.27%
Case temperature at emitter side (°C)	40.69	43.67	-6.82%
Case temperature at collector side (°C)	60.87	57.89	5.15%
Junction-case thermal resistance at collector side (°C/W)	0.895	0.663	34.99%
Junction-case thermal resistance at emitter side (°C/W)	0.304	0.296	2.70%

In order to verify the FE model, an experiment on the 3300V/50A single-chip device was carried out with the power cycling test rig of press-pack IGBT, as shown in Fig.6. The experimental conditions are the same as the boundary conditions of the FE models. The device uses double-side water cooling and the room temperature is 26°C.

The device under test (DUT) is shown in Fig.7. A part of housing was removed to measure the internal temperature of the device with a FLIR infrared camera. In order to acquire the accurate surface temperatures and reduce the effect of reflection, the side surfaces of chip, molybdenum plate, collector pole and emitter pole were coated with black insulation pigment, as shown in the figure, and the emissivity of coating is 0.98.

(a) Test vehicle of power cycling (b) Measurement Fixture

(c) Infrared Camera

Fig. 6 Power cycling test rig of press-pack IGBT

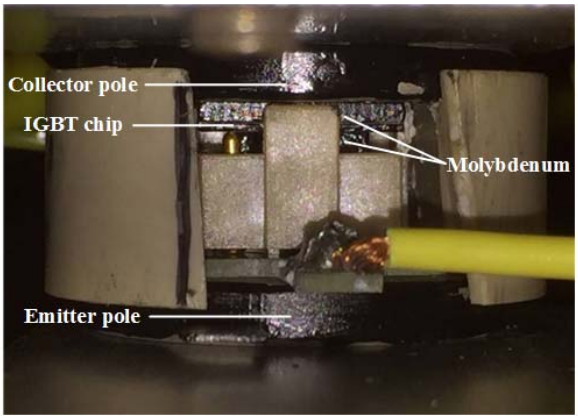


Fig.7 The device under test

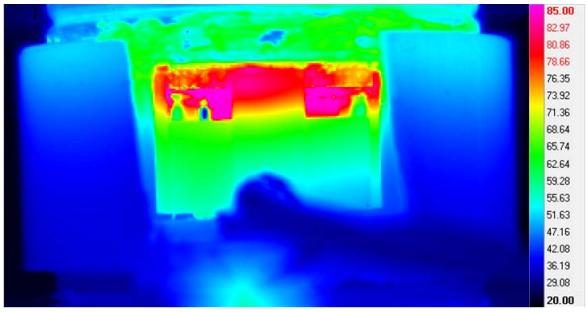


Fig.8 Thermograph of DUT at thermal steady state

The temperature distribution measured by infrared camera is shown in Fig.8, when the device reached the thermal steady state under DC current. It is noted that the surface temperature of the lower molybdenum plate is higher than the IGBT chip. Considering the chip is the main heat source in the device, this means that the temperature of termination region is lower than the active region, which is consistent with the simulation result of the proposed FE model (model 2).

The average side surface temperatures of the collector pole, chip, emitter pole, the upper and lower molybdenum plates are measured and compared with the simulation results, as shown in TABLE. II. The comparison result illustrates the error of the traditional FE model (model 1) is much higher than the refined model (model 2), and the largest error of model 1 is the side temperature of the IGBT chip, where the simulated temperature is about 27.95% higher than the experiment result. Since the error of model 2 is less than ±4%, the proposed model is basically validated.

TABLE II. COMPARISON OF SIMULATION RESULTS AND EXPERIMENT RESULTS

Average temperature at thermal steady state (℃)	model 1	model 2	Infrared camera	Error of model 1	Error of model 2
The side surface of upper molybdenum plate	80.14	71.20	70.94	12.97%	0.37%
The side surface of IGBT chip	98.47	77.38	76.96	27.95%	0.55%
The side surface of lower molybdenum plate	75.96	79.88	80.80	-5.99%	-1.14%
The side surface of emitter pole	39.88	42.81	44.47	-10.32%	-3.73%
The side surface of collector pole	59.89	56.86	56.75	5.53%	0.19%

IV. THERMAL NETWORK OF MULTICHIP PRESS-PACK IGBT CONDSIDERING THERMAL COUPLING

A computationally more efficient thermal network is widely used to analyze coupled electro-thermal behavior under variable ambient and operating conditions. In this section, a thermal network model of press-pack IGBT considering thermal coupling is proposed and derived based on FE method.

A. Thermal Network Model of Press-pack IGBT

The common RC thermal network models include Cauer model and Foster model, both of which characterize one-dimensional heat conduction. Since the heat conduction in the power module is mainly in the vertical direction, this one-dimensional approximation is effective and efficient.

The Physical Cauer model and the 3rd order Foster model of a press-pack IGBT are shown in Fig.9, assuming the numbers of IGBT and FRD chips in the device are m and n respectively. Where $T_{j,T1}$ and P_{T1} are the junction temperature and power loss of IGBT chip 1, and T_{amb} the ambient temperature. Due to the double-side cooling characteristic, the thermal model of the press-pack IGBT includes two thermal paths. The cases at both sides of the device are assumed to be at a uniform temperature, i.e. $T_{case(c)}$ and $T_{case(e)}$, to simplify the model.

In the physical Cauer model, each layer in the device is represented by a thermal resistance and a thermal capacitance. The thermal contact resistances, which characterize the heat conduction at the interfaces of neighboring layers, are represented by variable resistances because they are pressure dependent. The parameters of the physical Cauer model can be obtained by equation (1) [13] according to the geometric parameters and material properties of the device.

$$R_{th} = \frac{d}{\lambda_{th} A} \qquad C_{th} = c_{heat} \rho d A \tag{1}$$

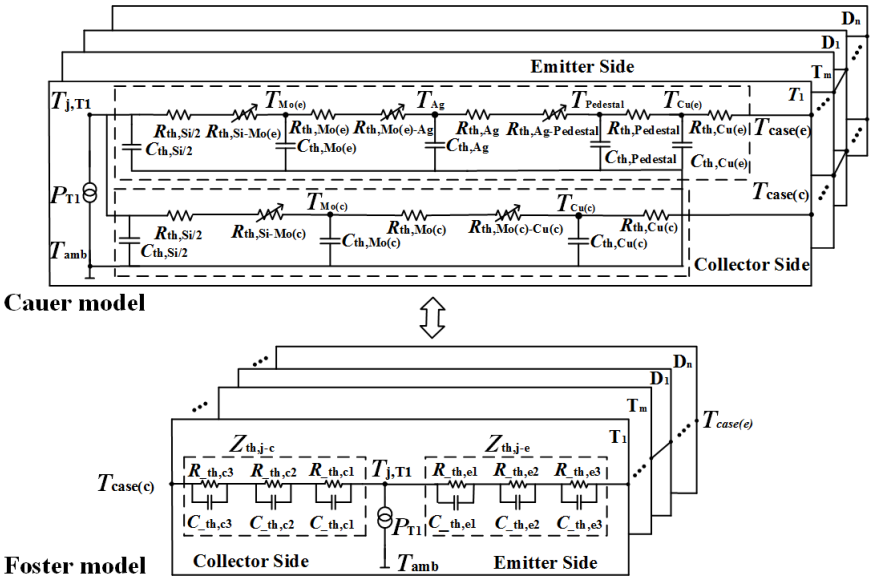


Fig.9 Thermal network models of press-pack IGBT

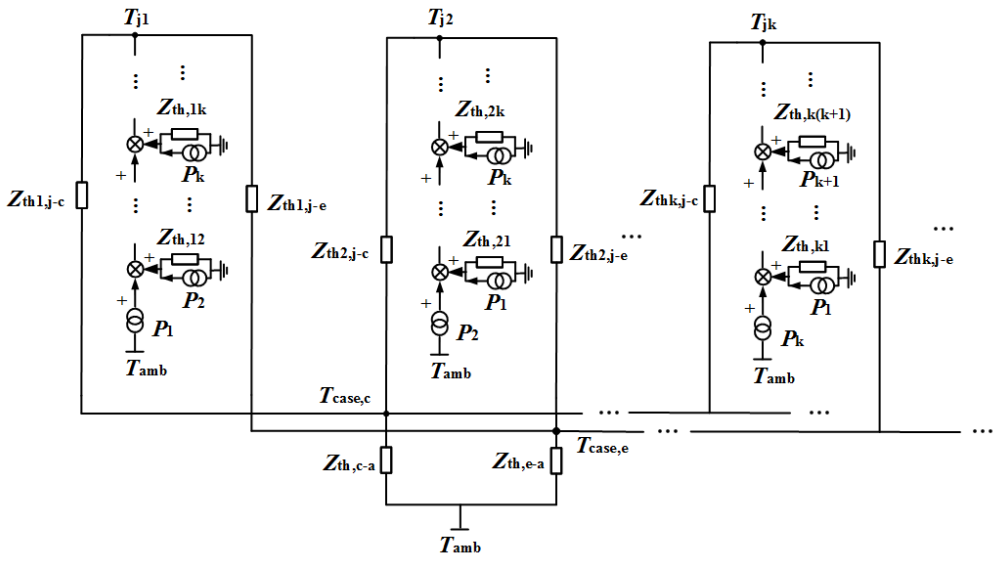


Fig.10 Proposed foster model of press-pack IGBT considering multi-thermal coupling

where d and A are the thickness and effective heat transfer area of each layer, ρ, λ_{th} and c_{heat} are the mass density, thermal conductivity and specific heat capacity of packaging material respectively. It is noted that if the cross section area of the layer is much larger than its neighboring, A is the function of the thickness, rather than a constant such as the cross section area and the contact interface area, hence the thermal parameters of the layer need to be obtained using integral.

The thermal contact resistance can be determined by the theoretical formulas and corrected by measuring the temperature drop across the contact interface at a given clamping force [5,14,15].

In a multichip press-pack device, because the chips share the emitter and collector pole structures, thermal coupling exists between chips and affects the temperature distribution of the device. Considering the physical Cauer model is mainly used to characterize the temperature of each layer, and its order is much higher than the Foster model, as shown in Fig.9, it is reasonable to neglect the direct thermal coupling between chips to simplify the model.

By contrast, a Foster model is used to calculate the junction temperatures of paralleled chips, and the coupling effect between chips should be considered to improve the accuracy of the model. The thermal coupling impedances [7] are introduced to characterize the multi-thermal coupling, and the improved Foster model of press-pack IGBT is shown in Fig.10. In this proposed model, the coupling effect of chip k on the junction temperature of chip 1 is represented by a thermal coupling impedance Z_{1k} in parallel with a power source P_k. The junction temperature of chip k considering coupling is determined by

$$\begin{aligned} T_{jk} &= \sum_{\substack{i=1 \\ i\neq k}}^{n}\left(Z_{th,ki}P_i\right)+Z_{thk,j-c}P_{k,j-c}+Z_{th,c-a}\sum_{i=1}^{n}P_{i,j-c}+T_{amb} \\ &= \sum_{\substack{i=1 \\ i\neq k}}^{n}\left(Z_{th,ki}P_i\right)+Z_{thk,j-e}P_{k,j-e}+Z_{th,e-a}\sum_{i=1}^{n}P_{i,j-e}+T_{amb} \end{aligned} \tag{2}$$

where $Z_{thk,j\text{-}c}$ and $Z_{thk,j\text{-}e}$ are the junction-case thermal impedance of chip k at collector side and emitter side respectively, $Z_{th,c\text{-}a}$ and $Z_{th,e\text{-}a}$ are the case-ambient thermal impedance on the two sides. $P_{i,j\text{-}c}$ and $P_{i,j\text{-}e}$ are the part of power loss of chip i dissipated from the collector side and the emitter side respectively.

B. Extraction of Thermal Network Model Parameters Based on FE Method

Since the junction temperature distribution in a press-pack IGBT can be obtained by FE modeling, the parameters of the linear proposed Foster model, including the junction-case thermal impedances and the coupling thermal impedances, can be extracted by superimposition using transient FE method.

For example, by applying the power loss P_k to chip k alone, and extracting the junction temperature of chip k, chip i and case temperatures of the device from the FE model results, the transient junction-case thermal impedances of chip k ($Z_{thk,j\text{-}c}$, $Z_{thk,j\text{-}e}$) and the transient thermal coupling impedance between chip k and chip i ($Z_{th,ik}$) can be acquired using the equations (3) and (4).

$$Z_{thk,j-c}(t)=\frac{T_{jk}(t)-T_{case(c)}(t)}{P_{k,j-c}} \tag{3}$$

$$Z_{th,ik}(t)=\frac{T_{ji}(t)-T_a}{P_k} \tag{4}$$

where T_{jk} and T_{ji} are the junction temperatures of chip k and chip i when the power loss P_k is applied to the chip k, $P_{k,j\text{-}c}$ is the power loss of chip k dissipated from the collector side.

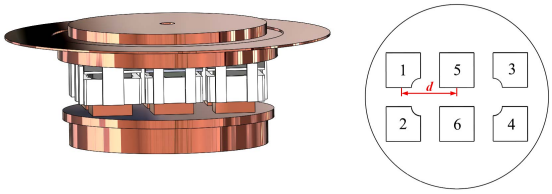
The parameters of the proposed thermal network are determined by fitting transient thermal impedance curves according to equation (5).

$$Z_{th}(t)=\sum_{i=1}^{n} R_{th,i}\left(1-e^{-t/\tau_{th,i}}\right), \qquad \tau_{th,i}=R_{th,i}C_{th,i} \tag{5}$$

where n is the order of fitting model, τ_{th} is the time constant. The junction-case thermal impedances are assumed in this study to be 3rd order both on the collector side and emitter side here, while the thermal coupling impedance and the case-ambient thermal impedance are 1st order and 2nd order respectively.

Although the parameters of the proposed model can be obtained by solving a series of FE models and curve fitting the transient thermal impedance, for a high power device having dozens of chips, the calculation demand is considerably high. Assuming that there are n chips in a device, the FE model needs to be solved n times to extract n junction-case thermal impedances and n^2-n thermal coupling impedances. This can be quite demanding in practice.

In order to compute more efficiently, firstly, the number of simulations and parameters can be at least halved, since the layout of press-pack IGBT device is usually axisymmetric in one dimension or another. Then, because the coupling thermal impedance depends on distance between chips in concern [7], the coupling impedance can be considered as a function of the chip distance, thus if there are k types of chip distances (including the position effects) in an n-chip power module, the number of coupling impedances need to be calculated can be reduced from n^2-n to only k. Besides, junction-case transient thermal impedances of different IGBT chips can be considered to be the same, since each IGBT submodule has the same geometry structures and packaging materials. This is also true for the FRD chips. Thus the junction-case thermal impedances of IGBT and FRD chip only need to be calculated once respectively.



(a)Schematic diagram (b)Inner layout

Fig. 11 3300V/200A press-pack IGBT/FRD

A commercially available 3300V/200A press-pack IGBT/FRD module shown in Fig. 11 is adopted here to illustrate the extraction of thermal parameters using the FE simulation results. The device has four 3300V/50A IGBT chips numbered as 1-4 located at the corners, and two 3300V/100A FRD chips numbered as 5-6 located in the center. There are four kinds of chip distances in this device, i.e. d, $\sqrt{2}d$, $2d$, $\sqrt{5}d$, assuming the distance between chips 1 and 5 is d.

The FE model of the 6-chip device is built using the modelling method proposed in sections II and III, under the clamping force of 7.2kN. The FRD chip is divided into termination and diode regions, and the latter is the heat source of the chip. By applying the power loss to chip 1 and 5 respectively, extracting the junction temperatures of 1-4 and 5 correspondingly, and fitting the transient thermal impedance curves, the parameters of the proposed network can be finally obtained, as shown in TABLE. III and TABLE. IV.

TABLE III. JUNCTION-CASE THERMAL IMPEDANCES(@7.2KN)

Collector side *i*	**IGBT**		**FRD**	
	$R_{th,i}$ (°C/W)	$C_{th,i}$ (J/°C)	$R_{th,i}$ (°C/W)	$C_{th,i}$ (J/°C)
1	0.092	0.157	0.098	0.146
2	0.192	1.048	0.190	1.188
3	0.082	22.573	0.043	35.695
Emitter side *i*	**IGBT**		**FRD**	
	$R_{th,i}$ (°C/W)	$C_{th,i}$ (J/°C)	$R_{th,i}$ (°C/W)	$C_{th,i}$ (J/°C)
1	0.190	0.082	0.192	0.080
2	0.387	0.620	0.376	0.724
3	0.196	15.351	0.103	36.962

TABLE IV. COUPLING THERMAL IMPEDANCES(@7.2KN)

Chip distance	R_{th} (°C/W)	C_{th} (J/°C)
d	0.111	99.955
$\sqrt{2}d$	0.091	148.999
$2d$	0.084	178.087
$\sqrt{5}d$	0.079	197.850

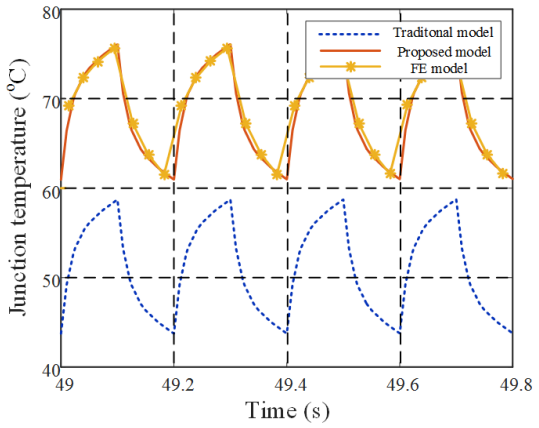
C. *Simulation Verifacation*

In order to verify the validity of the proposed thermal network model, the simulation results of traditional Foster thermal network without considering coupling are compared with the proposed model and FEM, under power cycling condition. The cycling test period and switching period of the device are both 0.2s, and the duty ratio is 0.5. Since the switching frequency here is rather low, the switching loss of the device is omitted, and the power loss for each IGBT chip is the nominal conduction loss 160W at room temperature. The thermal resistances and thermal capacitances in 2nd case-ambient transient thermal impedance $Z_{th,c\text{-}a}$ and $Z_{th,e\text{-}a}$ are shown in TABLE. V. The ambient temperature is 20°C.

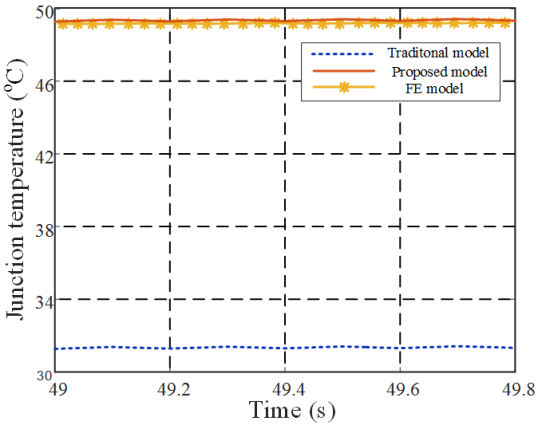
TABLE V. CASE-AMBIENT THERMAL IMPEDANCES

Collector side *i*	$R_{th,i}$ (℃/W)	$C_{th,i}$ (J/℃)
1	0.064	134.227
2	0.092	150.439
Emitter side *i*	$R_{th,i}$ (℃/W)	$C_{th,i}$ (J/℃)
1	0.249	51.877
2	0.020	56.021

The junction temperatures of IGBT chip 1 and FRD chip 5 calculated with two thermal models and FE model are shown in Fig.12, when the device reaches the thermal steady state. The comparison shows good agreement between the proposed thermal model and FE model, and the maximum/minimum junction temperatures obtained by improved the Foster model are about 17.2 ℃ and 17.8 ℃ higher than traditional model for IGBT chip 1 and FRD chip 5 respectively. This big difference means that the thermal coupling between chips has indeed a great influence on the magnitude of chip junction temperature, and the proposed Foster model is more suitable for calculating the junction temperature distribution inside a multichip device.



(a) junction temperature of IGBT chip 1



(b) junction temperature of FRD chip 5

Fig.12 Junction temperatures of different thermal models and FEM

V. CONCLUSION

The conduction voltage distribution of IGBT chip is uneven actually, resulting in an uneven distribution of heat source within the chip. The power loss distribution inside an IGBT chip affects the prediction of not only the chip temperature distribution but also the junction-case thermal resistance significantly. Therefore, it is necessary to consider the structure and loss distribution of IGBT chips to improve the accuracy when building the FE model of press-pack device.

In a multichip press-pack IGBT device, since the paralleled chips share the collector and emitter poles, thermal coupling exists between the chips and needs to be considered in model extraction. An improved Foster model considering the thermal coupling effect is proposed and derived using a series of transient FE simulation results. Since the thermal model in datasheets cannot be used to obtain the junction temperatures of all chips, the proposed thermal model can be used to calculate the chip temperature distribution inside the multichip device under different working conditions, which contributes to analysing the reliability of press-pack IGBT devices.

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