Modeling the Gate Driver IC for GaN Transistor: A Black-Box Approach

Ruiliang Xie[1, 2], Guangzhao Xu[1], Xu Yang[1], Gaofei Tang[2], Jin Wei[2], Yidong Tian[1], Feng Zhang[1], Wenjie Chen[1], Laili Wang[1], and Kevin J. Chen[2]

1. School of Electrical Engineering, Xi'an Jiaotong University, Shaanxi, Xi'an, China;

2. Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Kowloon, Hong Kong, China.

***Abstract*—During the switching performance evaluation for Si-based power devices, the gate driver IC's are commonly neglected because of Si device's slow switching speed. GaN transistors, with much smaller intrinsic capacitances, would enable faster switching speed and higher switching frequency. Consequently, the gate driver would largely impact the switching performance as well as the dead-time of the GaN transistor. In previous works, however, the gate driver IC used to drive GaN transistor have been ignored in circuit simulation, leading to lower modeling accuracy. In consideration of the lack of gate driver IC's critical design parameters, along with less familiarity of power electronics engineer/researcher with the semiconductor technologies, the gate driver IC could be regarded as a "black-box". Despite the difficulty in directly performing measurements inside the driver chip package, a black-box modeling method could be proposed. Based on the measured terminal current/voltage signals in a typical gate drive scheme, the I-V characteristics of the PMOS in the totem-pole topology could be extracted. With respect to the C-V curves, the characteristics of a discrete Si MOSFET with comparable voltage/current rating could be introduced. Taking into account the operating principle of the totem-pole topology, a circuit-level model could be established. Consequently, the simulated waveforms are in reasonable agreements with the testing results. Taking advantages of the proposed black-box modeling method, the switching transient waveforms as well as the dead-time of GaN transistor could be more accurately evaluated.**

Keywords—gate driver IC; GaN transistor; black-box approach; modeling.

I. INTRODUCTION

After several decades of intensive development, the mainstream Si-based power devices (IGBT, MOSFET, etc.) are quickly reaching their fundamental material limits. In next-generation power converters, the Gallium Nitride (GaN) power devices, which enable much faster switching speed, higher frequency (i.e. short dead-time) and lower loss, would be competitive candidates. Due to the large input capacitance (C_{iss}) of Si devices, the gate driver integrated circuit (IC) is commonly neglected in the switching transient analysis or loss evaluation [1]. On the contrary, the GaN transistor with much smaller C_{iss} and shorter dead-time could be largely affected by the characteristics of gate driver IC. However, in previous works associated with switching performance or loss analysis of GaN transistor, the gate drive schemes have not been taken into full account [2], [3]. Consequently, the modeled results of those analyses would exhibit dissatisfactory accuracy.

Besides, the researchers/engineers specializing in power electronics would not be that familiar with the semiconductor technologies (such as the integrated circuits design and the CMOS fabrication technology). In consideration of the critical design parameters reserved by the manufacturer, the gate driver IC could be regarded as a "black-box". Thus, it would be more difficult for the power electronic researcher/engineer to establish analytical model for gate driver IC and carry out accurate simulation for GaN transistor.

In this work, a black-box modeling method would be proposed to extract the characteristics of PMOS and NMOS in the totem-pole topology in a driver IC. Despite the obstacles encountered when performing measurements inside the driver chip package, the I-V characteristics of the PMOS could be extracted from the source/sink current and the output voltage signal in a typical gate drive scheme. The C-V curves associated with PMOS and NMOS could be approximated by the characteristics of a discrete Si MOSFET with comparable voltage/current rating. After taking the operating principle of the totem-pole topology in the driver IC into consideration, the circuit-level model compatible with different gate drive schemes could be established.

The proposed black-box gate driver IC model is then implemented to a double pulse testing platform with GaN transistors. In comparison with the experimental results and the waveforms simulated by the previously reported modeling approaches, the switching transient waveforms as well as the dead-time of GaN transistor could be more accurately evaluated by the proposed modeling method.

II. The Modeling Principle for Gate Driver IC

The totem-pole gate driver IC LM5114 from Texas Instruments that is commonly used in GaN-based applications would be selected as the study object. The source and sink currents of the driver could be conducted by the PMOS and NMOS separately. Since the size of PMOS would be significantly smaller than that of NMOS [4], the charging current would be limited and the turn-on performance of GaN transistor could be largely affected. Thus, the turn-on process (i.e. the turn-on of PMOS) would be focused in this study.

Although the topology is confirmed, without the exact design parameters and with the difficulty in measuring inside the chip package, the gate driver IC would still be regarded as a "black-box". A gate drive scheme is designed to test the terminal current and voltage signals, as shown in Fig. 1(a). To exclude the effect of channel's formation, a capacitor rather than a GaN transistor is mounted at the output of gate driver IC. The equivalent circuit along with the definitions of variables are depicted in Fig. 1(b).

Through measuring the voltage signal on the gate resistance, the current of PMOS I_p could be acquired and accurately fitted by piecewise equation (1) – (2), as plotted in Fig. 1(c). Likewise, the output current of the driver IC could be extracted from the difference between I_p and the displacement current of NMOS I_n, whose testing and fitting results are depicted in Fig. 1(d). Equations (3) – (5) denote the piecewise fitting principle for output voltage V_o. Good agreements could be reached, as shown in Fig. 1(e). The source-to-drain voltage of PMOS V_p could be derived by (6), whose time-domain waveform is depicted in Fig. 1(f).

$$I_{p1} = A_1(e^{-\alpha_1(t-t_1)} - e^{\alpha_1 t_1}) \tag{1}$$

$$I_{p2} = A_2\sin(\omega_2 t)e^{-\alpha_2 t} + A_3\sin(\omega_3 t)e^{-\alpha_3 t} + A_4\sin(\omega_4 t)e^{-\alpha_4 t} \tag{2}$$

$$V_{o1} = \frac{A_5\omega_5 + B_5\alpha_5}{C_o(\alpha_5^2+\omega_5^2)}[1-\cos(\omega_5 t)e^{-\alpha_5 t}] + \frac{B_5\omega_5 - A_5\alpha_5}{C_o(\alpha_5^2+\omega_5^2)}\sin(\omega_5 t)e^{-\alpha_5 t} \tag{3}$$

$$V_{o2} = \frac{A_6}{C_o\alpha_6}e^{-\alpha_6(t-t_6)} + V_1 \tag{4}$$

$$V_{o3} = \sum_{i=7}^{9}\frac{A_i\omega_i}{C_o(\alpha_i^2+\omega_i^2)}[1-\cos(\omega_i t)e^{-\alpha_i t}] - \frac{A_i\alpha_i}{C_o(\alpha_i^2+\omega_i^2)}\sin(\omega_i t)e^{-\alpha_i t} \tag{5}$$

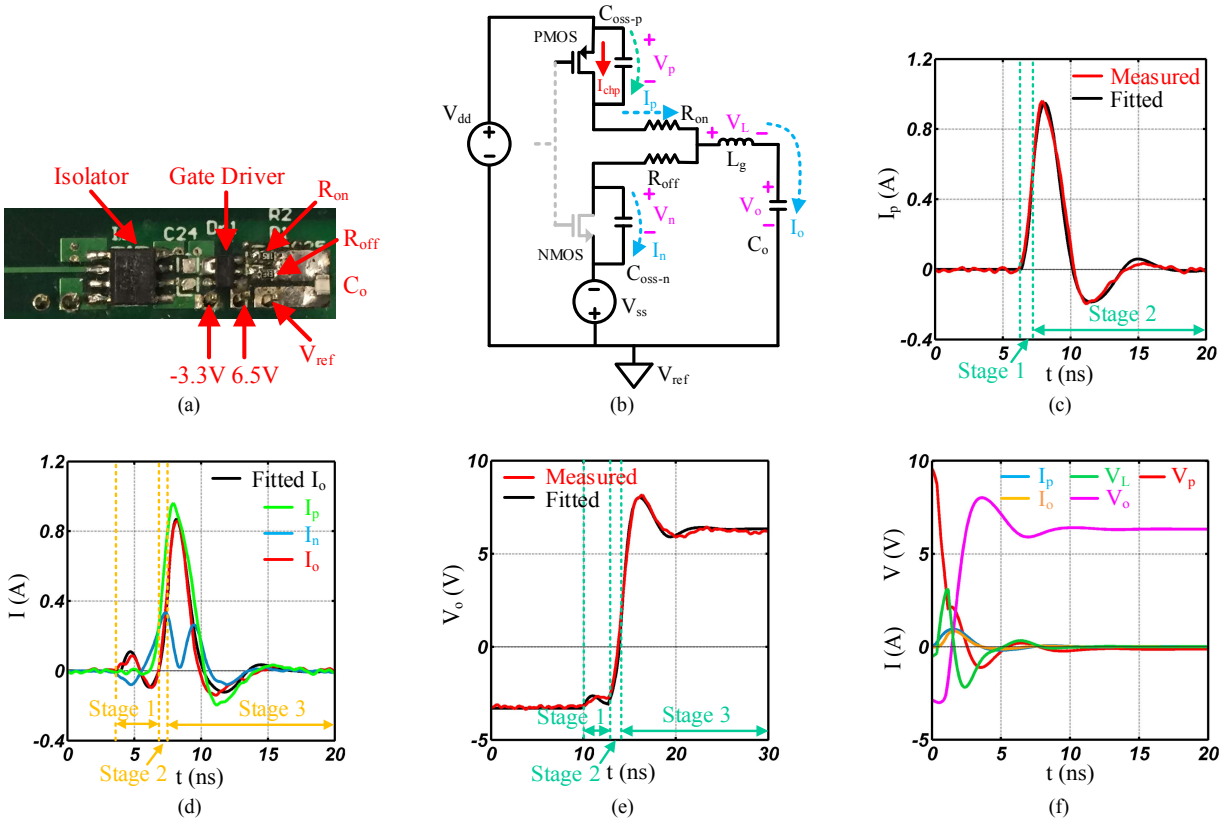


Fig. 1. (a) The gate drive scheme for waveform measurements; (b) The equivalent circuit along with the definitions of variables; (c) Comparison between the measured and fitted current of PMOS I_p; (d) Comparison between the measured and fitted output current I_o; (e) Comparison between the measured and fitted output voltage V_o; (f) The extracted waveforms of source-to-drain voltage of PMOS V_p and the voltage drop on L_g V_L.

$$V_p = V_{dd} - V_o - V_L - I_p R_{on} \quad (6),$$

where α_1~α_9, A_1~A_9, ω_2~ω_9, t_1, V_1, and C_0 are constants.

$$C = \sum_n A_n \log\left[1+\exp\left(-V_{ds}+V_n\right)\right] + \sum_m B_m \exp\left[\left(V_{ds}-V_m\right)^2 / 2\sigma^2\right] + C_{10} \quad (7)$$

$$C_{ossp} = R_{on\text{-}p} C_{oss\text{-}M_1} C_{ossn} / R_{on\text{-}n} C_{oss\text{-}M_1} = R_{on\text{-}p} C_{oss\text{-}M_1} Q_{ossn} / R_{on\text{-}n} Q_{oss\text{-}M_1} \quad (8)$$

$$I_{chp} = I_p - C_{ossp} dV_p / dt \quad (9)$$

$$\begin{cases} if \quad V_p \ge \left(V_{sgp} - V_{th}\right) \\ \quad I_{chp} = \beta\left(V_{sgp} - V_{th}\right)^2 \left(1+\lambda V_p\right) \\ \quad\quad * M_1\left[1-\exp\left(-M_2 V_{sgp} - M_3\right)\right] \\ if \quad V_p < \left(V_{sgp} - V_{th}\right) \\ \quad I_{chp} = \beta\left[2V_p\left(V_{sgp} - V_{th}\right) - V_p^2\right]\left(1+\lambda V_p\right) \\ \quad\quad * \left\{\left(M_4 + V_{sgp}^{M_5}\right) / \left[M_6\left(V_{sgp} - V_{th}\right) - V_p\right]\right\}^{P_1} \\ P_1 = \frac{1}{\pi}\arctan\left[-M_7\left(V_p - M_8 V_{sgp}\right)\right] + \frac{1}{2} \end{cases} \quad (10),$$

where A_n, V_n, B_m, V_m, C_{10}, β, λ and M_1~M_8 are constants.

For the purpose of capacitance approximation, a discrete Si MOSFET (IRLML5103TRPBF-1 from IR, denoted as M_1) with comparable voltage rating and R_{on} to the NMOS in the driver IC could be introduced. In combination of the logarithm functions and multiple Gaussian distribution functions, the intrinsic capacitances of M_1 could be modeled by (7). As described in [5], the intrinsic capacitances and charges would be directly proportional, while the R_{on} would be inversely proportional to the size of device. Thus, the output capacitance C_{ossp} of PMOS could be derived by (8). To obtain the load line associated with PMOS's turn-on process, equation (9) is established. As expressed in (10), the corrections could be made to the classic I-V equations according to the load line. Satisfactory accuracy and continuity could be reached in the I-V modeling for the PMOS in the driver IC, as depicted in Fig. 2(b) and (c). With respect to the buffer, a resistance declining with the time could be introduced [6].

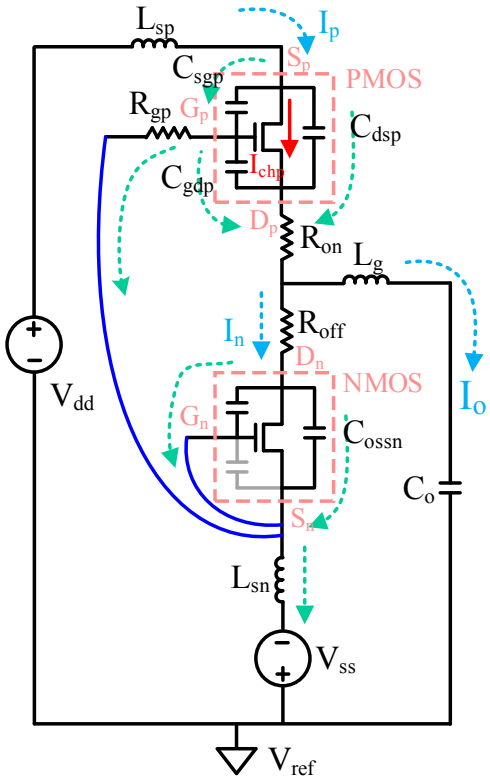


Fig. 3. The equivalent circuit for establishing the circuit-level model.

Figure 3 depicts the equivalent circuit for establishing the circuit-level model. Unlike the bridge-leg circuit analyzed in previous works [2], the gate-drive and the "power stage" of the IC are supplied by the same power source, according to

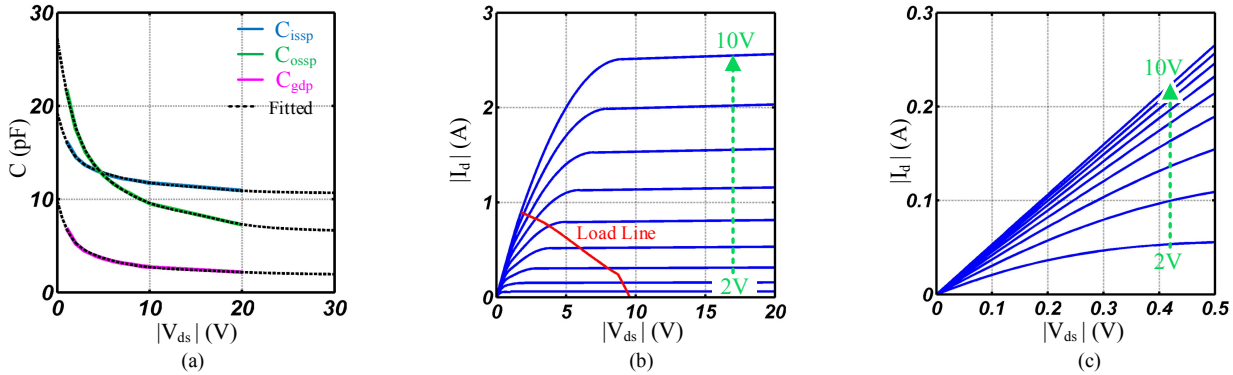
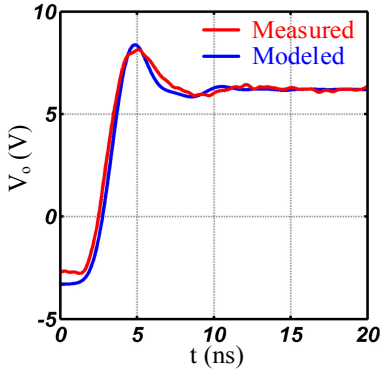


Fig. 2. (a) The approximation for intrinsic capacitances of PMOS and the corresponding modeled results; (b) The modeled I-V characteristics in contrast to the turn-on load line of PMOS; (c) The modeled linear region of the I-V characteristics of PMOS.

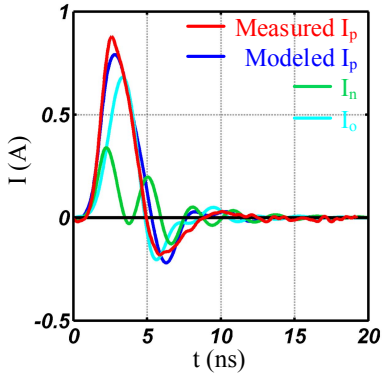
driver IC's operating principle. Through deriving the KCL and KVL equations and sorting them into a 6x6 matrix, the iterative computation could be carried out. Consequently, although the gate driver IC would exhibit as a "black-box", the proposed modeling method could approximate the relevant device characteristics inside the chip package and simulate the switching transient waveforms associated with the GaN transistor.

III. Experimental Results and Comparison with Other Models

The simulated current and voltage signals associated with Fig. 1(a) are presented in Fig. 4(a) and (b). Reasonable agreements could be reached between the simulation and measurement. The black-box modeling method is then implemented to a double pulse tester with 650V/30A from GaN Systems. For comparison purpose, the device model in [3] could be improved, such that only the influence of driver IC would be emphasized. As plotted in Fig. 5(a) and (b), compared with the model without gate driver, under 300V/6A condition, the V_{gs} and I_d waveforms simulated by the proposed modeling method would exhibit improved accuracy. Besides, a 3.3ns difference in dead-time (T_d) could be found as well, which would be non-negligible in consideration of the T_d less than 50ns for GaN transistor.

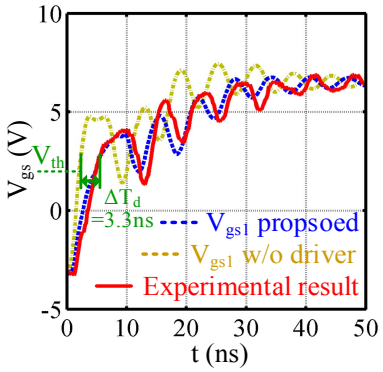


(a)

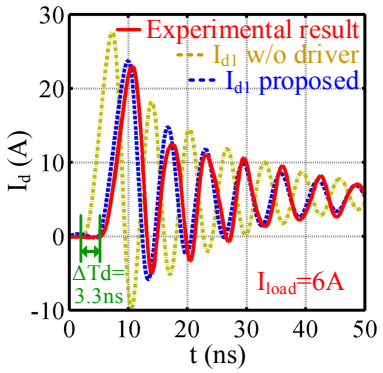


(b)

Fig. 4 (a) Comparison between the measured and simulated output voltage V_o; (b) Comparison between the measured and simulated current of PMOS I_p.



(a)



(b)

Fig. 5 (a) Comparison of V_{gs} of GaN transistor among the experiments, the model w/o gate driver, and the proposed model; (b) Comparison of I_d of GaN transistor among the experiments, the model w/o gate driver, and the proposed model.

IV. Conclusion

A black-box modeling method for the gate driver IC used to GaN transistor is proposed. Despite the critical design parameters reserved by the manufacturer and the difficulty in directly performing measurements inside the chip package, the device characteristics in the totem-pole topology of IC could be extracted from terminal measurements. Compared with the modeling approach that ignores the driver IC, the proposed model would exhibit improved accuracy. With respect to the power electronics researcher/engineer that could be less familiar with semiconductor technologies, the black-box modeling method would be helpful in more accurately evaluating the switching transient performance as well as dead-time of GaN transistor. The further work would be focused on the switching loss and dead-time evaluations in combination with GaN transistor's particularity (e.g. reverse conduction and V_{th} instability).

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