

A New Electronic Design Automation Tool for the Optimization of PwrSoC/PwrSiP DC-DC Converters

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Abstract— With the advent of PwrSoC/PwrSiP systems comes a wide range of process variables which the designer is required to optimize. However, as the number of parameters increases, so too does the complexity of the design. If active and passive components are not optimized in unison the advantages these highly integrated systems bring are negated. Considering this, the need for an intuitive design tool for the practicing engineer to quickly analyze a range of potential system configurations and find the Pareto optimal design with ease is clear.

In this paper we present a new Electronic Design Automation (EDA) package, the Ferrochip Design Studio for the co-optimization of DC-DC converter systems, primarily for PwrSoC and PwrSiP systems using thin film integrated magnetics. We discuss its constituent parts as well as presenting the design flow used by the tool. Finally small signal measurement results are presented and compared to the analytical results generated by the design studio.

Keywords— EDA, PwrSoC, PwrSiP, Design, Thin film magnetics, IVR, Modeling, Optimization

I. INTRODUCTION

As the use of highly integrated DC-DC converters in heterogeneous on die and package increase [1-3], there exists a need for the co-optimization of both the active and passive components to realize a fully optimized system.

One of the main advantages of PwrSoC (Power Supply on Chip) and PwrSiP (Power Supply in Package) DC-DC converters is the ability to control many of the semiconductor, magnetic and capacitive component process variables [4, 5], allowing for the optimization of converters for specific applications. This flexibility has previously not been available with designers constrained to using discrete semiconductor and passive components [6] with standardized values. While this typically resulted in straightforward design approaches for switching frequencies of less than 1 MHz in the past, the same approaches are not possible as switching frequencies are pushed above 20-100 MHz. The new degrees of freedom afforded by PwrSoC/PwrSiP DC-DC converters on die and package mean more complex design approaches are necessitated to realise highly integrated and efficient power converters.

While there are a number design methods [5, 7-9] available for thin film components using magnetic materials, there is no commercial tool available which combines a number of magnetic structures into one design environment, allowing for easy comparison of structures and circuit topologies.

For the practicing engineer there are a wide variety of optimization routes available, whether it's analytical, semi-empirical, finite element analysis or using combination of all, there are multiple avenues to the optimum design. However, it is critical that the correct approach is chosen to strike a balance between time and accuracy to maximise return on investment.

One common finite element analysis approach in the semiconductor industry for the iterative design of magnetic components is Method of Moments (MoM) or Fast Multipole Method (FMM) [10, 11]. These methods allow for rapid simulation of multiple designs in cases where the structures and materials are planar and homogenous. However, in cases where some materials are non-linear (e.g. magnetic material) the benefits of MoM and FMM is nullified as additional computation is required which renders these solvers unsuitable for devices with magnetic materials.

More traditional approaches using Finite Element Methods etc. are adept at solving complex three dimensional structures but the time required to solve them is significant and doesn't lend itself easily to a design approach involving multiple variables. The Ferrochip Design Studio uses analytical models which are validated using Finite Element Analysis (FEA) and measurement to allow for rapid optimization of the power supply system and its constituent parts.

While the magnetics design is important, consideration must also be given to the semiconductor node and process to realise an efficient power supply. There are a number of methodologies for optimising semiconductors ranging from basic scaling [9] of the MOSFET channel to extracting energy loss functions from discrete SPICE simulations [5], to simulation of the circuit in a SPICE simulator and adjusting the MOSFET sizes accordingly. Basic scaling shows general trends but lacks the accuracy needed to optimise a full system. The gold standard for accuracy prior to fabrication is to carry out SPICE simulations of the complete system, however this is time consuming and the number of parameters to be optimised mean this method is typically only used for minor design

adjustments. The multiple SPICE MOSFET level models available (>50) mean that developing a one size fits all approach is difficult if not impossible due to proprietary models etc. The Ferrochip Design Studio integrates a SPICE simulator for MOSFET modelling to extract parameters which represent its behaviour analytically. It can be used with most common compact SPICE MOSFET levels used in industry such those from the BSIM group at UC Berkeley [12, 13]. This approach allows the MOSFETs to be optimized while also accounting for short channel effects.

The optimization of a PwrSoC/PwrSiP converters requires multiple objectives to be satisfied such as area, current/voltage ripple and loss to name but a few. To fully leverage the design flexibility afforded by these highly integrated systems on die and package, the magnetic, semiconductor and capacitor components must be optimised simultaneously. This tool allows for the co-optimization of DC-DC converter systems with a focus on the magnetic component, which is typically the most difficult component to realize.

Key to optimising a system is the users understanding of the key factors affecting performance and the correlation between them. The Studio allows sweeping of parameters as well as algorithm aided parameter optimization. Sweeping design variables allows the designer to see at a high level the major factors affecting the performance of the power converter. However, as there are a considerable number of design variables it can be difficult to extract causality between design parameters for novice engineers. It is therefore important for the designer to be able to find the optimum design while also affording the possibility of sweeping design variables. The Design Studio addresses these issues by allowing the designer to select from a number of design constraints such as fixed, range, and sweep. This allows designers to investigate the underlying factors affecting device and converter performance while knowing that neglected parameters will be automatically optimised. In this way the Ferrochip Design Studio allows users at the interface of power converter and integrated circuit design to realise highly optimised PwrSoC/PwrSiP system with little effort.

The wide variety of magnetic component structures and semiconductor processes available means significant time is required to fully evaluate systems without a dedicated Electronic Design Automation tool. In this paper we describe some of the main aspects of the tool which are required to realize such a system. In section II the Design Studio components are discussed. Section III provides an overview of the typical design flow and finally conclusions are drawn in section IV.

II. SYSTEM COMPONENTS

A. Optimization Algorithm

The large number of variables for the co-optimization of semiconductor and passive components in a DC-DC converter means that simply sweeping parameters and evaluating their performance will at the very least be time consuming and at worst result in suboptimal converter performance. Considering this and the vast array of semiconductor processes, magnetic

materials and structures available, the design challenge is almost unsurmountable using traditional design approaches.

A wide variety of algorithms are available for such multi-objective constrained problems with all having advantages and disadvantages. In this section we give a brief outline of three potential algorithms; pattern search, particle swarm and differential evolution optimization.

The three algorithms are used to maximize the full load efficiency of a Buck converter with an elongated spiral inductor [14] with the circuit specification provided in Table I. The MOSFETs are designed for a 180 nm process.

TABLE I. CIRCUIT SPECIFICATION

| - | Parameter | Unit | Value |
|-----------------|------------------------------------|------------------|-------|
| V_{in} | Input Voltage | V | 4.2 |
| V_{out} | Output Voltage | V | 1.8 |
| I_{dc} | Output Current | A | 1 |
| Δ/I_{dc} | Phase Ripple Current over I_{dc} | $A_{p,p}/I_{dc}$ | 40% |

Table II sets out the design variables which have been chosen to optimise simultaneously. The MOSFET model and its implementation in the system optimisation flow is explained in the sub-section B.

TABLE II. OPTIMIZATION DESIGN VARIABLES

| | Parameter | Unit | Min. | Max. |
|----------|--------------------------------|---------------|------|------|
| Inductor | Phase Ripple Current/ I_{dc} | % | 0 | 40 |
| | Area | mm | 2 | 4 |
| | Saturation | T | 0 | 1.5 |
| | Number of Turns | - | 2 | 6 |
| | Winding Width | μm | 30 | 150 |
| | Core Thickness | μm | 2 | 6 |
| MOSFET | NMOS Channel Width | mm | 0.1 | 10 |
| | PMOS Channel Width | mm | 0.1 | 10 |
| | NMOS Driver Taper | - | 3 | 15 |
| | PMOS Driver Taper | - | 3 | 15 |
| | NMOS P/N Driver Ratio | - | 1 | 3 |
| | PMOS P/N Driver Ratio | - | 1 | 3 |

For this optimization there are a total of 12 independent variables to solve with a multi-objective problem to maximise full load efficiency. The optimization objective minimizes an error function which considers converter power loss, inductor saturation, device area and current/voltage ripple requirements. Table III presents the median and standard deviation across a sample of 10 runs of the multi-objective problem described.

TABLE III. ALGORITHM COMPARISON

| Optimization Algorithm | Error (Median) | Error (Std. Deviation) | Iterations (Median) | Time (s) (Median) |
|------------------------|----------------|------------------------|---------------------|-------------------|
| Pattern Search [15] | 0.188 | 0.0031 | 28 | 1.5 |
| Particle Swarm [16] | 0.1397 | 0.0064 | 53 | 11.5 |
| Diff. Evolution [17] | 0.1402 | 0 | 188 | 138.4 |

As can be seen from Table III the Hooke and Jeeves pattern search method [15] has the largest error but also converges in the shortest amount of time. The Particle Swarm [16]

Optimization (PSO) using a swarm size of 100 solves in approximately 11.5 s with the lowest error function value of all three. Using the PSO algorithm the Design Studio predicts an overall converter efficiency of 90.1% for this case. The Differential Evolution [17] while also a population based algorithm takes a significantly longer time to converge compared to the PSO algorithm for this problem.

The Ferrochip Design Studio uses a derivative of a population based algorithm to optimize the multi-objective problem which offers improved performance over the given algorithms in Table III. It first calculates a random set of potential solutions within the design space, then each solution is evaluated with respect to an internal error function. The best performing solutions are then stored and another set of solutions are evaluated with respect to the previous results. The steps are repeated until Pareto optimal front is found.

B. Semiconductor Models

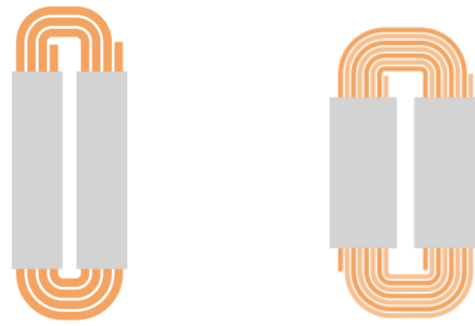
Accurate analytical models for semiconductor devices and passive components form the basis of the Design Studio. For accurate semiconductor performance estimation the SPICE model provided by the foundry must be used as it considers short channel effects which are sometimes ignored in analytical loss estimation [18]. The Design Studio has a built-in SPICE engine to handle parameter extraction from common compact MOSFET models such as those from the BSIM group at UC Berkeley e.g. BSIM3 [13] and BSIM4 [12]. The extracted device parameters are then optimized along with the required magnetic and capacitive components using the optimization algorithm discussed previously. The ability of the Ferrochip Design Studio to extract the required semiconductor parameters is paramount as it reduces the risk of user error, while, at the same time speeding up analysis and increasing model accuracy.

C. Magnetics

The magnetic component has a significant influence on the overall performance of the converter as well as being arguably the most difficult component to model. It is therefore important to accurately represent the electrical model of the magnetic component while also enabling creation of industry standards outputs such as SPICE and GDSII (a 2D layout file type) files for the optimized design.

A wide range of structures such as elongated spiral, solenoid, toroidal inductors as well as their coupled inductor and transformer counterparts are available for designers to choose from in the Ferrochip Design Studio. These structures cover the majority of applications in this space. Various magnetic materials can be easily implemented in the tool in order to investigate their impact on device performance. The Design Studio includes all major magnetic device characteristics of interest such as AC inductance, magnetic core saturation, winding loss, eddy current and hysteresis core loss in analytical models which have been validated by Finite Element Analysis and experimental measurements.

Two structures have been optimized using the Design Studio and fabricated. The GDSII layouts are shown below in Figure 1.



a) Elongated spiral inductor. b) Elongated spiral transformer.

Figure 1. Device structures automatically generated using the Ferrochip Design Studio (not to scale).

Figure 1 a) shows a 4 turn inductor in a 2.5 mm² area with a target inductance of 140 nH. Figure 1 b) shows a 1:1 transformer in a 3.8 mm² footprint area. The primary winding width is 40 μm and has 4 turns.

Measurement results of the elongated spiral inductor are presented below in Figure 2 and Figure 3.

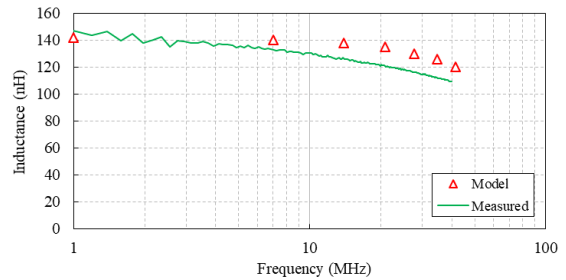


Figure 2. Small signal model versus measured inductance results from 1 MHz to 40 MHz for the elongated spiral inductor.

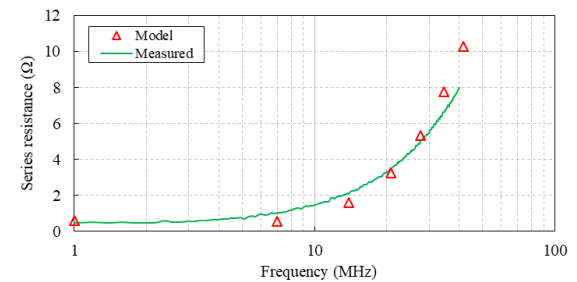


Figure 3. Small signal model versus measured series resistance results from 1 MHz to 40 MHz for the elongated spiral inductor.

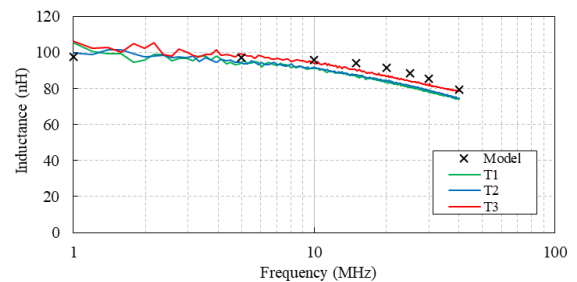


Figure 4. Small signal model versus measured open circuit primary inductance

results from 1 MHz to 40 MHz for 3 prototype transformers.

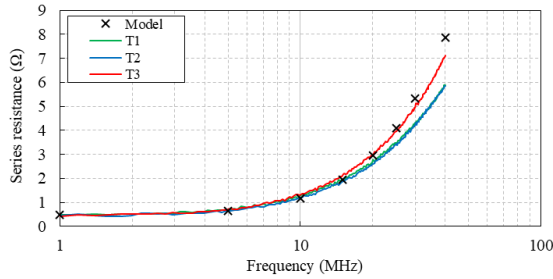


Figure 5. Small signal model versus measured open circuit primary series resistance results from 1 MHz to 40 MHz for 3 prototype transformers.

Figure 4 and Figure 5 show three prototype elongated spiral transformer designs with accompanying model.

Inductor and transformer samples were tested by first attaching and wire bonding each to a PCB board with test pins. The pins are inserted in a fixture which is connected to an impedance analyser and tested up to a frequency of 40MHz. The parasitic impedance of the test fixture, PCB board, test pins and wire bonds is extracted by shorting the test board and carrying out an impedance measurement test. The parasitics are then subtracted from the measurement results in order to get the actual device impedance.

1) GDSII

GDSII is the de-facto standard file format for design exchange in the semiconductor industry. The Design Studio automatically generates foundry compatible files which can be utilized by 3rd party EDA tools. Figure 1 shows GDSII layout images generated from the Design Studio which includes all layers for mask manufacturing.

2) SPICE

One of the most important features of the Design Studio is the generation of frequency dependent SPICE models which considers the impedance characteristics of the magnetic device. A SPICE model has been internally developed which accurately represents the magnetic device at low frequency as well as considering high frequency effects. The Studio can also generate SPICE circuit representations of measured data using a curve fitting algorithm.

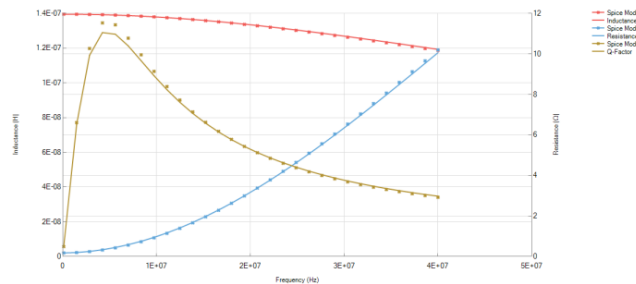


Figure 6. Screenshot from the Ferrochip Design Studio of the generated SPICE model versus the analytical representation of the elongated spiral inductor in Figure 1 a) from 100 kHz to 40 MHz.

D. Capacitors

The Design Studio allows for the optimization of the capacitive components required by each topology. The allowable area is considered as well as the capacitance density, parasitic series resistance and inductance.

III. DESIGN FLOW

A design flow is provided in Figure 7 which highlights the main design stages when optimizing a DC-DC converter for full load efficiency.

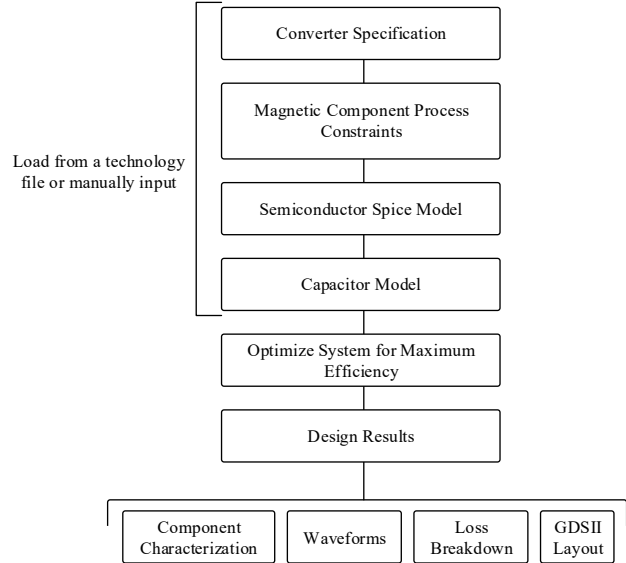


Figure 7. Typical optimization design flow to maximize the efficiency of a DC-DC converter using the Ferrochip Design Studio.

Firstly the user loads or inputs the desired circuit specification using the Design Studios Graphical User Interface (GUI) or via the scripting interface. The magnetic component structure is selected from a device library followed by the loading of the technology files provided by the foundry for the semiconductor and capacitor processes. Once the design space has been setup the Design Studio will optimize the input parameters to attain the Pareto optimal design front.

Once complete, the design results can be viewed at number of levels with varying degrees of detail; from system level efficiency down to the core thickness in an easy to use GUI. Key waveforms are presented along with loss breakdowns and efficiency curves. The GDSII layout file and SPICE model can also be generated for use in conjunction with 3rd party EDA tools. Using the scripting interface the Design Studio can also be integrated into typical IC design flows.

IV. CONCLUSIONS

In this paper we have described the Ferrochip Design Studio, a new Electronic Design Automation (EDA) tool to co-optimize the active and passive components in a PwrSoC/PwrSiP DC-DC converter which utilize magnetic materials. It allows for the complete design of DC-DC

converters, allowing the practicing design engineer to easily find Pareto optimal designs for a given set of constraints. We analyse three optimization algorithms for use when optimizing a DC-DC converter which shows that population based optimization algorithms are good candidates to solve these kinds of problems.

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