Harmonics and Voltage Quality in Post-Fault Reconfigured Multi-Level Inverters

Weiqiang Chen
Department of Electrical & Computer Engineering
University of Connecticut
Storrs, USA
Weiqiang.chen@uconn.edu

Ethan Hotchkiss
Department of Electrical & Computer Engineering
University of Connecticut
Storrs, USA

Ali Bazzi
Department of Electrical & Computer Engineering
University of Connecticut
Storrs, USA

***Abstract*—The main focus of this paper is to investigate the effect of post-fault reconfiguration on the inverter voltage total harmonic distortion in multilevel inverters (MLI). Three different operating conditions are compared: 1) Healthy, 2) Faulty, and 3) Reconfigured using different methods that utilize inherent inverter redundancy. Literature mostly addresses balancing line-to-line voltage RMS when reconfiguring the inverter after fault occurrence, and line-to-neutral voltage and harmonic content after reconfiguration is ignored. However, line-to-neutral voltage quality is essential for per-phase analysis of Y-connected three-phase loads, neutral point power conditioning when the neutral exists, unbalanced loading conditions, and harmonic content analysis required by some grid interconnection standards such as AS4777 and IEEE1547. This paper first introduces an accurate analytical model to analyze the harmonic content of the line-to-neutral voltage. Then, two fault conditions are introduced into the model and verified in experiments. Three popular reconfiguration methods to mitigate these faults are then evaluated to analyze and compare harmonic content and RMS values of the achieved line-to-neutral voltages. Simulation and experimental results of healthy, faulty, and reconfigured conditions show that the predicted RMS and total harmonic distortion of the line-to-neutral voltage using the proposed model are accurate. Results also show that the line-to-neutral voltage is severely impacted by existing reconfiguration methods.**

Keywords—Multilevel Inverter; Power Electronics; Voltage Quality; Fault Reconfiguration; Harmonic Analysis

I. INTRODUCTION

Multilevel inverters (MLIs) have been widely used in the industry for several advantages compared to two- and three-level inverters. These advantages include the ability to sustain higher voltage stress due to their cascaded per-phase structure, lower common-mode voltage, operation under both high frequency switching and lower frequency switching, and lower total harmonic distortion (THD) [1]. Disadvantages also exist including more complex control strategies and more semiconductor devices. The increased number of semiconductor devices increases the risk of failure since the failure of a single device could cause the whole inverter to fail. However, the increased number of semiconductor devices provides an opportunity for redundancy to recover the inverter from faults. Thus, researchers have developed many effective methods to reconfigure MLIs to recover from faults. Redundant switching schemes have been developed to survive a fault by operating the remaining healthy devices [2]-[3], with focus on phase-shifted and phase-disposition methods. Space vector modulation (SVM) is also a popular modulation method, where SVM-control-based fault cell or device bypassing methods have been developed [4]-[5]. Besides control-based reconfiguration, topology modification is also effective to tolerate a fault [6], or to bypass the failed cell or device with a modified control scheme [7]-[8]. For three-phase systems, the common problem when one device fails is that the corresponding leg also fails which can cause unbalanced voltages and currents among phases; a neutral-shifted method was developed to handle unbalanced conditions [3], [9]-[10]. These reconfiguration methods are effective and mature since they balance the three phases at desired RMS values.

Most of the existing reconfiguration methods focus on maintaining the line-to-line voltage waveform intact after reconfiguration of an MLI due to fault occurrence, while sacrificing the line-to-neutral voltage quality. However, RMS value and harmonic content of the line-to-neutral voltage after post-fault reconfiguration is essential in: 1) per-phase analysis of Y-connected loads, 2) unbalanced load conditions with neutral current flow, 3) grid-interconnection standards that limit the line-to-line voltage maximum (e.g. IEEE1547 and AS4777) and thus limit the line-to-neutral voltages indirectly, while limiting harmonics per-phase, and 4) neutral point control and power conditioning. Therefore, the line-to-neutral voltage quality should not be ignored. To analyze the harmonic content of output voltage waveforms in a multilevel inverter, it is common for researchers to use software tools [11] or focus on the low-frequency staircase function to approximate the low-frequency content of SPWM in multilevel inverters [12]. However, a model that includes high-frequency impacts is required for accurate mathematical analysis of MLIs.

The aim of this paper is thus to derive an accurate mathematical model of MLI output voltage to study the impact of different post-fault reconfiguration methods on the line-to-neutral voltage and explore its harmonic content and RMS value. The paper emphasizes that voltage quality improvement should go beyond just maintaining the desired line-to-line voltage shape. This paper provides analysis and comparison of

harmonic content in 1) Healthy, 2) Faulty and 3) Reconfigured conditions. Three popular reconfiguration methods: Two control-scheme modulation methods [2], and neutral point shift method [11] are applied for a 5-level NPC inverter for top side device failure as an example.

II. Mathematical Model Basis

Level-shifted PWM is the basis of the proposed mathematical model. Since the switches on the lower side of a phase leg accept the inverted signal of the top switches, the switching functions of the top switches are sufficient to construct the output of the inverter. For example, in the five-level multilevel inverter in Figure 2, S_1 and S_1', S_2 and S_2', S_3 and S_3', S_4 and S_4' always accept inverted signals. The instantaneous output voltage $V_{out}(t)$ can be written as shown in (1) where V_{in} is the input DC voltage, and $q_i(t)$ is the switching function given by [13] for a single PWM waveform.

$$V_{out}(t)=\sum_{i=1}^{S} q_i(t)\times\frac{1}{S}V_{in} \tag{1}$$

where ω_{switch} is the switching frequency, and d_i(t) is the duty cycle function that is a sinusoid with an offset such as $d(t)=\frac{1}{2}+\frac{1}{2}k\sin(\omega t)$, where k is modulation index. By substituting (2) into (1), the output function is obtained as (3)

Even though the fundamental carrier is a sine wave in level-shifted PWM, the fundamental carriers for the switches are not identical due to the level shift of the triangular waves shown in Figure 1. Figure 1 shows the angle regions of a 5-level case where the resulting PWMs are sent to switches accordingly. The fundamental carrier is assumed to be a sine wave, R_i is the angle region of switch S_i where i=1…S. When S_i switches, S_{i-1}, S_{i-2}, …, S_1 are on and S_{i+1}, S_{i+2}, …, S_S are off.

$$M_i(t)=\begin{cases}\dfrac{Sk\sin(\omega_{out}t)}{2}+\dfrac{S}{2}, R_i\\ i, R_{i+1,i+2,\ldots,S}\\ i-1, R_{i-1,i-2,\ldots,1}\end{cases} \tag{4}$$

$$d_i(t)=M_i(t)-i+1=\begin{cases}\dfrac{Sk\sin(\omega_{out}t)}{2}+\dfrac{S}{2}-i+1, R_i\\ 1, R_{i+1,i+2,\ldots,S}\\ 0, R_{i-1,i-2,\ldots,1}\end{cases} \tag{5}$$

Assume the amplitude of each sawtooth wave in Figure 1 as 1, in general, the fundamental carrier function can be written as (4) where k is the modulation index, ω_{out} is the frequency of fundamental carrier. However, since the duty cycle is always between 0 and 1, the duty cycle functions are obtained by eliminating the offset of fundamental carrier functions as shown in (5). By substituting (5) into (3), the output function becomes (6), where i = 1, 2, …, S. The sine term in (6) can be expended by taking advantage of Bessel functions—assume that $x=\frac{n\pi Sk}{2}, \theta=\omega_{out}t, \alpha=n\pi(\frac{S}{2}-i+1)$, the result is shown in (7). J is the first type Bessel function.

A five-level neural point clamped (NPC) inverter is used as a platform in this paper, and the topology of one phase is shown in Figure 2. Figure 3 shows the simulation result of healthy condition where the waveform is centered around 100V due to having the reference point at the negative DC bus rail in Figure 2. The parameters of the model are set as indicated in Table I and the generated waveform is shown in Figure 4 which implies the similarity to the simulation and experimental waveforms shown in Figures 4 and 5. Table II summarizes the RMS and THD values calculated from the dynamic simulation toolbox and mathematical model. Both RMS and THD values between these two cases are similar.

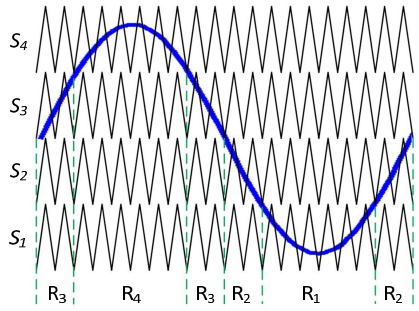

Fig. 1. Phase-shifted PWM of 5-level inverter

$$q_i(t)=d_i(t)+\frac{2}{\pi}\sum_{n=1}^{\infty}\frac{\sin(n\pi d_i(t))}{n}\cos(n\omega_{switch}t), i=1,2,3,\cdots,S \tag{2}$$

$$V_{out}(t)=\frac{1}{S}V_{in}\sum_{i=1}^{S}d_i(t)+\frac{2V_{in}}{S\pi}\sum_{i=1}^{S}\sum_{n=1}^{\infty}\frac{\sin(n\pi d_i(t))}{n}\cos(n\omega_{switch}t) \tag{3}$$

$$V_{out}=(\frac{V_{in}k\sin(\omega_{out}t)}{2}+\frac{V_{in}}{2})+\frac{2V_{in}}{S\pi}\sum_{n=1}^{\infty}\frac{\sin[\frac{n\pi Sk\sin(\omega_{out}t)}{2}+n\pi(\frac{S}{2}-i+1)]}{n}\cos(n\omega_{switch}t), R_i \tag{6}$$

$$\sin\left[\frac{n\pi Sk\sin(\omega_{out}t)}{2}+n\pi(\frac{S}{2}-i+1)\right]=(2J_1(x)\sin(\theta)+2J_3(x)\sin(3\theta)+2J_5(x)\sin(5\theta)+\cdots)$$
$$\times\cos(\alpha)+(J_0(x)+2J_2\cos(2\theta)+2J_4\cos(4\theta)+\cdots)\times\sin(\alpha) \tag{7}$$

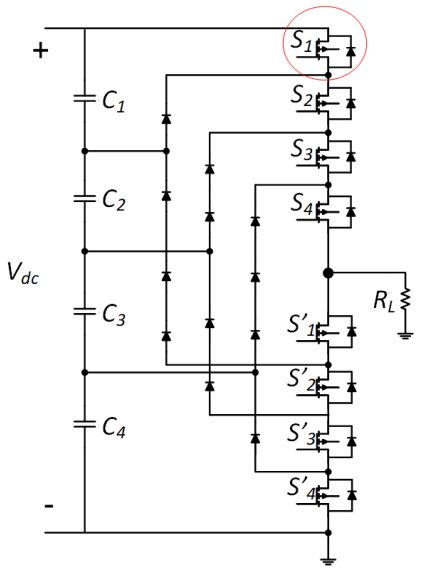

Fig. 2. Single phase of five level NPC inverter

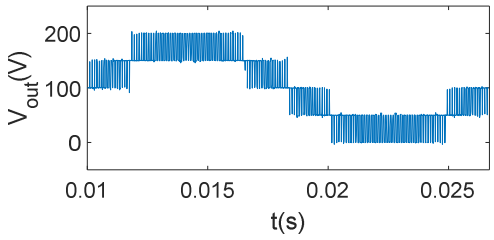

Fig. 3. Waveform generated by mathematical model

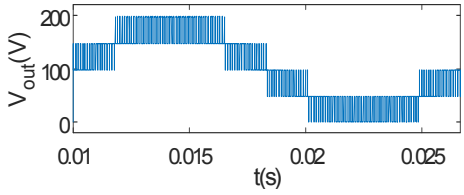

Fig. 4. Dynamic simulation of healthy condition

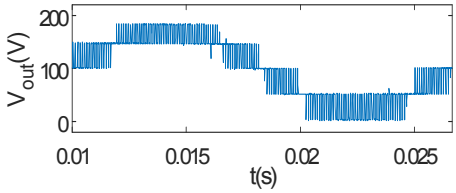

Fig. 5. Experimental result for healthy condition

TABLE I. SYSTEM OPERATING CONDITION

Parameter	Value
DC link voltage	200V
Fundamental frequency	60Hz
Switching frequency	10kHz
Modulation index	0.8

TABLE II. COMPARISON BETWEEN FFT TOOLBOX AND MATHEMATICAL MODEL

	RMS	THD
Mathematical Model	116.55V	39.11%
Dynamic Simulation	114.95V	38.41%
Experimental Result	113.25V	37.22%

III. SIMULATION RRSULTS AND COMPARISON

The 5-level NPC inverter is simulated in MATLAB/Simulink with conditions shown in Table I, and the Fast Fourier Transform (FFT) tool is used to analyze the harmonic content of phase to neutral voltage. Besides the healthy and reconfigured conditions, open circuit (OC) and short circuit (SC) faults are also analyzed and the three conditions are compared in three reconfiguration methods. The waveforms after OC and SC fault occurrence are shown in Figures 6 and 7, respectively. The unit of signal magnitudes in all the potted waveforms is Volt. The S_1 switch is where faults are injected as indicated by the red circle in Figure 2.

Figures 8-10 show the mathematical model generated and simulation waveforms of healthy condition and reconfigured conditions using three reconfiguration methods in sequence: neutral point shift (NPS), amplitude-limited modulation (ALM) and 120° discontinuous pulse width modulation minimum (DPWMMIN) modulation methods. The waveforms show the similarity of the mathematical model generated and simulation results. The RMS and THD values of mathematical model generated and simulation results are summarized in Table III and IV. The percentage error (PE) indicates the proportional change in mathematical model generated result with respect to simulation result. The small PE in all the conditions implies the accuracy of the proposed mathematical model.

By comparing Figures 8-10, the line-to-neutral voltage waveforms show significant difference with either decreased level or changed offset in certain voltage levels; this significantly impacts the RMS value of the line-to-neutral voltage. The variation of RMS and THD under different methods and the percentage degradation (PD) from healthy are summarized in Tables V and VI, respectively. From Table V, the PD of RMS are significant since the per-phase waveforms are distorted heavily. In the cases of Amplitude-limited and 120^O DPWMMIN methods, even though the THD does not change much, the voltage distortions can be observed. The comparison indicates the degree of waveform distortion affects the THD significantly in reconfigured conditions, thus mathematical analysis is essential to correlate the waveform shape and THD, for further THD improvement in future research on MLIs post-fault reconfiguration methods. It is thus clear from Tables V and VI that considering line-to-neutral RMS and THD values in any MLI post-reconfiguration strategy is very essential.

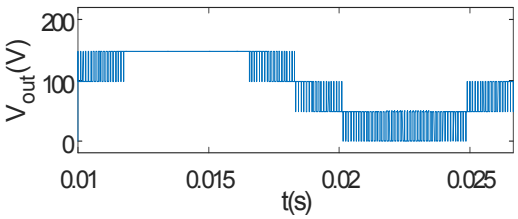

Fig. 6. Dynamic simulation of OC fault condition

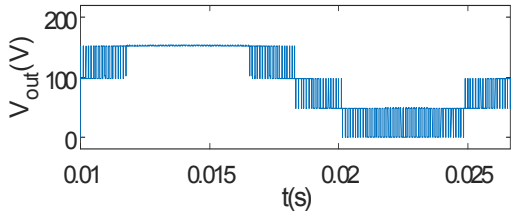

Fig. 7. Dynamic simulation of SC fault condition

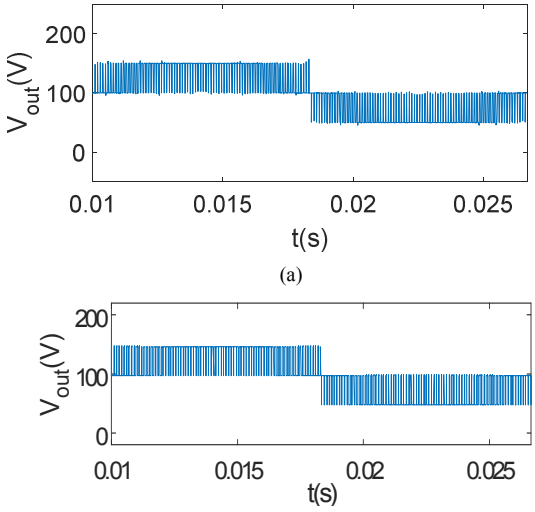

Fig. 8. NPS (a) Mathematical model (b) Simulation result

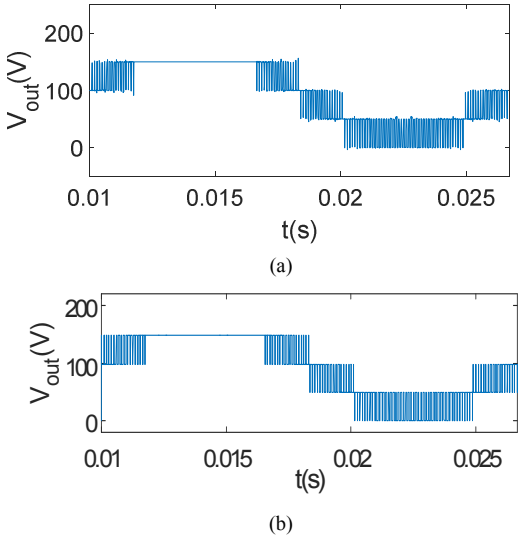

Fig. 9. ALM (a) Mathematical model (b) Simulation result

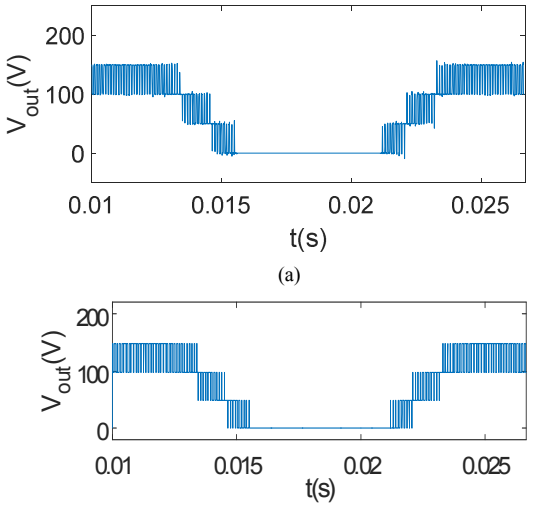

Fig. 10. 120^{O} DPWMMIN (a) Mathematical model (b) Simulation result

TABLE III. RMS COMPARISON BETWEEN MATHEMATICAL MODEL AND SIMULATION

Condition	Mathematical Model	Simulation	PE
Healthy	116.55V	114.95V	1.39%
NPS	107.24V	104.89V	2.24%
ALM	108.14V	106.18V	1.85%
120º DPWMMIN	89.37V	88.05V	1.50%

TABLE IV. THD COMPARISON BETWEEN MATHEMATICAL MODEL AND SIMULATION

Condition	Mathematical Model	Simulation	PE
Healthy	39.11%	38.41%	1.82%
NPS	59.02%	57.30%	3.00%
ALM	39.59%	39.05%	1.38%
120º DPWMMIN	38.60%	38.24%	0.94%

TABLE V. COMPARISON OF RMS BETWEEN RECONFIGURED AND HEALTHY CONDITIONS

Methods	Healthy	Reconfigured	PD
NPS	114.95V	104.89V	-8.75%
ALM	114.95V	106.18V	-7.63%
120º DPWMMIN	114.95V	88.05V	-23.40%

TABLE VI. COMPARISON OF THD BETWEEN RECONFIGURED AND HEALTHY CONDITIONS

Methods	Healthy	Reconfigured	PD
NPS	38.41%	57.30%	49.18%
ALM	38.41%	39.05%	1.67%
120º DPWMMIN	38.41%	38.24%	-0.44%

IV. EXPERIMENTAL SETUP

A 5-level NPC inverter which has the same topology as Figure 2 is shown in Figure 11. A FPGA is used to generate the PWM control signal. The system is successfully tested with the conditions shown in Table I. The healthy condition is shown in Figure 5 and S_1 OC and SC fault conditions of phase A to neutral voltage waveforms are shown in Figures 12 and 13,

respectively. Since the SC fault triggers the self-protection of the power supply, the voltage of the most top supply drops to very low value, so Figures 12 and 13 are similar, but the most top voltage level still has the low value voltage. For comparison purpose, simulation of SC fault is adjusted accordingly, so Figure 7 shows similar waveform as Figure 13. Tables VII and VIII show validation of the simulation with the comparisons of healthy, OC and SC conditions. The PE listed in Table VII and VIII indicates the proportional change in simulation result with respect to experimental result. It is clear from Tables VII and VIII that the simulation model accurately captures the RMS and THD values for healthy and faulty conditions.

Figures 14-16 show the experimental results of reconfigured conditions using three reconfiguration methods in sequence. The RMS and THD values of mathematical model generated and simulation results are summarized in Table IX and X. The small PE shows the proposed mathematical model can accurately describe the experimental result. In summary, Figures 17 and 18 show the comprehensive comparison of RMS and THD for healthy, NPS, ALM and 120º DPWMMIN conditions.

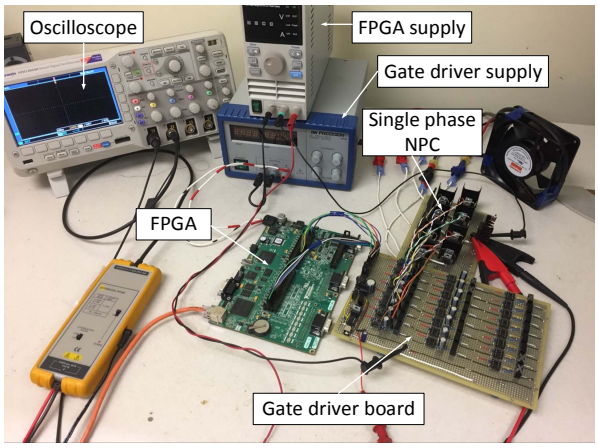

Fig. 11. hardware setup of 5-level NPC

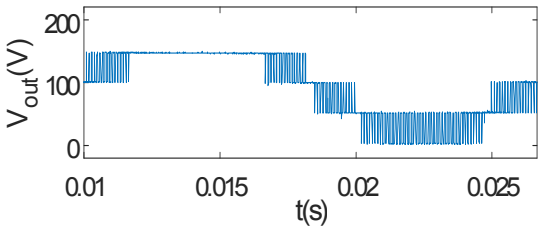

Fig. 12. Experimental OC fault condition

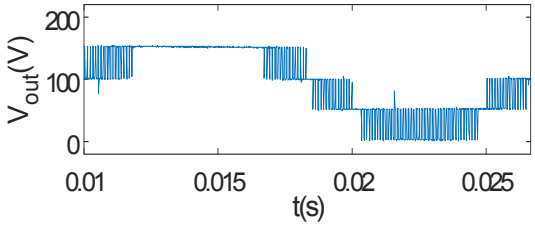

Fig. 13. Experimental SC fault condition

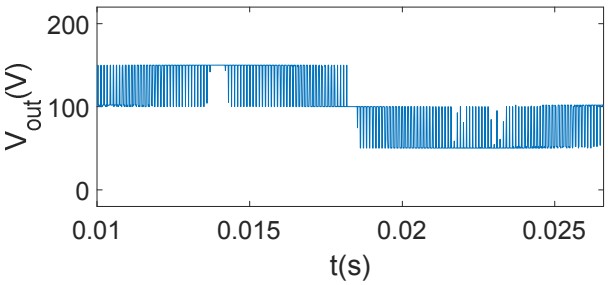

Fig. 14. Experimental result of NPS

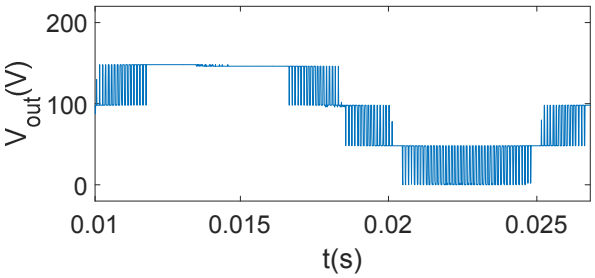

Fig. 15. Experimental result of ALM

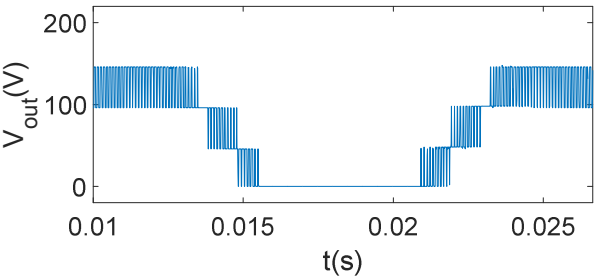

Fig. 16. Experimental result of 120º DPWMMIN

TABLE VII. RMS VALIDATION

Conditions	Simulation	Experiment	PE
Healthy	114.95V	113.25V	1.50%
OC	106.18V	107.03V	0.79%
SC	109.02V	110.09V	-0.97%

TABLE VIII. THD VALIDATION

Conditions	Simulation	Experiment	PE
Healthy	38.41%	37.22%	3.20%
OC	39.05%	39.58%	-1.34%
SC	37.95%	38.39%	-1.15%

TABLE IX. RMS COMPARISON BETWEEN MATHEMATICAL MODEL AND EXPERIMENT

Condition	Mathematical Model	Experiment	PE
Healthy	116.55V	113.25V	2.91%
NPS	107.24V	106.62V	0.58%
ALM	108.14V	103.38V	4.60%
120º DPWMMIN	89.37V	86.53V	3.28%

TABLE X. THD COMPARISON BETWEEN MATHEMATICAL MODEL AND EXPERIMENT

Condition	Mathematical Model	Experiment	PE
Healthy	39.11%	37.22%	5.08%
NPS	59.02%	58.55%	0.80%
ALM	39.59%	38.80%	2.03%
120º DPWMMIN	38.60%	40.53%	4.76%

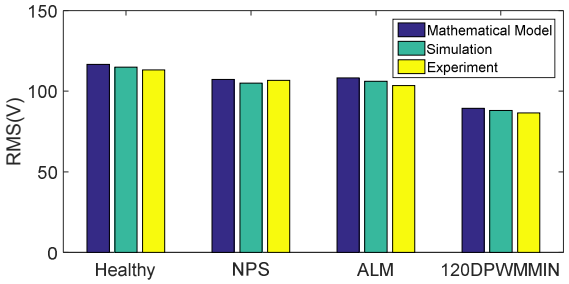

Fig. 17. Bar chart of RMS comparison

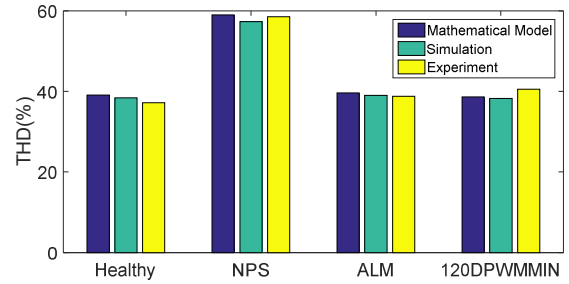

Fig. 18. Bar chart of THD comparison

V. CONCLUSION AND FUTURE WORK

A mathematical model which includes both low frequency and high frequency components is proposed and the significance of line-to-neutral harmonic and RMS analysis among healthy, faulty, and reconfigured conditions is raised in this paper. Based on the 5-level NPC inverter example, simulation and experimental results of healthy, faulty and reconfigured conditions are provided. The results indicate that while the reconfigured condition maintains the line-to-line voltage balance, this comes at a cost of distortion in the line-to-neutral voltage and increased THD and not maintaining desired line-to-neutral RMS values. This suggests that reconfiguration with the purpose of maintaining a desired line-to-line voltage and its RMS value are not sufficient when specific voltage quality and THD are desired to be met for per-phase conditions. The mathematical model has been verified by simulation and experimental results on all the conditions, this will help to better understand how to minimize the reconfiguration impact on the line-to-neutral voltage. A single phase 5-level NPC inverter has been tested and utilized as the platform to analyze the harmonic content. The results show similarity to simulation results and indicate waveform distortion and degradation of RMS and THD in the reconfigured conditions of used methods.

REFERENCES

[1] Surin Khomfoi and Leon M. Tolbert, *Multilevel book Chapter.* The University of Tennessee. Available: http://web.eecs.utk.edu/~tolbert/publications/multilevel_book_chapter.pdf

[2] Lei Hu, Mingyao Ma, Alian Chen, Xiangning He and Hao Ma, "Reconfiguration of carrier-based modulation strategy for fault tolerant multilevel inverters," In *Proc. 31st Annual Conference of IEEE Industrial Electronics Society, IECON 2005.*, Raleigh, NC, 2005, pp. 6 pp.-.

[3] S. M. Kim, J. S. Lee and K. B. Lee, "Fault-tolerant strategy using neutral-shift method for cascaded multilevel inverters based on level-shifted PWM," In *Proc. 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, Seoul, 2015, pp. 1327-1332.

[4] P. Correa and J. Rodriguez, "Control Strategy Reconfiguration for a Multilevel Inverter Operating with Bypassed Cells," *2007 IEEE International Symposium on Industrial Electronics*, Vigo, 2007, pp. 3162-3167.

[5] H. Ben Abdelghani and A. B. Ben Abdelghani, "Fault tolerant SVM strategy for 3-level NPC inverter," In *Proc. 8th International Multi-Conference on Systems, Signals and Devices (SSD)*, Sousse, 2011, pp. 1-6.

[6] H. B. Abdelghani, A. B. B. Abdelghani, F. Richardeau, J. M. Blaquière and F. Mosser, "Post-fault reconfiguration for a versatile and hybrid 4 Leg NPC-flying capacitor topology," In *Proc. IEEE 23rd International Symposium on Industrial Electronics (ISIE)*, Istanbul, 2014, pp. 1502-1507.

[7] T. Gallah, B. Bouzidi and A. Masmoudi, "DTC adaptation following the reconfiguration from three to two legs of a three level inverter fed induction motor drive," In *Proc. Ninth International Conference on Ecological Vehicles and Renewable Energies (EVER)*, Monte-Carlo, 2014, pp. 1-10.

[8] A. Chen, C. Zhang, X. He and N. Cui, "Fault-tolerant design for flying capacitor multilevel inverters," in *Proc. IEEE 6th International Power Electronics and Motion Control Conference, 2009. IPEMC '09.*, Wuhan, 2009, pp. 1460-1464.

[9] S. Khomfoi, N. Praisuwanna and L. M. Tolbert, "A hybrid cascaded multilevel inverter application for renewable energy resources including a reconfiguration technique," In *Proc. IEEE Energy Conversion Congress and Exposition*, Atlanta, GA, 2010, pp. 3998-4005.

[10] D. Eaton, J. Rama and P. Hammond, "Neutral shift [five years of continuous operation with adjustable frequency drives]," *IEEE Industry Applications Magazine*, vol. 9, no. 6, pp. 40-49, Nov.-Dec. 2003.

[11] Sang, Z. Mao, C. Wang, D, "Comparison on Staircase, PWM and Partial PWM Scheme for Hybrid Cascaded Multilevel Inverter," Internet: http://pe.org.pl/articles/2013/5/14.pdf

[12] E. Kabalci, I. Colak, R. Bayindir and C. Pavlitov, "Modelling a 7-level asymmetrical H-bridge multilevel inverter with PS-SPWM control," in *Proc. International Aegean Conference on Electrical Machines and Power Electronics and Electromotion, Joint Conference, Istanbul, 2011,* pp. 578-583.

[13] Philip T.Kerin, *Elements of Power Electronics,* pp. 217-219