Real-Time Calculation Method for Single-Phase Multilevel Converters Based on Phase-Shifted Carrier Pulsewidth Modulation

Junpeng Ma[1], Xiongfei Wang[2], Frede Blaabjerg[2], Wensheng Song[1]
[1]School of Electrical Engineering, Southwest Jiaotong university, Chengdu, Sichuan, China
[2]Department of Energy Technology, Aalborg University, Aalborg, Denmark
junpeng_ma@163.com, xwa@et.aau.dk, fbl@et.aau.dk, songwengsheng@163.com

***Abstract*—The time delay caused by the digital computation and the update of duty cycle tends to worsen the dynamic performance of digitally controlled power converters. This paper proposes a real-time calculation method for multilevel converters with the phase-shifted carrier pulsewidth modulation (PSC-PWM) to eliminate the time delay of the digital controller without the loss of duty cycle. A proposed sampling method, which samples the current and voltage at the intersections of all phase shifted carriers, is used alternately with the traditional regular sampling method following a selection rule, which is elaborated in theory. Experimental results verify that the proposed real-time calculation method effectively improves the bandwidth of the control system.**

Keywords—bandwidth*; *Multi-sampling method*; *multilevel inverter*; *phase-shifted carrier pulse width modulation*; *real-time calculation

I. INTRODUCTION

The regular-sampling pulsewidth moduation has been widely used with the digitally controlled power converters [1], [2]. In this method, the current and voltage are sampled at the instant of the peak or/and valley of the triangular carrier, and the calculated modulating voltage is updated at next sampling instant due to the computational delay [3], [4]. A sampling period of time delay is thus introduced into the control loop, which deteriorates the dynamic response and stability of the control system [5].

To suppress the influence of the unit delay on the control system, many methods have been reported in [6-8]. In [6], the deadbeat control scheme is applied to compensate the time delay. This method needs to predict the line current based on the mathematical model of the converters. Therefore, the inaccurate model of converters will worsen the control performance by using this method [9]. In [5], the sampling instant is shifted towards to the instant of the duty cycle update. It reduces the unit delay to computational delay, which is the computational duration of the control method. The bandwidth of the control loop is dramatically improved by using this method, but the current harmonics caused by the turn on/off of the power switching will be introduced into the control loop, leading to the undesired harmonics in the calculated modulating wave, which will increase the current harmonics content [10], [11]. In [12], a multi-sampling method is reported to improve the bandwidth of the control loop. In this method, the sampling and the duty cycle update are multiply carried out during one triangular carrier period. the time delay caused by the sampling is obviously reduced by using this method. However, the multiple switching and the dead-band caused by multi-sampling method complicates the modeling and analysis of the control system and lead to undesired switching noise[13]. In [14], a novel quadruple sampling method is proposed to solve the problem of the multiple switching in the traditional multi-sampling method. Yet, the unit delay, which equals to the quarter of the carrier period, still exists in the control loop.

The fast calculation of the control method by using field programmable gate array (FPGA) can reduce the computational delay to the degree of the microsecond, which gives a new path to reduce the digital delay[15], [16]. In [16], the sampling of the current and voltage takes place at the peak and/or valley of the carrier, yet the duty cycle is updated immediately after the digital computation. Thus, the time delay is greatly reduced, and a real-time calculation of the modulating wave is approximately achieved. However, this method is subject to the loss of duty cycle, and requires a high-performance digital controller which consequently increases the hardware cost. In [17], a dual sampling method is introduced to achieve the real-time calculation in single-phase two-level inverters without the loss of duty cycle and it merely needs a low-cost digital signal processor. Yet, this method cannot be applied in multilevel converters.

Phase-shifted-carrier PWM(PSC-PWM) is widely applied in multilevel converters to generate the desired driving pulse[18], [19]. The current and voltage are sampled at the peak and valley of all carriers, and there still exists a unit delay between the instant of the sampling and the duty cycle update[20], [21]. In order to achieve a real-time calculation of the modulating wave without time delay for multilevel converters, this paper proposes first a sampling method, which samples the current and voltage at the intersection of all carriers. Then, to avoid any loss of duty cycle, the proposed sampling method is alternately used with the traditional sampling method, and a selection rule between the traditional and developed sampling methods is formulated. Experimental results confirm that the bandwidth of the control loop is improved with the reduced time delay.

This work was supported in part by European Research Council (ERC) under the European Union's Seventh Framework Program (FP/2007-2013)/ERC Grant Agreement [321149-Harmony], in part by the Doctoral Innovation Foundation of Southwest Jiao University, and in part by China Scholarship Council.

The rest of this paper is organized as follows: Section II describes the topology of single-phase cascaded H-bridge (CHB) inverters. The traditional sampling method for single-phase two-level inverter is analyzed and discussed detailly in Section III. The proposed real-time calculation method for the single-phase multilevel inverter is elaborated in Section IV. Section V analyzes the stability boundary of the control loop with the proportional current controller by using traditional sampling method and the real-time calculation method. The experimental test is executed to verify the correctness of the theoretical analysis in Section VI. Section VII concludes this paper.

II. System Description

Fig. 1 shows the topology of a single-phase CHB multilevel inverter with a digital current controller, where u is the main voltage, and L and R are the filter inductance and its equivalent resistance, respectively. v_x is the output voltage of two-level H-bridge inverters in cell x, and all cells are connected in series. The synthesized voltage v is the sum of all individual cell outputs. u_{dcx} represents a constant dc-link voltage of the converter cell x. S_{xyp} and S_{xyn} represent upper and lower switching devices in leg y of the cell x, where $y = a$, b, and $x = 1, 2...N$. In this paper, two cascaded converter cells are considered.

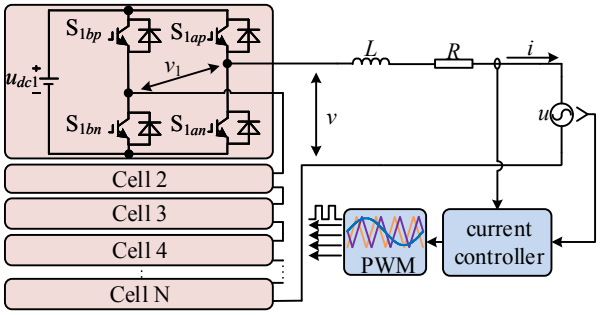


Fig. 1. A single-phase inverter with the digital current controller.

The resistance R is usually small, which is ignored for simplicity. The Kirchhoff voltage law (KVL) is adopted to analyze voltage across the inductor L, and the voltage equation is shown as

$$L\frac{di}{dt} = v - u. \tag{1}$$

The output voltage of the inverter can be described as

$$v = \sum_{x=1}^{N} v_x = \sum_{x=1}^{N} (v_{xa} - v_{xb}) = \sum_{x=1}^{N} v_{xa} - \sum_{x=1}^{N} v_{xb} \tag{2}$$

where the output voltage v_{xa} and v_{xb} of the leg a and leg b in cell x respectively are defined as

$$v_{xy} = \begin{cases} u_{dcx}/2 & S_{xy}=1 \\ -u_{dcx}/2 & S_{xy}=0 \end{cases} \tag{3}$$

where x=1…N, y=a, b. The switching function S_{xy} is defined as

$$S_{xy} = \begin{cases} S_{xyp} \ is\ on \text{ and } S_{xyn} \ is\ off \\ S_{xyp} \ is\ off \text{ and } S_{xyn} \ is\ on. \end{cases} \tag{4}$$

For simplification, it is assumed that the rated power and dc-link voltage of each converter cell is the same, that is

$$\begin{cases} u_{dcx} = u_{dc} \\ P_x = P_{rate}. \end{cases} \tag{5}$$

In this case, the modulating voltage of each cell satisfies

$$v_x^* = \frac{v^*}{N} \tag{6}$$

where v^* is the modulating wave calculated by the digital controller.

The normalized modulating wave for cell x, which feeds into the modulator, is simplified as

$$\underline{v}_x^* = \frac{v_x^*}{(u_{dcx}/2)} = \frac{v^*}{N(u_{dc}/2)} = \underline{v}^*. \tag{7}$$

PSC-PWM usually is applied to generate the drive pulse for CHB inverter, the shifted phase of the triangular carrier C_x for cell x relative to that for cell 1 is expressed as

$$\alpha_x = \frac{(x\text{-}1)\pi}{N} \tag{8}$$

where $x = 1…N$. Using two-cells CHB converter as an example, the shifted phase of the triangular carriers for cell 1 and cell 2 respectively are 0 and 90º.

III. Traditional Sampling Method for Two-Level H-Bridge

A. Traditional sampling method

Traditionally, the voltage and current are sampled at the instant of the peak and valley of the triangular carrier.it is shown in

Fig. 2. Where T_{cp} is the computational duration, and T_{on} and T_{off} represent the duration of turn-on and turn-off for the upper power switching of the corresponding leg during one sampling interval T_{sa} and these two durations satisfy

$$\begin{cases} T_{on} + T_{off} = T_{sa} \\ T_{sw} = 2T_{sa} \end{cases} \tag{9}$$

where T_{sw} is the switching period or triangular carrier period. In each sampling instant, the current and voltage are sampled and then the calculation of the modulating wave $\underline{v}$ will be completed after the duration T_{cp}. The calculated modulating wave $\underline{v}$ will be updated in next sampling instant. The modulating wave is compared with the triangular carrier to generate driving pulse ③. Therefore, there is the time delay of one sampling interval, named as unit delay, between the sampling instant and duty cycle update (modulating wave update) instant in the traditional method.

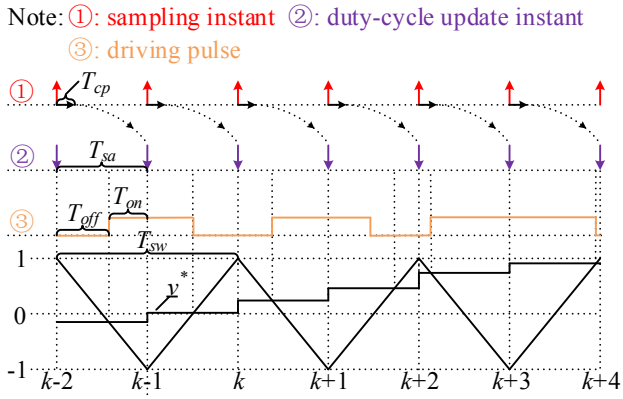


Fig. 2. The traditional sampling method and modulating process with the unit delay.

B. Real-Time Calculation and The Loss of the Duty cycle

In order to suppress the influence of the unit delay on the control system, the feasible method is to immediately update the duty cycle after the computational duration T_{cp}. This process, named as the computational delay mode, is described as the sampling instant ①, the duty cycle update instant ②, the driving pulse ③ and the modulating wave $\underline{v}_d$ in Fig. 3. The computational delay T_{cp} between the sampling instant and duty cycle update instant cannot be eliminated, but the ideal real-time calculation for the modulating wave satisfies that T_{cp}=0, which means that the sampling event happens at the instant of the duty cycle update. This ideal process, named as real-time calculation mode, is described as the sampling instant①, the driving pulse ④and the modulating wave $\underline{v}_r$, in Fig. 3. It can be seen that the driving pulse ③and ④ are the same during the interval from the instant *k*th to *k*+2th in Fig. 3(a) and the interval from the instant *k*-2th to *k*th in Fig. 3 (b). Consequently, the control performance in the real-time calculation mode is equivalent to that in the computational delay mode.

However, during the interval from the instant *k*-1th to *k*th in Fig. 3(a) and the interval from *k*th to *k*+1th in Fig. 3(b), the driving pulse ③ is different from ④. This difference is caused by the computational duration T_{cp}, which lead to the loss of the duty cycle. Therefore, in order to achieve equivalent process of the real-time calculation, the ranges of the modulating wave $\underline{v}$ need to satisfy

$$\frac{2T_{cp}}{T_{sa}} - 1 < \underline{v}^* < 1 - \frac{2T_{cp}}{T_{sa}} \tag{10}$$

Due to the limitation of the duty cycle shown in (10), by using the traditional method, the real-time calculation for the modulating wave cannot be achieved even if the duty cycle is updated immediately after the computational delay.

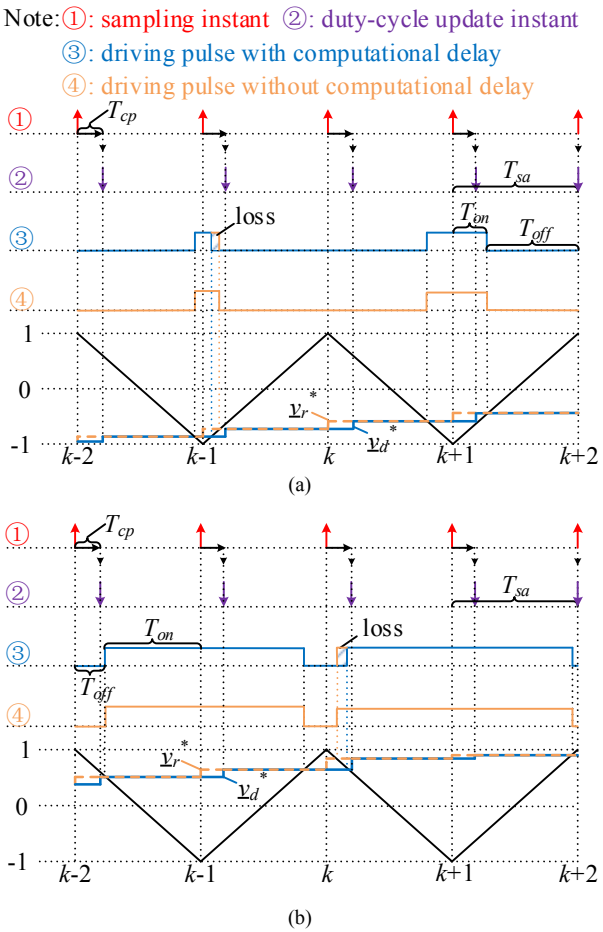


Fig. 3. The loss of the duty cycle caused by the computational delay mode in the traditional sampling mode. (a) the case of the modulating wave near to -1, and (b) the case of the modulating wave near to 1.

IV. The Proposed Real-time Calculation Method For Multilevel Converter

A. The multiple sampling mode I

The sampling mode I is shown in Fig. 4, the sampling and the duty cycle update happen in the peak and valley of all the triangular carriers, and there hereby are 2N sampling instants during one carrier period, that is

$$T_{sw} = 2NT_{sa}. \tag{11}$$

In Fig. 4, C_{xy} represents the triangular carrier for leg *y* in cell *x*, and C_{xb} is the reciprocal of C_{xa}. The equivalent PSC-PWM process for multilevel converters to generate the desired output voltage *v* can be achieved by the comparison of the triangular carriers and modulating wave $\underline{v}$. The amplitude of the carrier is divided into four sectors, and for N-cell cascaded inverter, there are 2N sectors, and the height of the sector can be expressed as

$$h = 1/N. \tag{12}$$

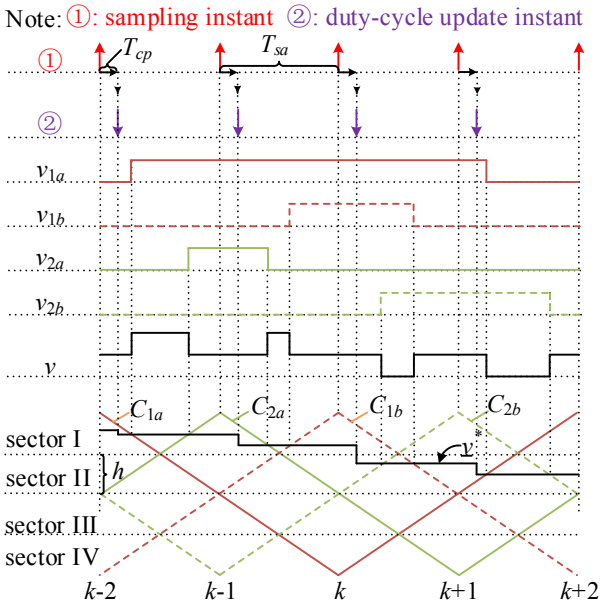


Fig. 4. The multiple sampling mode I.

Fig. 5 shows the loss of the duty cycle due to the computational delay mode. In Fig. 5, v_d is the output voltage of the inverter in the computational delay mode. v_r is the output voltage of the inverter in the ideal real-time calculation mode. It can be seen that the loss of the duty cycle is also introduced provided that the modulating wave near to the peak point, valley point, and zero point of the carriers and these points appear at the sampling instant. The loss of the duty cycle can be avoided provided that the modulating wave is far away from these points, which means that $\underline{v}$ need to satisfy

$$\begin{cases} \dfrac{T_{cp}}{T_{sa}} < \underline{v}^* < 1 - \dfrac{T_{cp}}{T_{sa}} \\ \dfrac{T_{cp}}{T_{sa}} - 1 < \underline{v}^* < -\dfrac{T_{cp}}{T_{sa}} \end{cases} \tag{13}$$

which can guarantee that the duty cycle update in computational delay mode is equivalent to that in real-time calculation mode. For N-cell cascaded inverter, the loss of duty cycle still appears in the case of the modulating wave near to the value of the carriers at the sampling instant. The similar analysis method can be used to deduce the range of modulating wave as

$$2mh - 1 + \frac{4T_{cp}}{T_{sw}} < \underline{v}^* < 2(m+1)h - 1 - \frac{4T_{cp}}{T_{sw}} \tag{14}$$

where m=0,1…N-1. It can be seen that the range of 2-cell cascaded inverter shown in (13) is a special case shown in (14).

This limitation of the modulating wave restrains the modulating range. In order to remove the limitation of the modulating wave shown in (13), a new sampling mode is proposed in this paper.

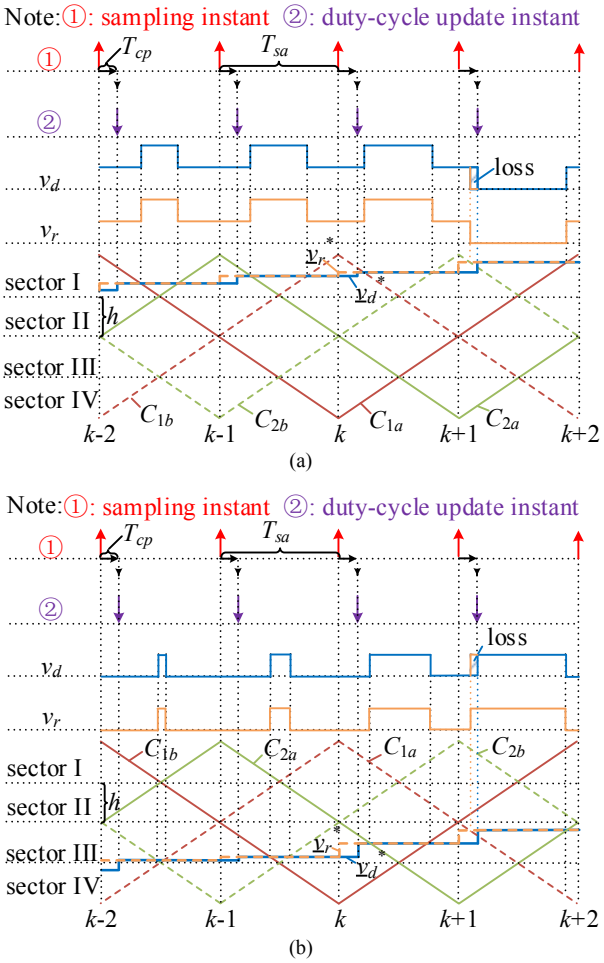


Fig. 5. The loss of the duty cycle due to the computational delay in the multiple sampling mode I. (a) the modulating wave near to 1, and (b) the modulating wave near to -1.

B. The proposed multiple sampling mode II

The proposed sampling method samples the voltage and the current at the instants of intersections of all carriers, except for instants of the peak and valley of the carriers. The duty cycle is updated immediately after the computational delay T_{cp}. This sampling mode is shown in Fig. 6.

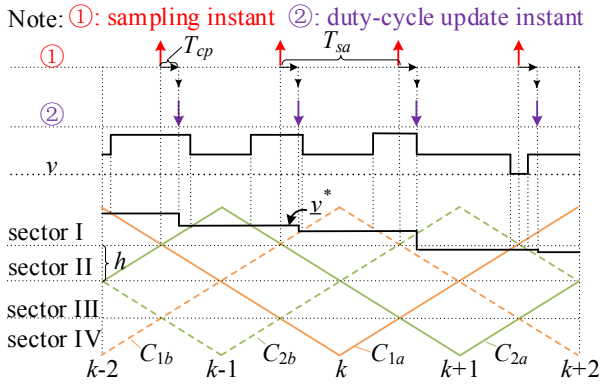


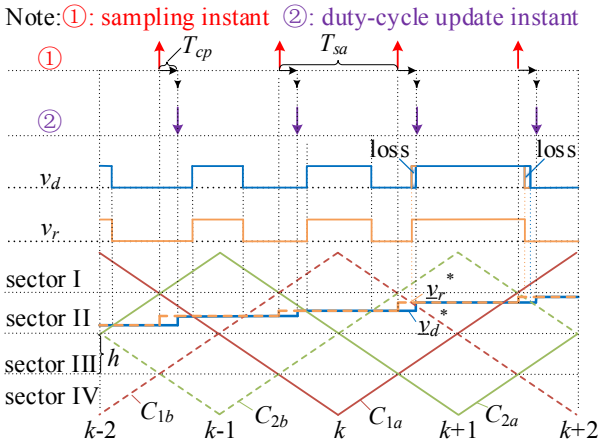
Fig. 6. The proposed multiple sampling mode II.

Fig. 7 shows the loss of the duty cycle due to the computational delay in the proposed multiple sampling mode II. Similarly, there exists the loss of the duty cycle when the modulating wave is close to the value of the carriers at the sampling instant, and the output voltage of the inverter v_d and v_r are the same provided that the modulating wave satisfies

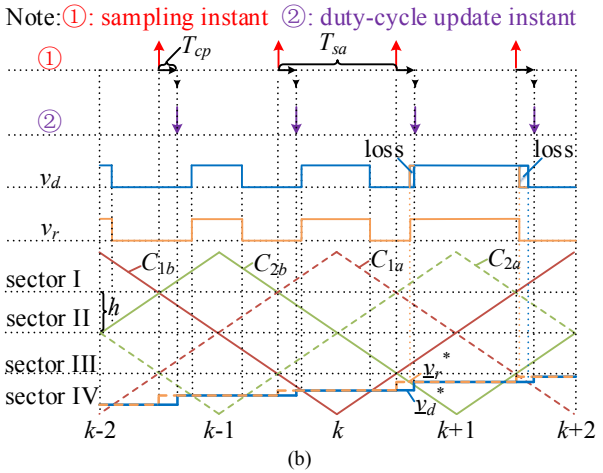
$$\begin{cases} \underline{v}^* > \dfrac{4T_{cp}}{T_{sw}} + h \\ -h + \dfrac{4T_{cp}}{T_{sw}} < \underline{v}^* < h - \dfrac{4T_{cp}}{T_{sw}} \\ \underline{v}^* > -h - \dfrac{4T_{cp}}{T_{sw}}. \end{cases} \tag{15}$$

For N-cell cascaded inverter, the range of the modulating wave without the loss of the duty cycle can be deduced as

$$\underline{v}^* < (2m+1)h\text{-}1 - \frac{4T_{cp}}{T_{sw}} \quad or \quad \underline{v}^* > (2m+1)h\text{-}1 + \frac{4T_{cp}}{T_{sw}}. \tag{16}$$



(a)



(b)

Fig. 7. The loss of the duty cycle due to the computational delay in the multiple sampling mode II. (a) the modulating wave near to the positive intersections of all carriers. (b) the modulating wave near to the negative intersections of all carriers.

C. The Selection of the Sampling Mode

According to (14) and (16), it can be seen that the range for the modulating wave in the sampling mode I is different from that in sampling mode II. In order to eliminate the limitation of the modulating wave of these two sampling modes, the sampling mode I needs to be switched to the sampling mode II if the modulating wave is out of the range in (14) and vice-versa. And the upper limitation and lower limitation in (14) and (16) need satisfy

$$\begin{cases} 2mh\text{-}1 + \dfrac{4T_{cp}}{T_{sw}} < (2m+1)h\text{-}1 - \dfrac{4T_{cp}}{T_{sw}} \\ 2(m+1)h\text{-}1 - \dfrac{4T_{cp}}{T_{sw}} > (2m+1)h\text{-}1 + \dfrac{4T_{cp}}{T_{sw}} \end{cases} \tag{17}$$

which guarantees that the union of (14) and (16) for the modulating wave $\underline{v}^*$ is equal to the complete set $\{\underline{v}^* : -1 < \underline{v}^* < 1\}$. And (17) can be further simplified as

$$T_{cp} < \frac{T_{sw}h}{8} = \frac{T_{sw}}{8N}. \tag{18}$$

The real-time calculation without the loss of duty cycle can be achieved by switching these two sampling modes provided that the computational delay T_{cp} is located in the range shown in (18). According to the range of the sampling mode I and the sampling mode II shown in (14) and (16), the criterion of sampling mode selection can be expressed as

$$\begin{cases} \text{mode I}: (2m+1)h\text{-}1 - \dfrac{4T_{cp}}{T_{sw}} < \underline{v}^* < (2m+1)h\text{-}1 + \dfrac{4T_{cp}}{T_{sw}} \\ \text{mode II}: \underline{v}^* < 2mh\text{-}1 + \dfrac{4T_{cp}}{T_{sw}} \quad or \quad \underline{v}^* > 2(m+1)h\text{-}1 - \dfrac{4T_{cp}}{T_{sw}} \end{cases} \tag{19}$$

This sampling mode selection can be achieved by using hysteresis comparator drawn as Fig. 8, where the coefficient a_m, b_m, c_m, and d_m are deduced as

$$\begin{cases} a_m = (2m+0.5)h\text{-}1 - \Delta h, b_m = (2m+0.5)h\text{-}1 + \Delta h \\ c_m = (2m+1.5)h\text{-}1 - \Delta h, d_m = (2m+1.5)h\text{-}1 + \Delta h \\ \Delta h = 0.5h - T_{cp} / T_{sa}, \quad m = 0,\ldots N-1 \end{cases} \tag{20}$$

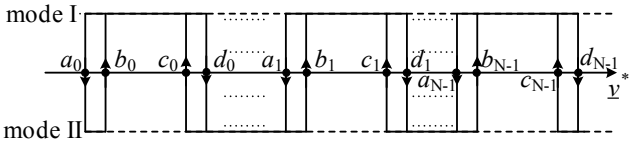


Fig. 8. The sampling mode selection.

For simplification, the hysteresis width $2\Delta h$ is set to zero and the criterion for the selection of the sampling mode can be deduced as

$$\begin{cases} \text{mode I}: 0.5h < \text{mod}(\underline{v}^* + 1, 2h) < 1.5h \\ \text{mode II}: \text{else} \end{cases} \tag{21}$$

where mod (x, y) is the remainder function, which is equal to x-$\lfloor x/y \rfloor y$. $\lfloor x/y \rfloor$ is the largest integer less than x/y. according to this selection of sampling mode, the real-time calculation method can be achieved without the loss of duty cycle.

Fig. 9 shows the operation process of the proposed method. The modulating wave, calculated at the instant k-1th, is located in the range of the sampling mode I in (21). Therefore, the sampling mode is switched to the mode I at the instant kth. The real-time calculation of the modulating wave is achieved and the loss of duty cycle due to computational delay is eliminated by using the proposed method.

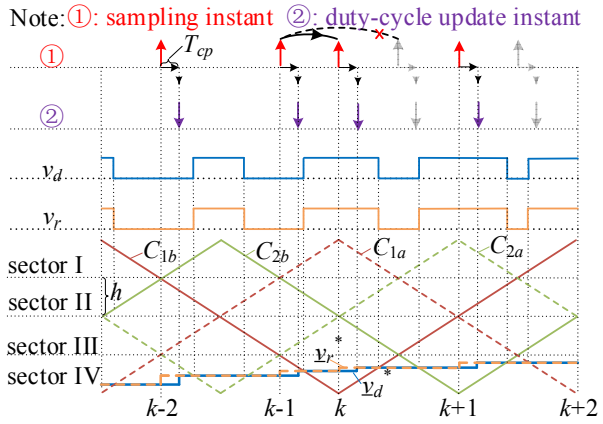


Fig. 9. The selection process of the sampling mode.

V. The Analysis for the Stability Boundary of the Control Loop

The forward difference is applied to discretize the model in (1) of the L-filtered inverter, and the block diagram of digitally controlled inverter with L-filter is drawn as

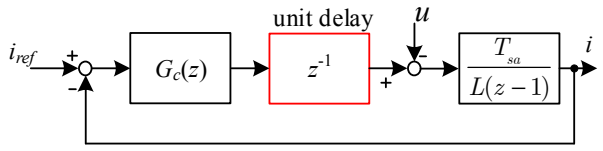


Fig. 10. The block diagram of the digitally controlled inverter with L-filter.

The proportional current controller (G_c (z) =K_p) is used to test the stability boundary of the current loop with different sampling method. In traditional sampling method, there exists the unit delay in the control loop but this time delay will be removed when the real-time calculation method is applied. The open loop transfer function with and without the unit delay can be expressed as

$$\begin{cases} G_1(z) = z^{-1}\dfrac{K_p T_{sa}}{L(z-1)} \\ G_2(z) = \dfrac{K_p T_{sa}}{L(z-1)} \end{cases} \tag{22}$$

The phase crossover frequency of (22) satisfies

$$\begin{cases} \angle G_1(e^{j2\pi f_{cr1}}) = -\pi \\ \angle G_2(e^{j2\pi f_{cr2}}) = -\pi \end{cases} \tag{23}$$

According to (23), the phase crossover frequency can be solved as

$$\begin{cases} f_{cr1} = \dfrac{1}{6T_{sa}} = \dfrac{N}{3T_{sw}} \\ f_{cr2} = \dfrac{1}{2T_{sa}} = \dfrac{N}{T_{sw}} \end{cases} \tag{24}$$

The corresponding critical proportional gain satisfies

$$\begin{cases} |G_1(e^{j2\pi f_{cr1}})| = 1 \\ |G_2(e^{j2\pi f_{cr2}})| = 1 \end{cases} \tag{25}$$

Therefore, the critical proportional gain can be solved as

$$\begin{cases} K_{p\_crit1} = 2NL / T_{sw} \\ K_{p\_crit2} = 4NL / T_{sw} \end{cases} \tag{26}$$

It can be seen from (24) and (26) that the phase crossover frequency and critical proportional gain in real-time calculation method are much larger than that in the traditional method, which means that the bandwidth of control loop is effectively improved by using the proposed method.

VI. Eperimental Test

In order to verify the correctness and validation of the proposed method, the experimental tests are implemented and the experimental parameter is listed in Table I.

TABLE I
Experimental Parameter

Parameter	Value
DC-link voltage of each cell	120 V
The main voltage u (RMS)	100 V
Filter inductance L	9 mH
Switching frequency/Carrier frequency f_{sw}	1250 Hz

Fig. 11 shows the measured line current in steady state with different time delay. The total harmonic distortion (THD) by using the traditional method with the unit delay is higher than that by using real-time calculation method without time delay, which verifies that the selection of the sampling mode for achieving real-time calculation has no effect on the line current quality.

Fig. 12 shows the measured line current in the instability state with the different method. In Fig. 12(a), the proportional gain is set to 42 Ω. The control system by using the traditional method with the unit delay becomes unstable and the resonant frequency is 833.3Hz, which is smaller than the resonant frequency(2500Hz) of the real-time calculation method shown in Fig. 12(b), where the proportional gain is set to 90 Ω. The bandwidth of the proposed real-time calculation method is much larger than that of the traditional method.

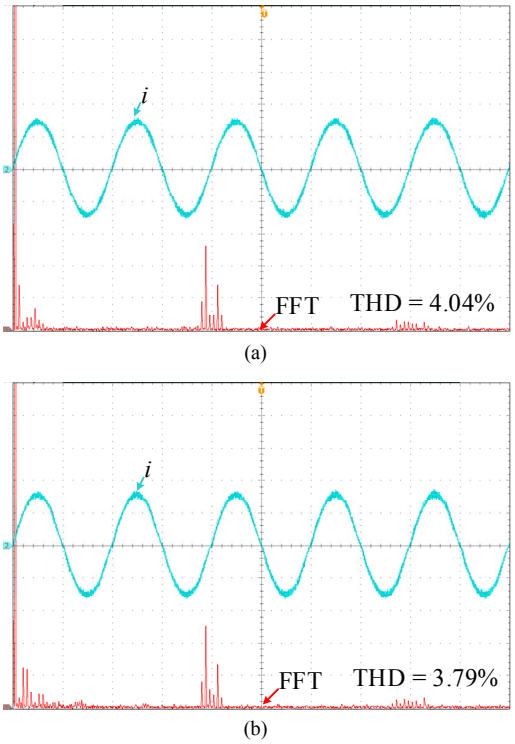


Fig. 11. The measured line current with different time delay: (a) traditional method with the unit delay, and (b) real-time calculation method without the time delay (*i*: 5 A/div, Time: 10 ms/div, THD: 50mA/div, 1.25kHz/div).

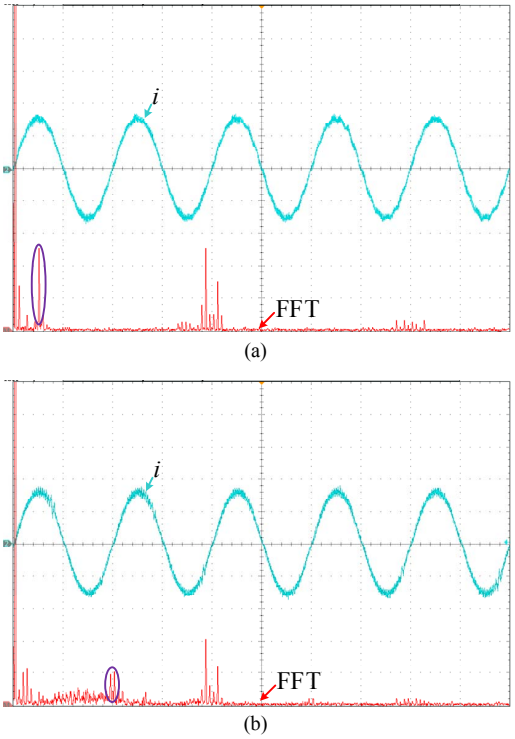


Fig. 12. The line current in instability state with the different methods: (a) traditional method with the unit delay, and (b) real-time calculation method. (*i*: 5 A/div, Time: 10 ms/div, THD: 50mA/div, 1.25kHz/div).

Fig. 13 shows the line current in the dynamic state, where K_p is set to 30 Ω and 45 Ω by using the traditional method with the unit delay and the proposed real-time calculation method, respectively. this proportional gain can guarantee that the controller can quickly track their reference current with little overshoot. It can be seen from Fig. 13 that although both controllers can track the reference, the proposed method can achieve a faster tracking with a smaller overshoot than that by using the traditional sampling method due to the larger proportional gain obtained by the proposed sampling method, which again implies that the real-time calculation increases the bandwidth of the control loop.

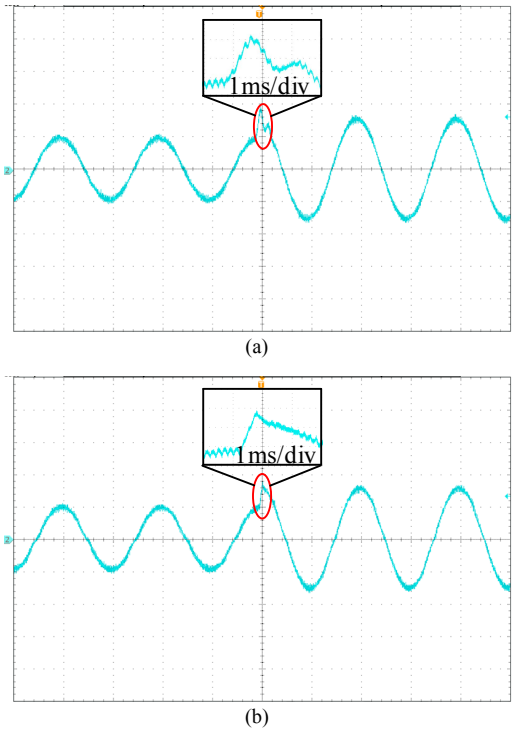


Fig. 13. The line current in the case of the sudden change of the reference current: (a) traditional method with the unit delay, and (b) real-time calculation method. (*u*: 50V/div, *i*: 5A/div, Time: 10ms/div)

VII. Conclusion

This paper has proposed a real-time calculation method for CHB multilevel converters modulated by PSC-PWM. a new sampling method, which samples the current and voltage at the intersection point of the phase shifted carriers is proposed. The selecting method of the traditional sampling mode and the proposed sampling mode is elaborated to avoid the limitation of the duty cycle due to the computational delay. The real-time calculation for the modulating wave is equivalently achieved by switching these two sampling modes, and the alternative selection of the sampling modes has no effect on the line current quality, and the bandwidth of the control loop is dramatically improved by using the proposed real-time calculation method.

References

[1] A. Edpuganti and A. K. Rathore, "A survey of low switching frequency modulation techniques for medium-voltage multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 5, pp. 4212-4228. 2015.

[2] W. Song, X. Feng, and K. M. Smedley, "A carrier-based PWM strategy with the offset voltage injection for single-phase three-level neutral-point-clamped converters," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1083-1095, Aug. 2013.

[3] A. Bouafia, J.-P. Gaubert, and F. Krim, "Predictive direct power control of three-phase pulsewidth modulation (PWM) rectifier using space-vector modulation (SVM)," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 228-236, Jan. 2010.

[4] P. Jintakosonwit, H. Fujita, and H. Akagi, "Control and performance of a fully-digital-controlled shunt active filter for installation on a power distribution system," *IEEE Trans. Power Electron.*, vol. 17, no. 1, pp. 132-140, Jan. 2002.

[5] P. Mattavelli, F. Polo, F. D. Lago, and S. Saggini, "Analysis of control-delay reduction for the improvement of UPS voltage-loop bandwidth," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2903-2911, Aug. 2008.

[6] W. Song, J. Ma, L. Zhou, and X. Feng, "Deadbeat predictive power control of single phase three level neutral-point-clamped converters using space-vector modulation for electric railway traction," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 721-732, Jan. 2016.

[7] Y. Zhang, W. Xie, and Y. Zhang, "Deadbeat direct power control of three-phase pulse-width modulation rectifiers," *IET Power Electron.*, vol. 7, no. 6, pp. 1340-1346, Nov. 2014.

[8] S. Vazquez, R. P. Aguilera, P. Acuna, J. Pou, J. I. Leon, L. G. Franquelo, and V. G. Agelidis, "Model predictive control for single-phase NPC converters based on optimal switching sequences," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7533-7541, Dec. 2016.

[9] W. Jiang, X. Ding, Y. Ni, J. Wang, L. Wang, and W. Ma, "An improved deadbeat control for a three-phase three-line active power filter with current tracking errors compensation," *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 1-1. 2017.

[10] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*, Seattle,WA,USA: Morgan & Claypool, 2015.

[11] L. Corradini, M. Paolo, E. Tedeschi, and D. Trevisan, "High-bandwidth multisampled digitally controlled DC-DC converters using ripple compensation," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1501-1508, Apr. 2008.

[12] X. Zhang, P. Chen, C. Yu, F. Li, H. T. Do, and R. Cao, "Study of current control strategy based on multi-sampling for high-power grid-connected inverters with LCL-filter," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5023-5034, Jul. 2016.

[13] L. Corradini and P. Mattavelli, "Analysis of multiple sampling technique for digitally controlled dc-dc converters," in *IEEE Power Electron. Specialists Conf.*, Jun. 2006, pp. 1-6.

[14] H. Fujita, "A single-phase active filter using an H-Bridge PWM converter with a sampling frequency quadruple of the switching frequency," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 934-941, Jul. 2009.

[15] A. Kawamura, H. Fujimoto, and T. Yokoyama, "Survey on the real time digital feedback control of PWM inverter and the extension to multi-rate sampling and FPGA based inverter control," in *Proc. of the IEEE Ind. Electron. Society*, Nov. 2007, pp. 2044-2051.

[16] T. Yokoyama, M. Horiuchi, and S. Shimogata, "Instantaneous deadbeat control for PWM inverter using FPGA based hardware controller," in *Proc. of the IEEE Ind. Electron. Society*, Nov. 2003, pp. 180-185.

[17] D. Yang, X. Ruan, and H. Wu, "A real-time computation method with dual sampling mode to improve the current control performance of the LCL-type grid-connected inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4563-4572, Jul. 2015.

[18] L. Yiqiao and C. O. Nwankpa, "A new type of statcom based on cascading voltage-source inverters with phase-shifted unipolar SPWM," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1118-1123. 1999.

[19] M. B. d. Alvarenga and J. A. Pomilio, "Voltage balancing and commutation suppression in symmetrical cascade multilevel converters for power quality applications," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5996-6003. 2014.

[20] T. P. Corrêa, O. König, and R. Greul, "Multisampling in interleaved converters and modular multilevel converters," in *Proc. of the IEEE Ind. Electron. Society*, Oct. 2016, pp. 3500-3505.

[21] M. Odavic, V. Biagini, M. Sumner, P. Zanchetta, and M. Degano, "Low carrier-fundamental frequency ratio PWM for multilevel active shunt power filters for aerospace applications," *IEEE Trans. Ind. Appl.*, vol. 49, no. 1, pp. 159-167. 2013.