Active Thermal Cycle Reduction of Power Modules via Gate Resistance Manipulation

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***Abstract*—This paper discusses active thermal cycle reduction techniques for power electronic modules. These reduce the thermomechanical strain in the interconnects of the power module leading to an enhanced reliability and lifetime. For this purpose, a model based control algorithm is presented, which allows controlling the temperature of the devices within one half bridge. It uniquely uses a virtual heat sink to determine feasible trajectories for active thermal cycle reduction. This concept is the first to explicitly handle the limitations of the loss manipulation process for a multi-device module. Loss manipulation is realized least invasively by online manipulation of the gate resistance only. For temperature estimation with zero lag, a spatial observer structure is used. It demonstrates the feasibility of observer based active thermal control. The complete control algorithm is validated experimentally with a three phase power module on a load emulator using realistic load cycles.**

***Index Terms* - Thermal Control, Active Thermal Cycle Reduction, Adaptive Gate Drivers, Virtual Heat Sink, Reliability, IGBT**

I. Introduction

In the last decade the number of electric vehicles on our streets has grown from very little to reasonable number. All car manufactures present new models each year and the technology of electric propulsion is becoming mature. As a consequence a strong competition is about to rise about how to make the electric drive train smaller, lighter and cheaper without jeopardizing reliability.

A key concept which addresses this challenge is the active thermal control of power modules [1]. It allows the operation of power modules safely at thermal limits and aims to reduce the thermal cycles by smart manipulation of the losses of the devices or the cooling of the power module. Among the earliest contributions in this area, [2] discusses the question, how simple thermal models can be used to actively manipulate current and switching frequency, such that the power devices can be operated close to their thermal limits. After it was demonstrated by [3] that the degradation of power modules occurs primarily due to thermal cycling, in [4] a concept for thermal cycle reduction by active thermal control was patented. The potential of thermal cycle reduction to increase the lifetime of a power module over mission cycles has been demonstrated in [5], [6] by comparison of the estimated cycles to failure with and without active thermal control.

The first detailed scientific investigation of control concepts, which enable operation at thermal limits while reducing thermal cycles, has been presented in [7]. For that purpose, a region based active control law was presented which selects one control algorithm in the high-temperature regions, and another one in the power cycling region. Both control algorithms manipulate the switching frequency and the load current to regulate the junction temperature. The load current based loss manipulation can be realized in an electric drive train by variations of the flux linkage as illustrated in [8]. The thermal control concept from [7] has been enhanced in [9] and [10]. In [9] a relative temperature control of paralleled power modules is introduced. In [10] a loss modulator has been proposed to partition the thermal control and loss modulation process by manipulated input decoupling. This brings the great benefit that the thermal control law and the loss modulation algorithm can be designed independently.

In addition to the loss manipulation via current and switching frequency, it is also an option to manipulate the modulation scheme via zero sequence injection. This techniques has been employed together with switching frequency manipulation in a hysteresis controller on device temperature in [11]. Alternatively, the cooling can be manipulated by variation of the flow rate of the coolant, which is illustrated in [12]. This exhibits the advantage that no additional losses are generated within the device. However, the bandwidth of this approach is limited.

Another promising approach for loss manipulation uses adaptive gate drivers. In [13] an overview of possible architectures, models and hardware for gate driver based active thermal cycle reduction is given. It was demonstrated that the thermal transient of a load step can be reduced by an increment of the gate resistance from one value to another. In [14] a two step gate driver has been developed for a GaN dc-dc converter. It changes the switching instant gradually to manipulate losses and is supposed to be used for active thermal cycle reduction. A three-stage gate driver circuit for silicon IGBTs has been presented in [15] for active loss minimization. It intensively investigates the effect of different gate resistances and switching instants to manipulate losses. A gate driver circuitry with adaptive gate resistances is proposed in [16] to reduce the thermal cycles at the fundamental frequency of the inverter. This has been achieved by selecting a small, medium or large gate resistance dependent on the device current. These concepts demonstrate the potential of gate driver based loss manipulation for active thermal cycle reduction, but they do not address the model based loss manipulation within a multi-device power module.

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This work has three objectives that address limitations of the presented state of the art technology. The first objective is the model based loss manipulation of IGBTs via resistances manipulation. This picks up on the ideas discussed in [13]–[16] as it uses a gate drive with adaptive gate resistances. However, in this work the gate driver is interface with a model based loss manipulation unit that allows to command device losses within a multiple device power module. The second objective is to derive a control algorithm for active thermal cycle reduction of a power module with multiple devices taking into account the limits of loss manipulation. For this purpose, the concept of a virtual heat sink is used because it automatically generate feasible temperature trajectories. This generalizes the low pass concept, which has been used in [7], [10], [17] for trajectory generation, and the virtual heat sink concept, which was initially discussed in [9]. As a third objective, a thermal observer, that was developed in [18], is used to control the active thermal cycles of a three phase inverter module. It estimates the device temperature, averaged over one excitation period, with zero lag based on models and a temperature sensor. Thereby, active thermal control with high bandwidth is feasible. The control and active gate driver concepts, which are presented in this work, were experimentally validated for IGBTs using the Hybridpack2 (HP2) power module that has been intensively characterized in [19]–[21]. The power module was operated interfaced to a load emulator over realistic mission profiles to investigate the performance of the control algorithms.

II. Lifetime Enhancement by Active Thermal Cycle Reduction

The degradation of power electronic modules is primary driven by thermomechanical strain at its interconnects, for example the bond wires, solder layers or substrates. It occurs due to a mismatch in the coefficients of thermal expansion of interfacing material layers.

A. Classification of Thermal Cycles

The thermal cycles of a three phase inverter module within an electrical driver train can be classified in two types. The first type of cycles occur at the excitation frequency f_0 and are a result of the sinusoidal current. It is difficult to reduce these cycles for IGBT power modules by loss manipulation, because there is only current in each device for half of the excitation period. There are approaches, which aim to actively reduce these cycles by switching loss manipulation as discussed in [16]. However, it is usually most effective to keep the losses all time as small as possible to reduce these cycles. Note that this limitation does not hold for devices which allow bidirectional current conduction e.g. MOSFETs.

The second type of thermal cycles occur due to variations of the load. They are induced in the frequency range below the excitation frequency. It are these cycles of the averaged power module temperature, which are actively reduced in this work. The power module temperatures, which are averaged over one excitation period, do not reflect the thermal cycles at excitation frequency anymore. For that reason, these *averaged temperatures* are used as a control variable in the control algorithms presented in this work.

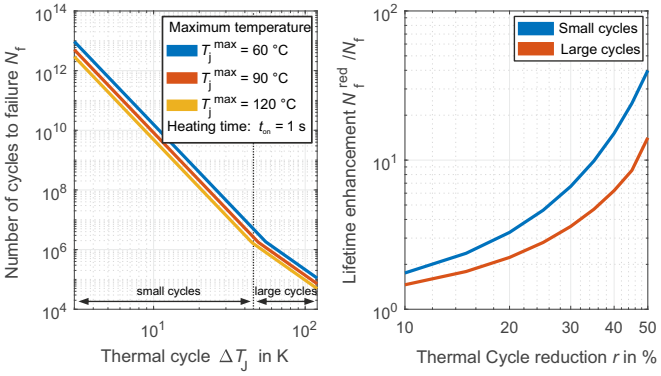

Fig. 1. Cycles to failure and lifetime enhancement plot of the Hybridpack2

To make the averaged temperatures available, they are estimated with a thermal observer, presented in [18]. The thermal observer structure eliminates the thermal cycles at excitation frequency and allows the estimation of the averaged temperatures of a power module with zero lag. Without the zero-lag estimates of the averaged device temperature, obtained form the observer, an effective active cycles reduction is hard to achieve. Alternative methods for averaged temperature estimation, based on low pass filters, always induce lag and degrade the performance of the thermal control algorithm.

B. Lifetime Estimation

The impact of thermal cycles on the lifetime of power modules has been first formulated in [3] using an empirical model, that was derived based on power cycling test results. It has been further refined in [22] taking into account more factors, that influence aging. Manufacture information, including active and passive cycling data, which allow estimating the cycles to failure N_f of the HP2 power module, has been presented in [23]. Based on this information, the following empirical lifetime model can be formulated in analogy to [3], [22].

$$N_\mathrm{f} = \begin{cases} a_1 \cdot \Delta T_\mathrm{j}^{-\mathrm{b}_1} \cdot \exp\left(\frac{E_{\mathrm{a},1}}{k_\mathrm{b} T_\mathrm{j}^{\max}}\right) \cdot f(t_{on}) & \text{if } \Delta T_\mathrm{j} \leq 45\ \mathrm{K} \\ a_2 \cdot \Delta T_\mathrm{j}^{-\mathrm{b}_2} \cdot \exp\left(\frac{E_{\mathrm{a},2}}{k_\mathrm{b} T_\mathrm{j}^{\max}}\right) \cdot f(t_{on}) & \text{if } \Delta T_\mathrm{j} > 45\ \mathrm{K} \end{cases} \tag{1}$$

$$f(t_{on}) = \begin{cases} 2.25 & \text{if } t_\mathrm{on} \leq 0.1\ \mathrm{s} \\ \left(\frac{t_{on}}{1.5\ \mathrm{s}}\right)^{-0.3} & \text{if } 0.1\ \mathrm{s} \leq t_\mathrm{on} \leq 60\ \mathrm{s} \\ 0.33 & \text{if } t_\mathrm{on} \geq 60\ \mathrm{s} \end{cases} \tag{2}$$

The cycles to failure N_f are a function of the the junction temperature cycle ΔT_j, the maximum temperature of the power module during cycling $T_\mathrm{j}^{\max}$ and the heating interval t_on. The coefficients of the aging law are summarized in Tab. I. The cycles to failure are plotted as a function of the thermal cycles ΔT_j for a range of maximum temperatures $T_\mathrm{j}^{\max}$ and a heating time of $T_\mathrm{on} = 1$ s in Fig. 1 (left). This plot and its fundamental equations (1) and (2) demonstrate that the

TABLE I
COEFFICIENTS OF THE EMPIRICAL LIFETIME MODEL FROM [23]

a_1	a_2	b_1	b_2	$E_{a,1}$	$E_{a,2}$	k_b
$1.4 \cdot 10^{12}$	$1.4 \cdot 10^{10}$	5.3	3.6	0.22 eV	0.15 eV	86 µeV/K

empirical lifetime of the power model can be increased by thermal cycle reduction.

C. Potential of Active Thermal Cycle Reduction

To investigate the potential lifetime increment, which can be achieved by active thermal cycle reduction, (1) can be used to formulate the lifetime enhancement (3).

$$\frac{N_\mathrm{f}^\mathrm{red}}{N_\mathrm{f}} = \left(\frac{\Delta T_\mathrm{j}^\mathrm{red}}{\Delta T_\mathrm{j}}\right)^{-\mathrm{b}} = \left(\frac{1}{1-r}\right)^{\mathrm{b}} \tag{3}$$

It is plotted in Fig. 1 (right) and determines the ratio of the cycles to failure with cycle reduction $N_\mathrm{f}^\mathrm{red}$ and without cycles reduction N_f as a function of the percentage of cycle of reduction r. The plot illustrates that even active cycles reduction in the range of 10 % to 35 % can contribute to a lifetime enhancement of $N_\mathrm{f}^\mathrm{red}/N_\mathrm{f} = 2$ to 10. This demonstrates, that even comparatively small manipulations by an active thermal control law make a difference. An additional detail, which emphasizes the potential of active thermal cycle reduction, is that the lifetime enhancement purely relies on the aging coefficient b. In case of the Hybridpack2 at small cycles it is 5.3, whereas for larger cycles it is reduced to 3.5. The comparison of this aging coefficient b with other contributions, which investigated power cycling of silicon IGBT modules e.g. [3], [22], [23], shows that b is always in the range between 4.5 and 5.5. In [22] even a confidence interval $\Delta b = 0.25$ is given for this coefficient comparing various different IGBT modules. This demonstrates, that despite the fact that the cycles to failure have been significantly increased in power modules over the last decade, the potential of active thermal cycle reduction is similar for most silicon IGBT power modules independent of their technology.

III. MODEL BASED LOSS MANIPULATION VIA ADAPTIVE GATE RESISTANCES

A gate driver circuitry with adaptive gate resistances provides an excellent tool to manipulate switching losses for active thermal control without interference of the inverter operation. In the following, the gate driver unit, which is used for that purpose, is introduced. Afterwards, the model based loss manipulation process is illustrated..

A. Adaptive Gate Driver Circuitry

In this work six adaptive gate drivers are used to manipulate the switching losses of the IGBTs within the three phase Hybridpack2 (HP2) power module. The schematic of one gate driver unit, which is depicted in Fig. 2, is shown in Fig. 3. The galvanically isolated power supply, which supplies voltages of -10, +3.3 ,+15 V for the gate driver output stage and the Complex Programmable Logic Device (CPLD), is realized

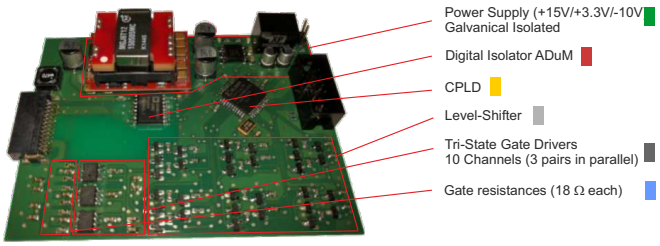

Fig. 2. IGBT driver unit of one IGBT

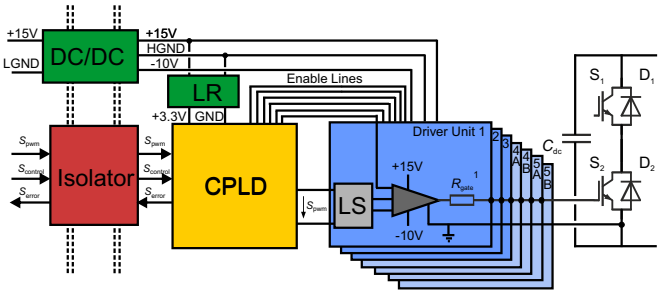

Fig. 3. Schematic of one IGBT driver unit

with a MGJ6T12 DC-DC converter from Murata and a linear regulator (LR). The digital signal isolation was realized with a four channel ADuM1400 IC. A XC9572XL CPLD from Xilinx was used to implement the adaptive gate resistance selection. The output stage circuitry has been derived from the gate driver unit that was presented in [24]. It exhibits 10 channels, each connected via a discrete level shifter and IXDD604SIA tri-state gate driver unit from IXYS to an 18 Ω gate resistance. For simplicity, the same gate resistance is used for turn-on and turn-off. Three channel pairs (1,2,3) are always paralleled and have a effective resistance of 9 Ω. The remaining four channels (4A,4B,5A,5B) can be addressed independently with a resistance of 18 Ω.

Each gate driver unit receives one standard PWM signal which is passed to the IGBT. In addition, a second PWM signal at a defined frequency of 8 kHz is passed to the CPLD, which exhibits information about the effective gate resistance $R_\mathrm{g}^\mathrm{eff}$ to be applied. To realize a wide range of effective gate resistances $R_\mathrm{g}^\mathrm{eff}$ and to spread the loss dissipation in the small 0603 SMD resistance packages, there is always a sequence of four intervals applied. After each PWM interval the output resistance combination is adjusted, such that an effective resistance is manipulated over four switching periods. In Tab. II all sequences with the associated resistance combinations applied after one other and the resulting effective gate resistances are summarized.

To apply the right resistance, firstly, the CPLD determines the width of the PWM pulse d_R and selects the sequence which leads to the commanded effective resistance $R_\mathrm{g}^\mathrm{eff}$. A state machine has been implemented on the CPLD that applies the correct gate resistance combination each PWM-interval. After the sequence is completed, the process is repeated. Each duty cycle d_R of the second PWM channel is mapped monotonically increasing to a higher effective gate resistance

TABLE II
SEQUENCES OF GATE RESISTANCE COMBINATIONS

No	Interval A	Interval B	Interval C	Interval D	R_g^{eff} in Ω
1	4A	4B	5A	5B	18
2	1	4A	4B	5A	15.75
3	2	5B	5A	3	13.5
4	1	2	3	4A	11.25
5	1	2	3	4	9
6	1	2	3	4,5B	8.25
7	1	2	3,5A	1,5B	7.5
8	1	2,4B	3,5A	1,5B	6.75
9	1,4A	2,4B	3,5A	1,5B	6
10	1,4A	2,4B	3,5	3,5	5.25
11	1,2	3,4	1,5	2,3	4.5
12	1,2,4A	1,3,4B	2,3,5A	1,2,5B	3.6
13	1,2,3	1,2,3	1,2,3	1,2,3	3
14	1,2,3,4A	1,2,3,4A	1,2,3,4A	1,2,3,4A	2.5
15	1,2,3,4,5A	1,2,3,4,5A	1,2,3,4,5A	1,2,3,4,5A	2
16	all	all	all	all	1.8

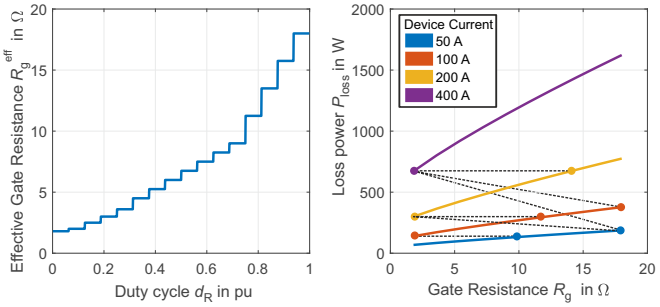

Fig. 4. Mapping of the duty cycle to the effective gate resistances (left) and loss generation of the HP2 IGBT as a function of the gate resistance and current for $f_{\text{sw}} = 5$ kHz $V_{\text{dc}} = 400$ V and $T_{\text{j}} = 40$ °C (right)

R_{g} to ensure robustness. This mapping is shown in Fig. 4. With this approach sixteen gate resistances, nearly equally distributed between 1.8 Ω and 18 Ω, can be commanded to manipulate losses.

In a standard application, for the Hybridpack2 a gate resistance between 1.5 Ω and 6 Ω is typically used. In this work, the lower bound of the resistance range is set to 1.8 Ω to avoid switching over-voltages at turn-off and large reverse recovery currents at turn-on. The upper bound of 18 Ω ensures that a blanking time of 3.5 µs is sufficient, such that one IGBT in a half bridge is completely turned off until the other IGBT turns on.

The functionality of the driver is illustrated in Fig. 5. The gate voltage v_{gate} and the collector emitter voltage v_{ce} are shown for the turn-on process of the driver unit with different gate resistance. It can be seen that large gate resistances slow down the charging process of the gate and lead to a reduction of the commutation speed. As a consequence, the switching losses increase nearly linearly with the gate resistance.

B. Switching Loss Model

This fundamental mechanism is reflected in the switching loss energy model of the HP2 power module, which has been derived and parameterized in [19] based on more than 700 measurements on a temperature controlled double pulse test

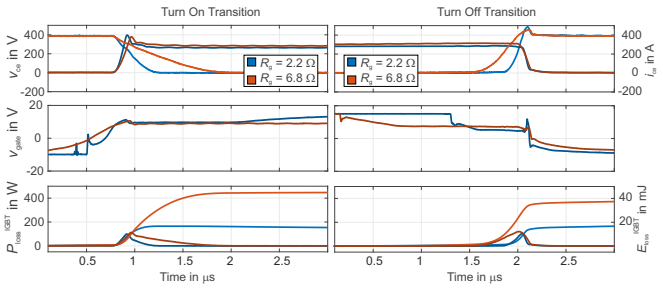

Fig. 5. Switching transients of the Hybridpack2 power module at $T_{\text{j}} = 25$ °C with two gate resistances

TABLE III
SWITCHING LOSS PARAMETERS OF THE HP2 POWER MODULE FOR THE REFERENCE POINT $V_{\text{dc}}^{\text{ref}} = 400$ V, $R_{\text{g}}^{\text{ref}} = 2.2$ Ω AND $T_{\text{j}}^{\text{ref}} = 20$ °C

E_0	K_0	α	β	K_{T}	E_0^{rr}	K_0^{rec}	$K_{\text{T}}^{\text{rec}}$
1.2 mJ	0.1 mJ/ A	1.75	0.82	1 µJ/ K	0.5 mJ	4.4 µJ/ A	0.02 1/ K

bench [25], [26] The loss energies of the IGBT and diode are given as a function of the device current i_{ce}, the dc-link voltage V_{dc}, the gate resistance R_{g} and the device temperature T_{j} according to (4) and (5).

$$E_{\text{sw}}^{\text{IGBT}} = E_0 + K_0 \cdot i_{\text{ce}} \cdot \left(\frac{V_{\text{dc}}}{V_{\text{dc}}^{\text{ref}}}\right)^{\alpha} \cdot \left(\frac{R_{\text{g}}}{R_{\text{g}}^{\text{ref}}}\right)^{\beta} + \Delta T_{\text{j}} \cdot K_{\text{T}} \quad (4)$$

$$E_{\text{sw}}^{\text{D}} = \left(E_0^{\text{rec}} + K_0^{\text{rec}} i_{\text{ce}} \left(\frac{V_{\text{dc}}}{V_{\text{dc}}^{\text{ref}}}\right)^{\alpha} \left(\frac{R_{\text{g}}}{R_{\text{g}}^{\text{ref}}}\right)^{-\beta}\right) \cdot (1 + \Delta T_{\text{j}} \cdot K_{\text{T}}^{\text{rec}})$$

$$\text{with } \Delta T_{\text{j}} = T_j - T_{\text{j}}^{\text{ref}} \text{ and } E_0^{\text{rec}} = E_0^{\text{rr}} \cdot \frac{V_{\text{dc}}}{V_{\text{dc}}^{\text{ref}}} \quad (5)$$

The parameters of the switching loss model are summarized in Tab. III. The entire device losses of the IGBT and the diode can be determined according to (6) and (7).

$$P_{\text{loss}}^{\text{IGBT}} = P_{\text{cond}}^{\text{IGBT}}(i_{\text{ce}}, T_{\text{j}}) + E_{\text{sw}}^{\text{IGBT}} \cdot f_{\text{sw}} \quad (6)$$

$$P_{\text{loss}}^{\text{Diode}} = P_{\text{cond}}^{\text{Diode}}(i_{\text{ce}}, T_{\text{j}}) + E_{\text{sw}}^{\text{Diode}} \cdot f_{\text{sw}} \approx P_{\text{cond}}^{\text{Diode}}(i_{\text{ce}}, T_{\text{j}}) \quad (7)$$

For the conduction loss model used in this work, it is referred to [18], [19]. Note that the switching losses of the diodes within the Hybridpack2 power can be often neglected as they are very small in comparison to the conduction losses.

The potential of adaptive gate resistance based thermal cycle reduction of an IGBT can be analyzed based on the presented model. Therefore, the device losses have been plotted in Fig. 4 as a function of the gate resistance R_{g} at different currents i_{ce}. It can be seen, in particular at higher currents, that the gate resistance has a major influence on the losses of the IGBT. Thermal cycling is directly caused by loss variation of the device, which occurs primarily due to changes of the device current. As a consequence, active cycle reduction by gate resistance manipulation can only be applied successfully, if these loss variation can be reduced. To illustrate the degree of freedom, which is gained by gate resistance manipulation, operational traces are indicated as dashed lines in Fig. 4 that minimize the loss variations when the device current changes. Fig. 4 demonstrates that the manipulation of the gate resistance can significantly reduce loss variations. At high currents, for

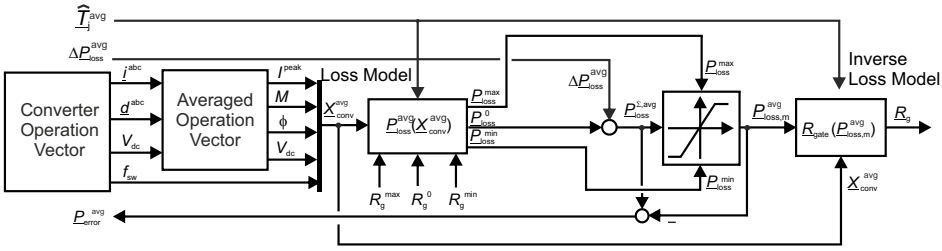

Fig. 6. Loss manipulation unit

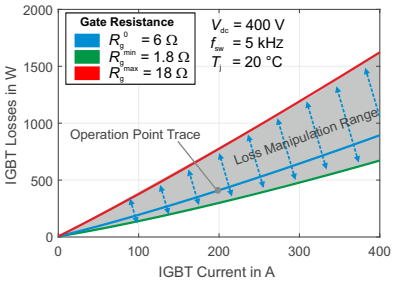

Fig. 7. Loss manipulation range

example at a load change from 200 A to 400 A, the losses can even be kept constant, if the gate resistance is adjusted.

In this work, the active thermal control of the averaged module temperatures is addressed. As the averaged model temperature is a result of the averaged losses, an averaged loss model is essential. The average switching losses of the IGBT over one fundamental electrical period can be determined via (8) assuming a purely sinusoidal load current with an amplitude of $\hat{I}$ and neglecting the temperature variation over te fundamental period.

$$\begin{aligned}\frac{\bar{P}_{\mathrm{sw}}^{\mathrm{IGBT}}}{f_{\mathrm{sw}}} &= \int_{t_0}^{t_0+T_0} E_{\mathrm{sw}}^{\mathrm{IGBT}}(i_{\mathrm{ce}},T_{\mathrm{j}},V_{\mathrm{dc}},R_{\mathrm{g}})\cdot f_{\mathrm{sw}}\,\mathrm{d}t \\ &= \left(\frac{E_0}{2}+\frac{K_0}{\pi}\hat{I}\left(\frac{V_{\mathrm{dc}}}{V_{\mathrm{dc}}^{\mathrm{ref}}}\right)^{\alpha}\left(\frac{R_{\mathrm{g}}}{R_{\mathrm{g}}}\right)^{\beta}+\Delta T_{\mathrm{j}}\frac{K_{\mathrm{T}}}{2}\right) \end{aligned} \tag{8}$$

The averaged switching losses of the diode can be derived analogously via (9).

$$\frac{\bar{P}_{\mathrm{sw}}^{\mathrm{D}}}{f_{\mathrm{sw}}} = \left(\frac{E_0^{\mathrm{rec}}}{2}+K_0^{\mathrm{rec}}\frac{\hat{I}}{\pi}\left(\frac{V_{\mathrm{dc}}}{V_{\mathrm{dc}}^{\mathrm{ref}}}\right)^{\alpha}\left(\frac{R_{\mathrm{g}}}{R_{\mathrm{g}}^{\mathrm{ref}}}\right)^{-\beta}\right)\cdot(1+\Delta T_{\mathrm{j}}\cdot K_{\mathrm{T}}^{\mathrm{rec}}) \tag{9}$$

Although they are too small to be actually used for the active control of the diode, they still contribute to the heat dissipation of the power module. For more information on the conduction loss model, which is used in in this work, as well as on the switching loss model it is referred to [18], [19].

C. Loss Manipulation Unit

For active thermal cycle reduction via IGBT gate resistance manipulation positive and negative loss commands $\Delta\underline{\boldsymbol{P}}_{\mathrm{loss}}$ with respect to the operation point losses $\underline{\boldsymbol{P}}_{\mathrm{loss}}^{0}$ must be realized. The operation point losses $\underline{\boldsymbol{P}}_{\mathrm{loss}}^{0}$, that are plotted in Fig. 7, are the losses that occur during operation with the gate resistance of $R_{\mathrm{g}}^{0}=7\ \Omega$. This resistance is slightly larger than the gate resistance, which would typically be used for the power module operation, and therefore it creates more average losses. However, this is necessary to allow a reduction and increment of the device losses, as illustrated in Fig. 7, for the active thermal cycle reduction with the feasible gate resistances between $R_{\mathrm{g}}^{\mathrm{min}}=1.8\ \Omega$ and $R_{\mathrm{g}}^{\mathrm{max}}=18\ \Omega$.

The loss manipulation unit, which ensures proper loss manipulation of the six IGBTs within the power module based on the derived loss model, is depicted as a state block diagram in Fig. 6. The operation vector of the inverter, that exhibits load current $\underline{\boldsymbol{i}}^{\mathrm{abc}}$, duty cycle $\underline{\boldsymbol{d}}^{\mathrm{abc}}$, dc-link voltage V_{dc} and switching frequency f_{sw}, is passed to the loss manipulation unit, which firstly determines the averaged operation quantities. These include the peak current $\hat{I}$, the modulation index M and the angle between voltage and current φ. Based on these operational variables and the junction temperatures, which are estimated by the thermal observer, the loss model determines the average losses of all devices $\underline{\boldsymbol{P}}_{\mathrm{loss}}^{0}$ for the operation point gate resistance R_{g}^{0}. In addition, it calculates the maximum and minimum average losses $\underline{\boldsymbol{P}}_{\mathrm{loss}}^{\mathrm{max}}$ and $\underline{\boldsymbol{P}}_{\mathrm{loss}}^{\mathrm{min}}$, which can be realized within the feasible range of the gate resistances for the given operation point. The loss command from the thermal control unit $\Delta\underline{\boldsymbol{P}}_{\mathrm{loss}}^{\mathrm{avg}}$ is added to the operation point loss $\underline{\boldsymbol{P}}_{\mathrm{loss}}^{0}$. The result is clipped based on the estimated maximum and minimum losses to ensure that the loss command $\underline{\boldsymbol{P}}_{\mathrm{loss,m}}^{\mathrm{avg}}$ is feasible. Finally, an inverse loss model is used to determine the gate resistances $\underline{\boldsymbol{R}}_{\mathrm{gate}}$ which realizes the loss command $\underline{\boldsymbol{P}}_{\mathrm{loss,m}}^{\mathrm{avg}}$. The part of the commanded losses $\underline{\boldsymbol{P}}_{\mathrm{error}}^{\mathrm{avg}}$ that cannot not be realized is fed back to the thermal control law to ensure proper handling of this limit.

This model based loss manipulation unit realizes an effective *manipulated input decoupling* for a multi device power module. It interfaces the strongly crosscoupled loss generation process, such that it can be used as an *ideal* loss modulator, that creates commanded losses with unity gain and reports any unfeasible loss commands.

IV. Active Thermal Control via a Virtual Heat Sink

The objective of this work is to present a active thermal control framework based on a virtual heat sink. It allows the effective reduction of thermal cycles in the presence of system limits. In this work, the control framework is validated with the introduced variable gate resistance based loss modulator. However, it can be easily adapted to any other loss manipulation methods e.g. manipulation of switching frequency [7], modulation scheme [11] or reactive power [8].

A. Functional Principle

In the following, the functional principle of the virtual heat sink based thermal control framework is illustrated based on the state block diagram that is depicted in Fig. 8. All three phases of the power module are operated independently via identical paralleled thermal control structures Therefore, only the thermal control structure of one half bridge is discussed for simplicity. During the inverter operation the load profile,

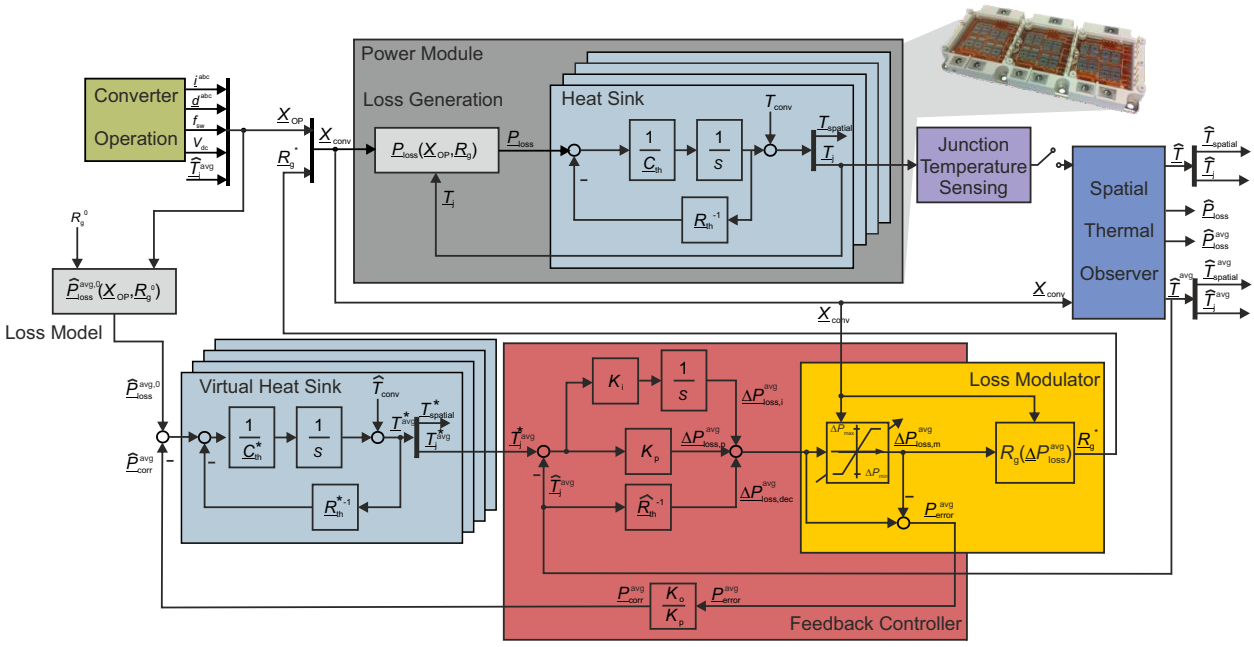

Fig. 8. Thermal control framework for active thermal cycle reduction

which consists of the load current i^{abc}, the duty cyle d^{abc}, the switching frequency f_{sw}, the dc-link voltage V_{dc} and the gate resistance R_{g} is applied to the power module. As a consequence, losses are generated in each device of a half bridge, which are concentrated in the loss vector $\underline{\boldsymbol{P}}^{\mathrm{loss}}$.

$$\underline{\boldsymbol{P}}_{\mathrm{loss}} = \left(\underline{\boldsymbol{P}}_{\mathrm{loss}}^{\mathrm{IGBTA}}\,\underline{\boldsymbol{P}}_{\mathrm{loss}}^{\mathrm{DA}}\,\underline{\boldsymbol{P}}_{\mathrm{loss}}^{\mathrm{IGBTB}}\,\underline{\boldsymbol{P}}_{\mathrm{loss}}^{\mathrm{DB}}\right)^{\mathrm{T}} \tag{10}$$

The device losses are dissipated via the lateral layers of the power module and the pin-fin array to the coolant fluid, which exhibits a temperature T_{conv}. From the thermal perspective, the entire power module appears as a heat sink. The heat conduction results in a spatial temperature distribution throughout the power module $\underline{\boldsymbol{T}}_{\mathrm{spatial}}$ and the junction temperature of the devices, which are concentrated in the vector $\underline{\boldsymbol{T}}_{\mathrm{j}}$.

$$\underline{\boldsymbol{T}}_{\mathrm{j}} = \left(\underline{\boldsymbol{T}}_{\mathrm{j}}^{\mathrm{IGBTA}}\,\underline{\boldsymbol{T}}_{\mathrm{j}}^{\mathrm{DA}}\,\underline{\boldsymbol{T}}_{\mathrm{j}}^{\mathrm{IGBTB}}\,\underline{\boldsymbol{T}}_{\mathrm{j}}^{\mathrm{DB}}\right)^{\mathrm{T}} \tag{11}$$

A spatial thermal observer structure, which is introduced in [18], is used to estimate the averaged temperatures throughout the power module with zero lag. The averaged device temperature estimates with zero lag, provided by the observer, are the control variables for the active thermal control algorithm presented in this work. For this reason, the observer is very important for the effective realization of the thermal controller. It allows separating load cycles, which this work aims to actively reduce, from the fundamental cycles, that occur at the electrical excitation frequency of the converter. If no observer was used, the average junction temperature would have been determined by low pass filtering the measured transient junction temperature. However, this results in a large lag of the average junction temperature and thereby degrades the performance of the thermal control system.

Another feature of the observer is, that it can estimate the power module temperatures either open loop or closed loop. For open loop estimation it requires information on the operation vector $\underline{\boldsymbol{X}}_{\mathrm{conv}}$ of the system only. For a closed loop temperature estimation, which provides a better estimation accuracy, the transient junction temperature $\underline{\boldsymbol{T}}_{\mathrm{j}}$ must be extracted e.g. using a junction temperature sensing method [27].

The most important aspect for active thermal cycle reduction is the generation of a good junction temperature reference $\underline{\boldsymbol{T}}_{\mathrm{j}}^{\mathrm{avg}*}$. On the one hand, the reference shall reduce thermal cycles, and on the other hand it must take into account the limits of the system i. e. the limits of the loss modulation unit. In this work a *virtual heat sink* is used for that purpose. The virtual heat sink is a modified model of the physical heat sink. It exhibits the same static characteristics, which are modeled with the thermal resistance matrix $\underline{\boldsymbol{R}}_{\mathrm{th}}^{*}$. However, its thermal capacitances, modeled in the capacitance matrix $\underline{\boldsymbol{C}}_{\mathrm{th}}^{*}$, are enhanced. The virtual heat sink is fed with the estimated averaged losses $\hat{\underline{\boldsymbol{P}}}_{\mathrm{loss}}^{\mathrm{avg},0}$ of the power module for the operation point gate resistance $R_{\mathrm{g}} = R_{\mathrm{g}}^{0}$, which is 6 Ω in this work. The temperature vector $\underline{\boldsymbol{T}}_{\mathrm{j}}^{\mathrm{avg}*}$ of the virtual heat sink exhibits reduced thermal cycles in comparison to the the physical heat sink due to the enhanced virtual capacitances. For that reason, the virtual temperature vector $\underline{\boldsymbol{T}}^{\mathrm{avg}*}$ is an ideal reference for feasible active cycles reduction. The derivation of the virtual heat sink model from the physical power module ensures, that by more or less enhancement of the virtual thermal capacitances, a desired thermal cycle reduction can be achieved. Furthermore, the thermal resistances $\underline{\boldsymbol{R}}_{\mathrm{th}}^{*}$, which are inherited from the physical model, ensure that the thermal cross-coupling between the devices is taken into account in the virtual heat sink. This is important to avoid that the created

TABLE IV
THERMAL MODEL CHARACTERISTICS OF THE HP2 POWER MODULE

Device	τ in s	C_{th} in $\frac{\mathrm{J}}{\mathrm{K}}$	R_{th} in $\frac{\mathrm{K}}{\mathrm{W}}$	$R_{\mathrm{th}}^{\mathrm{cross}}$ in $\frac{\mathrm{K}}{\mathrm{W}}$
IGBT	0.26	3.25	0.08	0.024
Diode	0.15	1.26	0.115	0.024

junction temperature references $\underline{\boldsymbol{T}}_{\mathrm{j}}^{\mathrm{avg}*}$ are far away from the physical ones, such that the thermal control task is unfeasible.

The device temperature reference $\underline{\boldsymbol{T}}_{\mathrm{j}}^{\mathrm{avg}*}$, which is generated by the virtual heat sink, as well as the averaged device temperature estimates from the observer, are passed to the thermal feedback controller. It exhibits a proportional and integral (PI) feedback loop on the estimated junction temperature $\underline{\hat{\boldsymbol{T}}}_{\mathrm{j}}^{\mathrm{avg}}$ and a state feedback decoupling path. The feedback regulator determines a loss command $\Delta\underline{\boldsymbol{P}}_{\mathrm{loss}}^{\mathrm{avg}}$ that is passed to the loss modulator. In case the loss command is feasible, the loss modulator commands a gate resistance that realizes the losses in the power module. In this situation the virtual heat sink works as a normal trajectory filter, that creates a references for the controller. If the loss command is only partially feasible, the fraction of the loss command that could not be realized $\underline{\boldsymbol{P}}_{\mathrm{err}}^{\mathrm{avg}}$ is passed via a feedback path to the virtual heat sink. Due to this loss error feedback, the junction temperature of the virtual heat sink $\underline{\boldsymbol{T}}_{\mathrm{j}}^{\mathrm{avg}*}$ starts to follow the temperature in the physical heat sink $\underline{\boldsymbol{T}}_{\mathrm{j}}^{\mathrm{avg}}$ until the control system runs out of the limitation of the loss modulation process. Thus, the presented control structure allows the reduction of thermal cycles in the presence of loss manipulation limits.

B. Virtual Heat Sink Design

For the realization of the virtual heat sink any kind of model of the power module can be used. This can range from a simple Cauer-model, which is extracted from datasheet parameters, to a spatially resolved 3D model. However, the model should exhibit a structure which allows an easy modification of the thermal capacitances. In this work, the model has been derived from a spatial thermal state space model, that is presented in [18] and that is also used in the thermal observer structure. It exhibits four inputs and outputs that are representing the heat dissipation and temperature at the four devices of a half bridge. For the model derivation, firstly, the static transfer characteristic $\boldsymbol{R_{\mathrm{th}}}$ has been derived from the original model. Afterwards, the original model has been reduced by balanced truncation [28] to two first order single-input single-output models of the IGBT and the diode. These models allow the extraction of the effective thermal capacitances C_{th} and time constants τ of the IGBTs and the diodes. The extracted parameters, which characterize the thermal model, are summarized in Tab. IV.

This static and dynamic information was used to create a simple physically insightful model according to (12)

$$c \cdot \boldsymbol{\Gamma} \frac{\mathrm{d}\underline{\boldsymbol{T}}_{\mathrm{j}}^{\mathrm{avg}*}}{\mathrm{d}t} + \underline{\boldsymbol{T}}_{\mathrm{j}}^{\mathrm{avg}*} = \boldsymbol{R_{\mathrm{th}}} \underline{\hat{\boldsymbol{P}}}_{\mathrm{loss}}^{\mathrm{avg}} \tag{12}$$

The transfer matrix Γ is a diagonal matrix with the time constants as entries, whereas the input matrix $\boldsymbol{R_{\mathrm{th}}}$ reflects

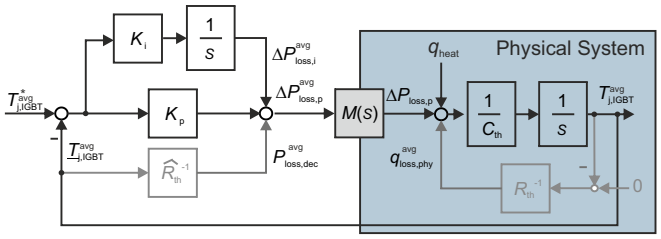

Fig. 9. State block diagram of the feedback controller of one IGBT

the static system behavior. The factor c has been added to effectively create virtual heat sinks with various thermal capacitances $\underline{\boldsymbol{C}}_{\mathrm{th}}^{*} = c \cdot \underline{\boldsymbol{C}}_{\mathrm{th}}$.

C. Control Design

The control design of the PI regulator, the state feedback decoupling path and the error feedback path are discussed for one IGBT as an example based on the state block diagram depicted in Fig. 9. The state block diagram illustrates the control unit and the physical heat sink, which has been approximated using a first order model with a thermal resistance R_{th} and a thermal capacitance C_{th}. The heat exchange between the IGBT with the other devices is modeled as a disturbance q_{heat}. The loss modulator is assumed to operate ideal $M(s) = 1$. For that reason, the error feedback path to the virtual heat sink $P_{\mathrm{error}}^{\mathrm{avg}}$ is not considered and will be addressed later. The thermal resistance R_{th} has been estimated and used to decouple the physical feedback path with $P_{\mathrm{loss,dec}}^{\mathrm{avg}}$. In addition, the proportional feedback gain K_{p} is selected such that it matches the thermal resistance estimate $K_{\mathrm{p}} = \hat{R}_{\mathrm{th}}$. Thereby, the original physical feedback gain, as well as the eigenvalues of the closed loop system, are not changed by the controller. However, the original virtual zero reference of this feedback path, which is explicitly drawn in Fig. 9, is replaced by the reference $T_{\mathrm{j,IGBT}}^{\mathrm{avg}*}$ from the virtual heat sink. This significantly improves the reference tracking without modification of the physical system behavior e.g. the response to q_{heat}.

The integral feedback path is finally added to ensure that the physical system follows the reference from the virtual heat sink. For its design the closed loop transfer function (13) of the state block diagram in Fig. 9 has been reviewed.

$$\frac{T_{\mathrm{j,IGBT}}^{\mathrm{avg}}(s)}{T_{\mathrm{j,IGBT}}^{\mathrm{avg}*}(s)} = \frac{K_{\mathrm{p}} s + K_{\mathrm{i}}}{s^2 C_{\mathrm{th}} + K_{\mathrm{p}} s + K_{\mathrm{i}}} \tag{13}$$

$$\text{with } K_{\mathrm{i}} = \frac{K_{\mathrm{p}}^2}{4 C_{\mathrm{th}}} \rightarrow s_{\mathrm{p1,2}} = -\frac{2K_{\mathrm{p}}}{C_{\mathrm{th}}} \tag{14}$$

The integral feedback gain K_{i} has been designed by (14) to enforce critical damping with maximum K_{i}.

Finally, the design of the error feedback path to the virtual heat sink $P_{\mathrm{error}}^{\mathrm{avg}}$ must be addressed. If the thermal control pushes the loss manipulator in saturation, the converter losses cannot be manipulated anymore and the control loop is opened. However, via the error feedback path to the virtual heat sink $P_{\mathrm{error}}^{\mathrm{avg}}$ another control loop is closed. In this situation, the regulator starts to control the virtual heat sink, to bring it back to the physical system. To guarantee, that this secondary

TABLE V
PARAMETERS OF THE VIRTUAL HEAT SINK AND FEEEDBACK GAINS

Device	R^*_{th} in $\frac{\mathrm{K}}{\mathrm{W}}$	C^*_{th} in $\frac{\mathrm{J}}{\mathrm{K}}$	K_{p} in $\frac{\mathrm{W}}{\mathrm{K}}$	K_{i} in $\frac{\mathrm{W}}{\mathrm{K\,s}}$	$\frac{K_{\mathrm{o}}}{K_{\mathrm{p}}}$
IGBT	0.08	$3.25 \cdot k$	12	12.5	c
Diode	0.115	$3.25 \cdot k$	0	0	c

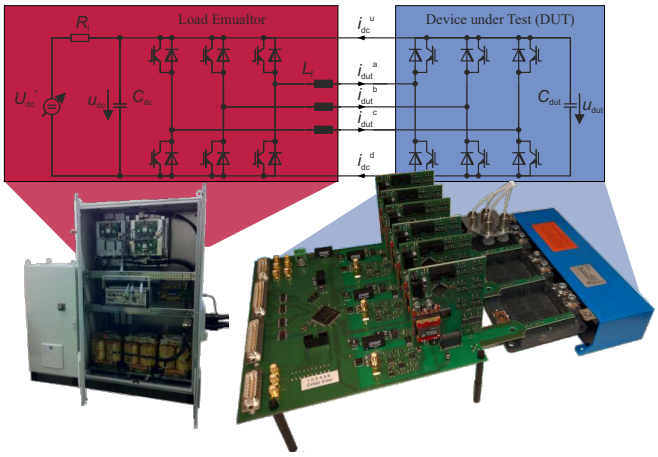

Fig. 10. Load emulator with Device under Test

control loop operates with the same dynamics as the primary control loop, the feedback gain is set to $K_{\mathrm{o}} = K_{\mathrm{p}} \cdot c$. This compensates the capacitance enhancement of the virtual heat sink, such that the secondary loop dynamics do not vary from the primary loop.

Following this design guidelines, the virtual heat sink and feedback gains summarized in Tab. V have been identified for the system. As the diode losses are not manipulated their feedback gains have been set to zero.

V. EXPERIMENTAL RESULTS

For the experimental validation of the proposed control structure, one decapsulated Hybridpack2 power module was operated with a load emulator. The topology of the resulting setup as well as images of the load emulator and the device under test (DUT) are depicted in Fig. 10. For the average temperature estimation a thermal observer structure was used, which is presented in [18]. It uses four infrared sensors to correct its temperature estimates. The DUT was operated with Ethylene-Glycol water coolant at a temperature of 20 °C, at a dc-link voltage of 100 V and a current controller [29] that operates with a PWM frequency of 9 kHz. The dc-link voltage was kept at 25 % of its rated value to prevent discharge processes within the decapsulated power module. This brings the disadvantage, that the loss manipulation capability of the gate driver is reduced by a factor of 10 according to (8). The control algorithm has been implemented in a C++ framework that is computed on a XCS2005 control system from AixControl with a Shark DSP from Analog Devices. The sampling and computation frequency was set to 1 kHz.

In Fig. 11 a repetitive load pattern has been applied with a current between 50 A and 250 A and at a fundamental

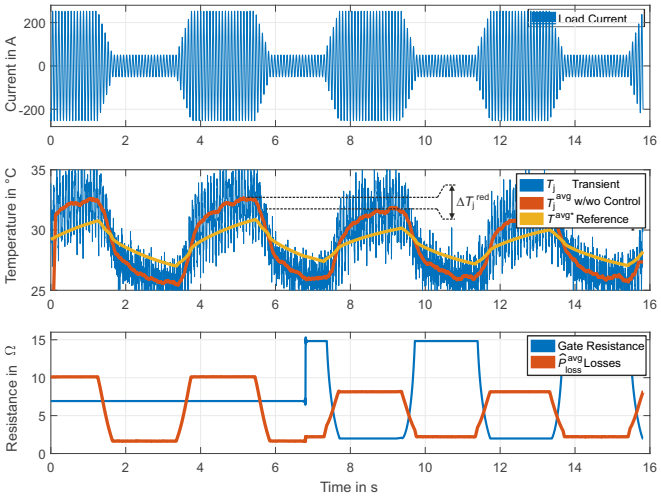

Fig. 11. Experimental evaluation of open loop observer based active cycle reduction of IGBTs at repetitive load cycles

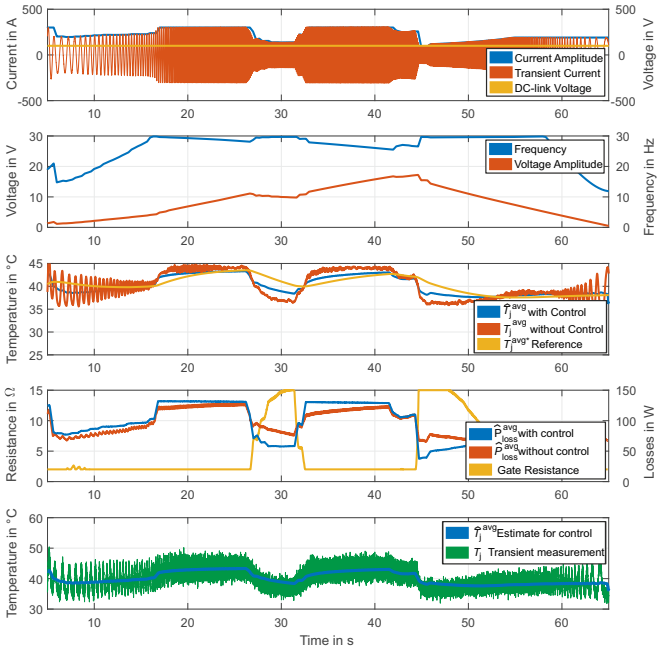

Fig. 12. Experimental evaluation of closed loop observer based active cycle reduction of IGBTs at realistic load cycles

frequency of 12 Hz. The phase voltage has been maintained at an amplitude of 20 V at a power factor of $\cos(\varphi) = 1$. The transient and averaged temperature of one IGBT are shown as well as the temperature reference from the virtual heat sink. After $t = 7$ s the active cycle reduction algorithm has been activated using the open loop estimates from the observer. From this time on, the gate resistance is manipulated and the thermal cycle of the junction temperature is reduced from 7.3 K to 5.8 K by 20 %.

In a second experiment, whose results are shown in Fig. 12, a complex load profile is used and the closed loop observer has been applied. The experiment has been conducted with the active thermal control algorithm and without. In the last trace,

it is shown that the observer accurately estimates the average junction temperature of the IGBT. The thermal control unit uses the estimates to reduces the thermal cycles effectively with active gate resistance manipulation trying to mimic the behavior of the virtual heat sink..

To understand, why the experimentally demonstrated moderate active thermal cycle reduction of 20 % is a remarkable and encouraging result, it must emphasized that all experiments were conducted at 25 % of the rated voltage. The significantly increased loss manipulation ability at rated voltage will significantly increase the performance of the active thermal cycle reduction techniques presented in this work.

VI. Conclusion

This work has demonstrated the feasibility of active thermal cycle reduction via gate resistance manipulation. A control framework has been presented that effectively reduces thermal cycles of large scale power modules in the presence of limits. It uses the concept of a virtual heat sink to create feasible temperature trajectories for the thermal feedback controller. The design process of the virtual heat sink and the controller has been illustrated. A thermal observer has been successfully applied for observer based active control of the averaged device temperatures. All thermal control techniques, that have been proposed in this work, have been experimentally evaluated on a three phase power module with a load emulator by injection of realistic load profiles.

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