Noise Mitigation and Delay Compensation in High Frequency Dual Current Programmed Mode Control

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***Abstract*—To overcome the increased switching losses in high frequency power electronics, control-based modulation techniques such as boundary current mode (BCM) are commonly used in full bridge inverter and rectifier topologies to guarantee zero voltage switching (ZVS). Traditionally, in order to implement BCM modulation, a combination of current programmed mode (CPM) control and model-based techniques are used. The former is highly susceptible to noise and sensing delay, while the latter is subject to modeling error. In this work, a dual-current programmed mode (DCPM) control circuit for BCM operation is designed and implemented. The proposed control network achieves better noise immunity and low propagation delay at high frequency while regulating peak and valley currents in each period. The operation of this control scheme is demonstrated experimentally using a GaN-based half bridge inverter prototype.**

I. Introduction

In recent years, there has been a push toward small and lightweight converters, driving research in high frequency and high efficiency power conversion. However, operating converters at high switching frequency result in high switching losses and more severe electromagnetic interference (EMI) [1]. To overcome these challenges, soft switching techniques such as boundary current mode control (BCM) have been widely used in inverters and rectifiers to realize zero voltage switching (ZVS) operation [2]–[8]. In the half bridge topology shown in Fig. 1, the parasitic drain-to-source capacitors C_{ds1},C_{ds2} of the transistors and the inductor L form a resonant network during the switching dead time enabling soft switching transitions [9], [10].

To achieve ZVS operation with minimum current stresses during the positive line cycle, the inductor current is controlled to follow the envelop wave shape shown in Fig. 2 with enough negative current during the dead time to achieve ZVS. One traditional implementation of this is the dual-current programmed mode (DCPM) control loop shown in Fig. 3.

A combination of current-sensing resistor, differential amplifier, comparators, and flipflop are used for practical implementation. The analog and digital circuitry regulates the inductor current within a line-frequency envelope set by a controller through inductor current references $\pm I_{ref}$ [11]. Although the differential amplifier in the loop contains a low-pass filter characteristic that attenuates the high-frequency noise, the current control network is still prone to anomalous switching actions when subject to high dv/dt switching, as will be present in a GaN-based implementation [12]. In [13], several control techniques have been proposed to mitigate this issue; however, these control schemes are complicated for practical implementation. In addition to noise issues, propagation delays inherently introduced by components in the current loop cause the inductor current to overshoot its reference point. This results in extra unnecessary peak inductor current, and changes of the switching frequency [14]. To overcome both the issue of noise and propagation delay in BCM, a simple and low cost solution is proposed in this paper. The description of the proposed current mode control circuit, the characterization of propagation delay and current compensation implementation are outlined in Section II, followed with experimental results in Section III and conclusions in Section IV.

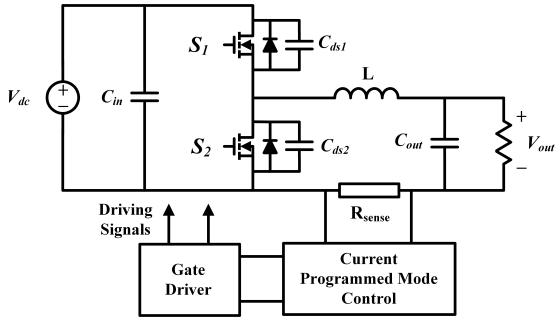


Fig. 1. Half-bridge inverter with current control loop.

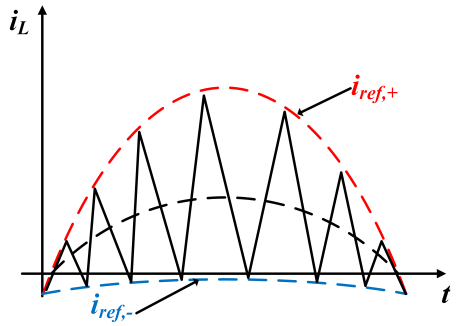


Fig. 2. Inductor current waveform.

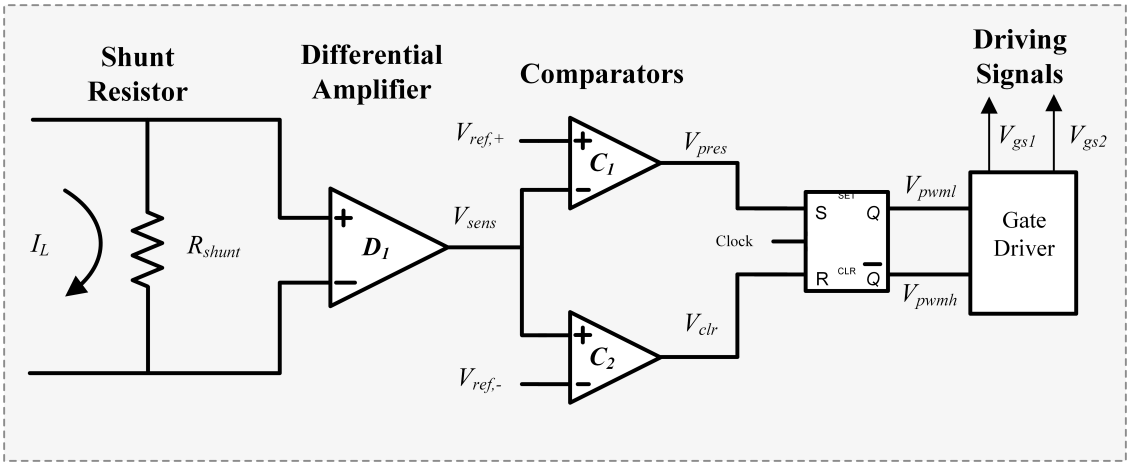


Fig. 3. Traditional dual current programmed mode control loop.

II. Principle of Operation

A. Noise Mitigation

The traditional DCPM implementation of Fig. 3 relies on instantaneous comparison between sensed inductor current V_{sens} and two low-frequency references, $V_{ref,+}$ and $V_{ref,-}$.

While this allows wide-bandwidth, cycle-by-cycle current regulation, it also results in high susceptibility to noise. Any oscillation in the sensed inductor current at or near the switching time will result in anomalous level transitions at the outputs of comparators C_1 and C_2. Due to parasitics in the sensing circuitry and nonidealities of the analog elements, such oscillations are observed following power stage switching.

Fig. 4 shows the diagram of the proposed improved DCPM control loop with additional switching noise immunity. One-shots B_1 and B_2 and AND gates A_1 and A_2 have been added to the traditional design of Fig. 3. These elements are used to create a controllable blanking time T_{blk} following each switching action to reject ensuing noise. The blanking time can be set such that T_{blk}, during which switching is prevented, is below the minimum required T_{on} or T_{off} during operation.

Ideal operation waveforms of the circuit are outlined in Fig. 5. For simplicity, the synchronization of the waveforms with the clock has been omitted. The effective transimpedance of the current sensing resistor and amplifier is

$$R_{sens} = \frac{V_{sens}}{i_L} = R_{shunt} \cdot H \tag{1}$$

where H is the voltage gain of D_1. Relative to Fig. 2, the current limits $i_{ref,\pm} \cdot R_{sens} = V_{ref,\pm}$

During the turn-on transition of S_2, the following events happen in sequence. Prior to the beginning of the transition, both one-shot B_1 and B_2 outputs are high. First, the sensed inductor current V_{sens} reaches the high reference $V_{ref,+}$; then, the comparator C_1 is triggered, causing its output $V_{cpr,pres}$ to change state from low to high. Second, the logic change of the comparator triggers two simultaneous events: (1) the output of the AND gate A_1 goes high tracking $V_{cpr,pres}$ and (2) the output of B_2 one-shot, $V_{blk,pres}$ is driven low. The output of B_2 remains low for the duration of T_{blk}, during which A_2 prevents high frequency switching noise from resetting the latch and causing an undesirable turn off of S_2. Third, after T_{blk}, the output of B_2 goes back to high, and the next switching action is ready to occur. In the next switching action, S_1 turns on, S_2 turns off and the entire process is repeated.

For proper operation of the logic circuit, T_{blk} should be set based on the highest expected switching frequency and should not exceed the lowest allowed switching interval, $T_{blk} \leq \min(T_{on}, T_{off})$. Though this implementation significantly improves switching noise immunity, it still requires that any parasitic ringing which couples into the sensing circuitry following a switching action is damped out prior to T_{blk}. If not achieved inherently, this constraint can be met by reducing sensing and power stage parasitics, adding additional filtering, or increasing T_{blk}. The latter may require reducing power stage maximum switching frequency.

B. Delay Compensation

Propagation delay introduced by the current control circuit presents challenges in BCM modulation. The current controller cannot immediately react when the current crosses the high and low references. Various delay mechanisms due to components between the sensing resistor and gate driver outputs cause time delay. This delay results in overshoot of the references which can quickly increase when the inductor current slope is large [2]. Fig. 6 shows representative waveforms of the effect of propagation delay on the inductor current. During the turn-on transition, $V_{ref,+}$ is the actual peak reference point that should initiate S_1 turn off transition. However, because of propagation delay t_{delay} in the control loop, the inductor current overshoots the reference as illustrated with the red dotted line of the sensed inductor current, resulting in a $\Delta V_{ref,+}$ error in the set reference. The propagation delay t_{delay} can be broken down into three components:

- t_{d1}: time delay of the comparator

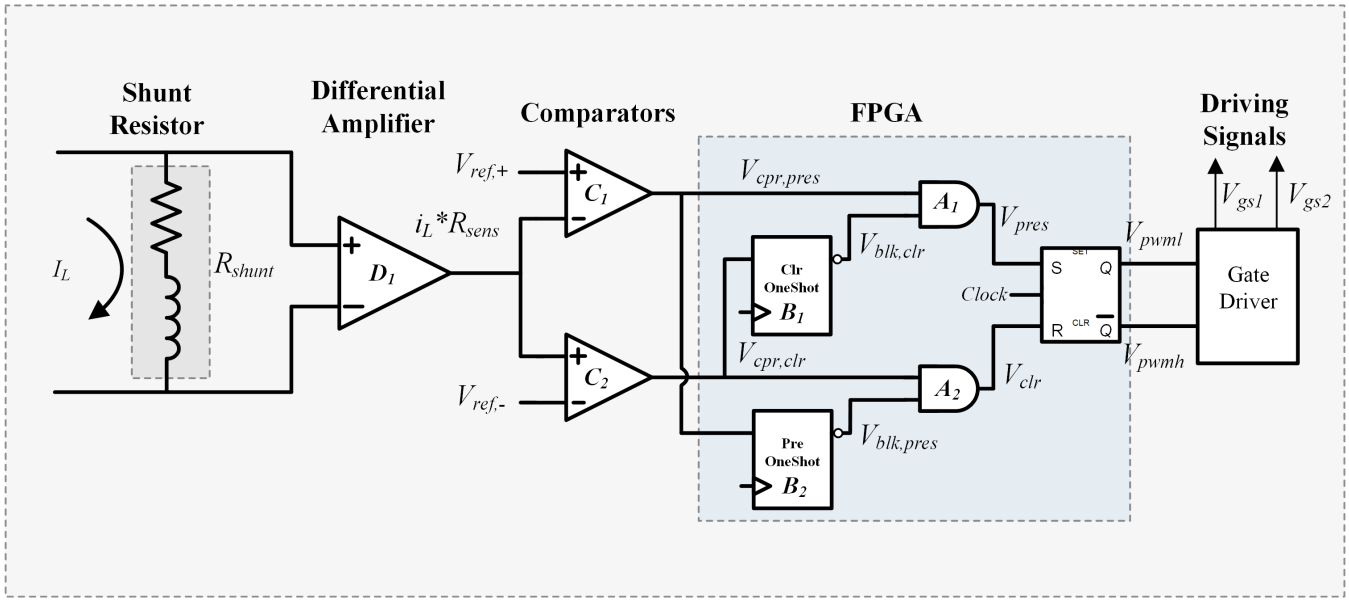


Fig. 4. Proposed dual current programmed mode control loop network.

- t_{d2}: time delay of the logic network consisting of the one-shot, AND gate and SR latch
- t_{d3}: time delay of the gate driver

t_{dt} represents the switching deadtime. The effect of deadtime is not considered part of the delay in this work, as its effect on current regulation can be compensated out using established techniques [12].

To minimize the overall propagation delay in the control loop, large bandwidth, high speed and noise-immune components are selected for the current control loop, including the gate driver. However, these efforts are limited by the nonideality of available components and current compensation techniques are required to account for the remaining delay in the loop. The logic network in the proposed DCPM control only contributes a nearly-constant 8 ns time delay in the control loop, with t_{d3} being the largest contributor of time delay.

In [14], a constant offset has been used in the reference signal to develop a hysteretic compensation method that achieved acceptable compensation over a limited range of operating points. However, the dynamic variation of di_L/dt in BCM operation results in a compensation magnitude that varies with operating point. During inverter operation, the slope of the inductor current during T_{on} is at its maximum at the zero crossing of the output voltage while at its minimum during the peak output AC voltage. Additionally, the inductor slope is different during each subinterval, with the slope during T_{on} determining the positive current overshoot, and the slope during T_{off} determining the undershoot of the negative reference. Additionally, sensing delays, in particular t_{d1} may vary significantly with di_L/dt. In high frequency applications, because of all of these dynamics, the inductor overshoot current can be on the order of several amps.

In order to eliminate this error, one approach is to dynamically adjust the comparator reference voltages to compensate a known time delay. Using the inductor positive slope as an example, to initiate S_1 turn-off at a set reference voltage $V_{ref,+}$, the compensated reference should be set to

$$V^*_{ref,+} = R_{sens}\left[i_{L,+} - t_{delay}\left(\frac{di_L}{dt}\right)\right] \tag{2}$$

where $R_{sens} \cdot i_{L,+}$ is the uncompensated reference and $R_{sens} \cdot t_{delay}(di_L/dt)$ is the offset to the reference voltage to compensate for the time delay.

In addition to time through the sensing circuitry, current regulation errors arise from parasitics in the sensing resistance. For fast-switching BCM modulation, minimal series inductance in the sensing resistor, as shown in Fig. 4 may result in significant distortion of the sensed voltage. The parasitic inductance, L_{shunt}, of the shunt resistor can additionally be compensated using the same technique. The resulting compensated reference voltage during T_{on} is

$$V^*_{ref,+} = R_{sens}\left[i_{L,+} - t_{delay}\left(\frac{di_L}{dt}\right)\right] + H \cdot L_{shunt}\left(\frac{di_L}{dt}\right) \tag{3}$$

Eliminating the term describing the intended reference, the dynamic compensation of the reference voltage is

$$\begin{aligned}\Delta V_{ref,+} &= V^*_{ref,+} - V_{ref,+} \\ &= (H \cdot L_{shunt} - R_{sens}t_{delay})\left(\frac{di_L}{dt}\right)\end{aligned} \tag{4}$$

Note that the effect of parasitic inductance of the shunt resistor counteracts the effect of time delay in the control loop.

Assuming a known inductance and online sensing of the input and output voltages, $\frac{di_L}{dt}$ can be calculated dynamically. By characterizing L_{shunt} and t_{delay} prior to deployment,

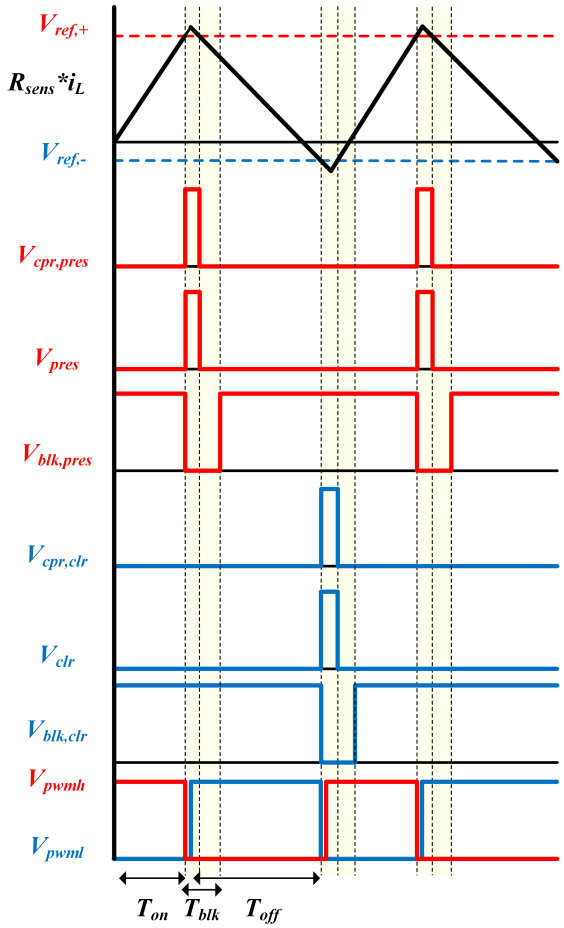


Fig. 5. Ideal waveform of proposed current control loop.

TABLE I
EXPERIMENTAL PROTOTYPE CONVERTER DESIGN

Parameter	Value
S_1, S_2	Panasonic GaN-GIT
L	26 μH
R_{shunt}	20 mΩ
Inductor Core Geometry	Toroid
Inductor Core Material	Mix No. 2 (Micrometal)
V_{dc}	400 V
P_{out}	500 W
f_{max}	800 kHz

the necessary compensation to a controller-provided reference $\Delta V_{ref,+}$ can be calculated online using (4) in the case of T_{on}. These calculations can be done online, or pre-calculated over a range of $\frac{di_L}{dt}$ and stored in a Look-Up-Table (LUT).

III. EXPERIMENTAL RESULTS

In order to further examine the impact of noise and control delay, and to validate the proposed solutions, a 500 W prototype experimental converter is constructed. The converter is a half-bridge, configured as shown in Fig. 1, with the DCPM control implementation of Fig. 4. Details of the converter power stage are given in Table I, and components used in the

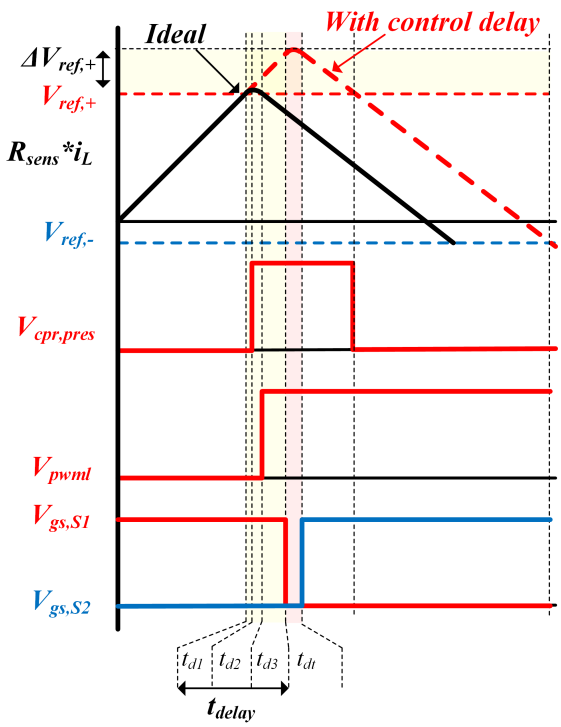


Fig. 6. Inductor waveform with propagation delay. In the top plot, the solid black line is the ideal waveform, and the dashed red line is the waveform when control circuit delays are considered.

TABLE II
EXPERIMENTAL PROTOTYPE CONTROL CIRCUIT COMPONENTS

Component	Part No.
Gate Driver	UCC21520
OpAmp	THS4509
Comparator	LTC6752-4
FPGA	XILINX Spartan 6

control circuitry are given in Table II. A photograph of the experimental prototype is shown in Fig. 7. The power stage is implemented using GaN-GIT devices from Panasonic Corporation and the measured efficiency in a DC-DC ZVS operation at a constant switching frequency of 500 kHz is shown in Fig. 8. The digital logic circuitry of the DCPM loop and the reference generation and compensation are implemented in a XILINX Spartan 6 FPGA.

Next, the converter is operated in BCM operation as illustrated in Fig. 2, resulting in a varying switching frequency ranging from 300 kHz to 800 kHz. The upper and lower boundaries of the inductor current are set using an FPGA to generate the subsequent voltage references. Fig. 9a shows the inductor current I_L, the sensed inductor current $V_{sens} = R_{sens} \cdot i_L$, and gate drive signals V_{pwmh}, V_{pwml} when using the traditional current mode control and the proposed current mode control with noise immunity. With the traditional approach, the effect of the noise during the inductor zero-current crossing is seen on the gate drive signals causing the active switch S_1 to exhibit anomalous switching actions. In

Fig. 7. Experimental prototype board

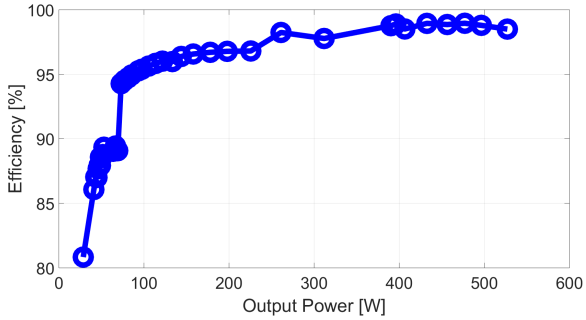
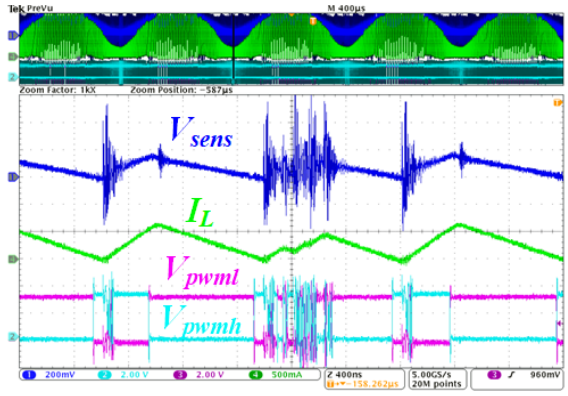
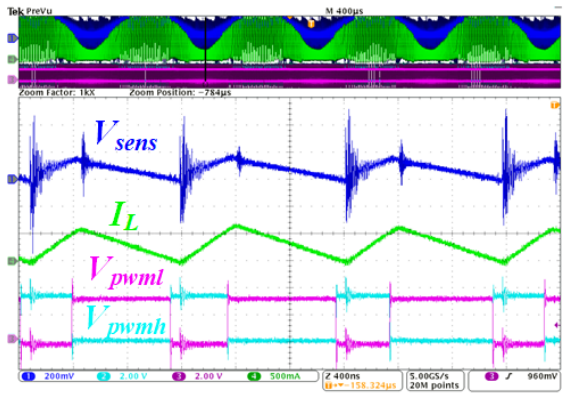


Fig. 8. Measured efficiency, $D = .5$, $V_{in} = 400$ V, $V_{out} = 200$ V, $f_{sw} = 500$ kHz



(a)



(b)

Fig. 9. Experimental result using (a) Traditional DCPM without blanking time and (b) proposed DCPM with blanking time.

Fig. 9b, the undesirable switching of S_1 is eliminated by using the proposed current loop with a blanking time of 290 ns. Both gate drive signals show no uncontrolled switching actions while operating at 800 kHz maximum switching frequency and 3.5 A peak inductor current.

Next, using a fixed upper and lower reference in a DC-DC type operation, the total delay of the proposed current loop is characterized experimentally in Fig. 10. The measured propagation delay from the current sensor to the output of the differential amplifier is minimal and has been excluded. The total propagation delay of the network including the gate driver is approximately 39 ns over the range of measured di_L/dt. The logic network in the proposed DCPM control only contributes about 8 ns time delay, while the comparator added 5 ns of delay, with the gate driver accounting for the majority of the propagation delay, up to 26 ns. .

Fig. 11 shows the measured inductor current I_L, the sensed inductor current V_{sens}, and the switch node voltage V_{sw}. During T_{on} and T_{off}, the parasitic inductance of the shunt resistor results in a voltage offset ΔV_e labeled in Fig. 11. To eliminate the effect of DC bias in the measured result, L_{shunt} has been approximated using

$$\Delta V_e = L_{shunt}\left[\left(\frac{di_{L1}}{dt}\right) - \left(\frac{di_{L2}}{dt}\right)\right] * H \qquad (5)$$

where H is the gain of the differential amplifier. From (5), L_{shunt} is approximately 1 nH in the prototype converter.

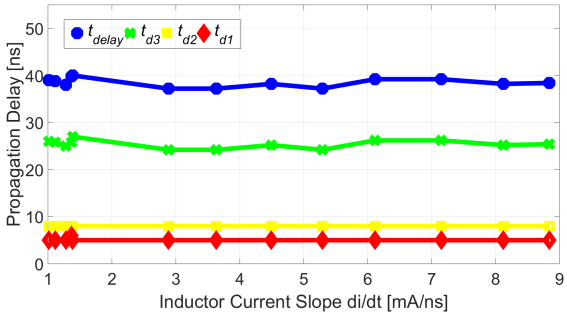


Fig. 10. Propagation delay characterization.

Fig. 12 shows the modeled compensation voltage $\Delta V_{ref,+}$ based on time delay with or without consideration of L_{shunt}. When L_{shunt} is not considered, as in (2), there is a significant increase in the reference compensation voltage with di_L/dt. However, when the effect of L_{shunt} is considered using (3), $\Delta V_{ref,+}$ is nearly flat and can be approximated as constant with respect to inductor current slope.

Experimental result of the inductor current compensation are shown in Fig. 13. The analytical predictions resulting from (3) are compared to experimental measurements of the actual $\Delta V_{ref,+}$ required to compensate current error. The latter

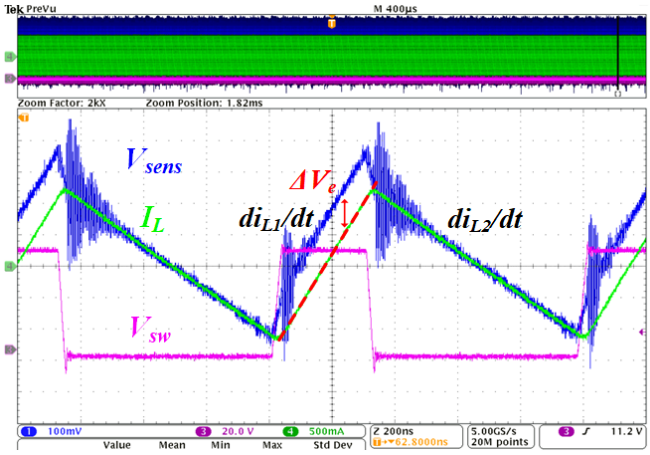


Fig. 11. Experimental result showing effect of parasitic on the sensed inductor current.

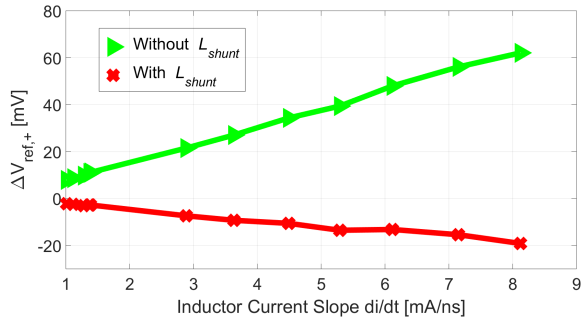


Fig. 12. Estimated compensation reference voltage $\Delta V_{ref,+}$ with or without parasitic inductance L_{shunt}

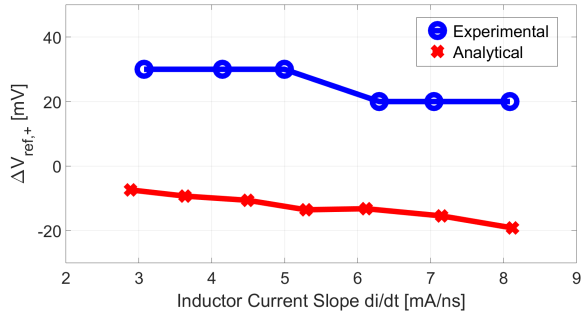


Fig. 13. Comparison between experimental and predicted compensation reference voltage $\Delta V_{ref,+}$

are obtained by manually tuning until switching occurs at a current of exactly $R_{sens} \cdot i_{L,+}$ As expected, $\Delta V_{ref,+}$ does not vary significantly with inductor current slope. However, there is significant offset between the analytical model and the experimental result that requires further research. Despite these discrepancies, it has been shown that a constant $\Delta V_{ref,+}$ can be used to compensate for the extra inductor current resulting from t_{delay} in the current control loop during T_{on}.

IV. Conclusions

An improved simple and low cost noise immunity and current compensation model to address noise and propagation delay challenges prevalent in boundary current mode control has been proposed. A combination of one-shot and AND gates are used to implement a blanking time that prevents the noise during the inductor zero current transition to interfere with the operation of the active switch. The proposed solution has been successfully demonstrated in an experimental GaN based half bridge inverter prototype that operates at a maximum frequency of 800 kHz and 3.5 A inductor peak current. The propagation delay of the proposed current control network has been characterized and a current compensation method that takes advantage of the parasitic inductance in the shunt resistor to estimate the compensation error has been proposed. Future research is needed to fine tune the proposed current compensation technique and integrate dead-time optimization into the proposed DCPM control.

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