Peak Offsetting Based CPM Controller for Multi-level Flying Capacitor Converters

Liangji Lu, S. M. Ahsanuzzaman, Aleksandar Prodić
Laboratory for Power Management and Integrated SMPS
ECE Department, University of Toronto
Toronto, ON, CANADA
liangji.lu@mail.utoronto.ca,
{ahsansm,prodic}@ece.utoronto.ca

Giacomo Calabrese, Giovanni Frattini, Maurizio Granato
Texas Instruments
Freising, GERMANY and Milan, ITALY
{g-calabrese,giovanni.frattini,maurizio.granato}
@ti.com

***Abstract*— This paper introduces a practical mixed-signal peak current programmed mode (CPM) controller suitable for emerging low-power dc-dc multi-level flying capacitor (ML-FC) converters. The controller eliminates the inherent instability problem of ML-FC converters associated with flying capacitor voltage runaway. The method is based on separate asymmetrical thresholds defining multiple inductor current peaks within one switching period. The effectiveness of the controller is verified through simulations and with a low-power 12 V to 1.8 V/1A, 3-level ML-FC experimental prototype.**

Keywords*— *cpm control, peak cpm, mixed-signal control, low-power dc-dc converter, flying capacitor

I. INTRODUCTION

Multi-level flying capacitor (ML-FC) converters, introduced by Meynard [1], for high power applications [2]–[3], have been recently investigated as an attractive alternative to predominantly used conventional, i.e., 2-level, dc-dc buck and boost topologies in numerous low-power applications [4]-[5], requiring power from a fraction of watt to few kilowatts. Benefits of multi-level converters such as switching node voltage reduction and frequency multiplication translate into physical size reduction and power processing efficiency improvements [5]. Nevertheless, a wider adoption of ML-FC converters in low-power dc-dc applications is slowed by several implementation challenges, including control issues. These issues are primarily related to the simultaneous regulation of the converter output voltage and balancing of the flying capacitor voltage [6] and not fully understood dynamics of realistic ML-FC. Recent publications, addressing pulse-width modulated voltage mode control, have pointed out the flying capacitor voltage stability problems in discontinuous conduction mode and in the presence of non-negligible ripple and proposed solutions for them [7]-[8]. Stability problems have been recognized for current programmed mode (CPM) operation, and in [9]-[11] it was indicated that valley-based CPM provides inherent flying capacitor balancing. In targeted cost-sensitive low-power applications, peak CPM is often preferred to the valley method, largely due to the inherent protection of the main transistor switches under fault condition. Furthermore, compared to the voltage mode control, the peak CPM provides simpler system dynamics.

This work of Laboratory for Power Management and Integrated SMPS is supported by Texas Instruments.

The main goal of this paper is to introduce a practical mixed-signal peak CPM controller for multi-level flying capacitor (ML-FC) converters that provides both stable output voltage regulation and balancing of the flying capacitor voltage. The controller of Fig. 1 provides stability of both the output and flying capacitor voltages in a 3-level buck converter through novel *Peak Offsetting Mechanism (POM)*. The *POM* is based on separate programming of two current peaks, corresponding to the two halves of a switching period. During a flying capacitor voltage disturbance, the two peaks (I_{CMD_1} and I_{CMD_2}) are offset by a quantity (ΔI_{CMD}) symmetrically in opposite directions centered around the current command steady state value (I_{CMD}), to achieve the stabilization of flying capacitor voltage.

The discussion is divided into three parts. A review of the problems with the peak CPM in ML-FC converters is given, and the fundamental principle of the peak CPM with *Peak Offsetting Mechanism (POM)* described. This part is followed by the description of a practical controller implementation. In the final part, simulation and experimental results verifying the *POM* scheme are presented.

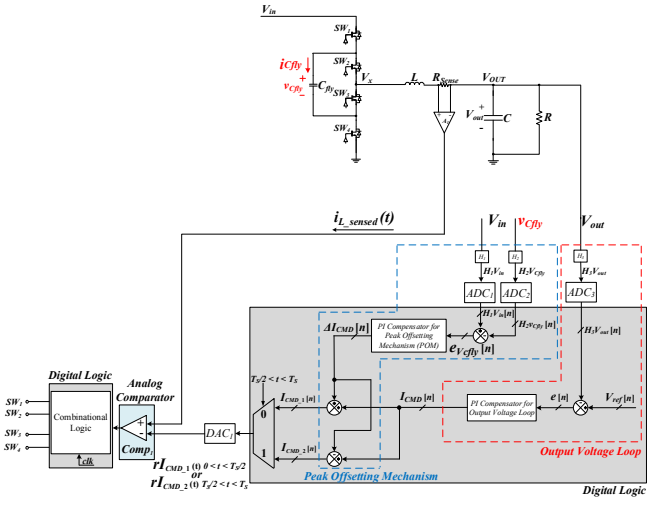

Fig. 1 A block diagram of a 3-level buck converter regulated by a mixed-signal peak CPM controller with *Peak Offsetting Mechanism*.

II. PEAK CPM STABILITY PROBLEMS AND PEAK OFFSETTING MECHANISM

Before presenting the *Peak Offsetting Mechanism* for stabilizing flying capacitor voltage (v_{Cfly} of Fig.1) at half of the input voltage ($V_{in}/2$) for peak CPM controlled three-level buck converter, the origin of the stability problem is reviewed.

A. Flying Capacitor Voltage Stability Problem in Peak CPM

The stability problem of the peak CPM for a 3-level flying capacitor buck converter (Fig. 1) is described by Figs. 2 and 3 showing the key converter waveforms over one switching period T_s, in steady state and during a flying capacitor voltage disturbance, respectively. When there is no disturbance in the system, as shown in Fig. 2, assuming the peak current command I_{CMD} generated by the outer voltage loop controller (Fig. 1) is constant, the flying capacitor voltage stays at the desired value of half V_{in} ($v_{Cfly} = V_{in}/2$). This yields equal inductor current slopes m_1 and m_3, where the expressions for the two slopes are shown within Fig. 2. In turn, these equal inductor current slopes imply equal flying capacitor current slopes for both of its charging and discharging phases. Furthermore, the duty ratios D_1 and D_2 for each half of the switching cycle are identical and can be expressed as

$$D_1 = \frac{(I_{CMD} - I_{0(Ts)})}{m_1 \cdot T_S}, \qquad (1)$$

$$D_2 = \frac{(I_{CMD} - I_{(Ts/2)})}{m_3 \cdot T_S}, \qquad (2)$$

where, $I_{(Ts/2)}$ can be expressed as Eq. (3) and ideally without perturbation equals to $I_{0(Ts)}$, i.e.,

$$I_{(Ts/2)} = I_{CMD} - m_2 \cdot (0.5 - D_1) \cdot T_S, \qquad (3)$$

if substituting Eq. (1) to Eq. (3), one can see that $I_{(Ts/2)}$ can also be expressed as a function of I_{CMD}, $I_{0(Ts)}$, m_1, m_2, and T_S

$$I_{(Ts/2)} = I_{CMD} - m_2 \cdot \left[\frac{T_S}{2} - \frac{(I_{CMD} - I_{0(Ts)})}{m_1}\right], \qquad (4)$$

As a result, the charge flowing in the flying capacitor during the first portion of a switching interval is equal to the charge flowing out during the second portion, represented by surface areas Q_A and Q_B, respectively, in Fig.2. These areas can be calculated as:

$$Q_A = \frac{(I_{CMD} + I_{0(Ts)})}{2} \cdot D_1 T_S, \qquad (5)$$

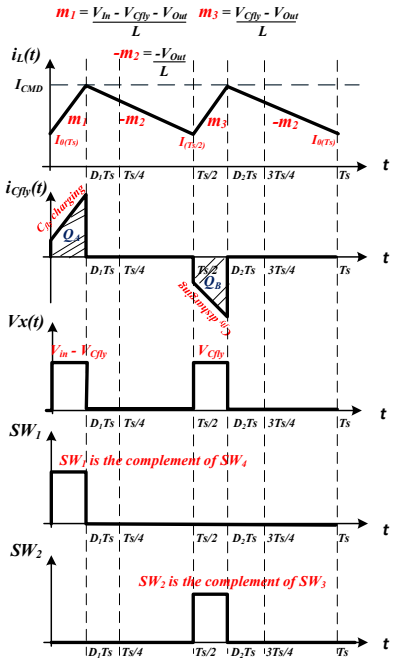

Fig. 2 Key steady-state waveforms of a 3-level buck converter with conversion ratio $D < 0.5$ (top to bottom): inductor current $i_L(t)$, flying capacitor current $i_{Cfly}(t)$, switching node voltage $v_x(t)$, and gating signal waveforms.

$$Q_B = \frac{-(I_{CMD} + I_{(Ts/2)})}{2} \cdot D_2 T_S, \qquad (6)$$

substitute Eq. (1) and (2) to Eq. (5) and (6) will further yield the expressions for Q_A and Q_B to be

$$Q_A = \frac{(I_{CMD}^2 - I_{0(Ts)}^2)}{2 \cdot m_1}, \qquad (7)$$

$$Q_B = \frac{-(I_{CMD}^2 - I_{(Ts/2)}^2)}{2 \cdot m_3}, \qquad (8)$$

and the net change of the capacitor charge ΔQ_{Cfly}, within T_s, i.e.,

$$\Delta Q_{Cfly} = \int_0^{Ts} i_{Cfly}(t)dt = Q_A + Q_B, \qquad (9)$$

is zero without disturbance, where $i_{Cfly}(t)$ is the flying capacitor current.

The result, $\Delta Q_{Cfly}=0$, from Eq. (9) implies that the total charge in the flying capacitor is constant, and therefore its voltage is constant and equal to $V_{in}/2$, the initial flying capacitor voltage at the beginning of a cycle in an ideal case. However, this does not constitute a stable equilibrium, which in the presence of a disturbance, will yield a runaway condition of $v_{Cfly}(t)$. Fig. 3 is a graphical representation of the case where the flying capacitor voltage, $v_{Cfly}(t)$ is perturbed from its nominal value of $V_{in}/2$ by quantity of $\Delta V_{Cfly}<0$ within one switching

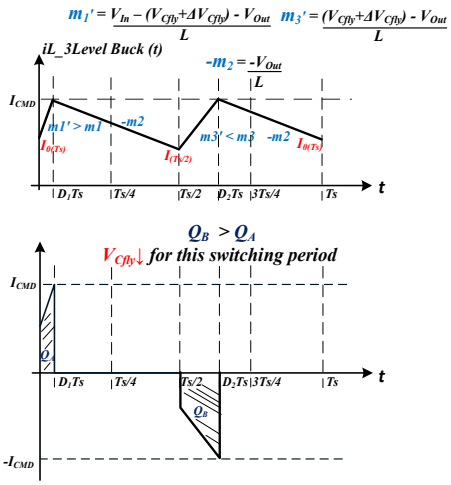

Fig. 3 Key current waveforms of the conventional peak CPM controller during flying capacitor disturbance within one switching period, T_S.

period T_S. As one can see, the initial perturbation, as introduced, causes the new charging and discharging slopes, m_1' and m_3' to deviate from their respective steady-state values, i.e.,

$$V_{Cfly} + \Delta V_{Cfly} < \frac{V_{in}}{2}, \qquad (10)$$

$$m'_1 = \frac{V_{in} - (V_{Cfly}+\Delta V_{Cfly}) - V_{out}}{L} > m_1, \text{ and} \quad (11)$$

$$m'_3 = \frac{(V_{Cfly} + \Delta V_{Cfly}) - V_{out}}{L} < m_3, \qquad (12)$$

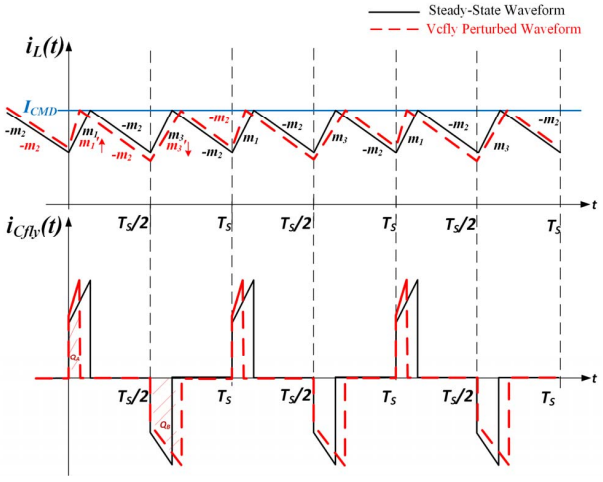

Fig. 4 Inductor and flying capacitor current waveforms over multiple switching cycles when a perturbation is introduced in $v_{Cfly}(t)$: solid line steady-state conditions; dashed line – waveforms of the current in the presence of flying capacitor voltage disturbance, i.e. for the case when $V_{Cfly} < V_{in}/2$.

This means for the same peak current command I_{CMD}, the larger charging phase slope m_1' (m_1' > m_1) will lead the inductor current to reach the peak command, I_{CMD}, faster compared to the condition in steady-state. Similarly, the smaller slope m_3' (m_3' < m_3) will delay the inductor current from reaching the peak command, I_{CMD}. Based on the previous considerations, m_1' and m_3' will in turn modify D_1, D_2 and $I_{(Ts/2)}$ from their pre-disturbance states and cause reduction of total charge of the flying capacitor, as described by Eq. (7), (8) and (9). This reduction of the total charge will ultimately further reduce the flying capacitor voltage. Fig. 4 shows the net charge loss and subsequent flying capacitor voltage loss from cycle to cycle will continue in the classical peak CPM scheme, which forces a fixed command for each peak within one switching cycle.

B. Peak Offsetting CPM Control

The peak CPM controller with *Peak Offsetting Mechanism* in steady-state, when the flying capacitor voltage is ideally equal to $V_{in}/2$, has no impact on the current loop operation. However, in the presence of a flying voltage disturbance, it modifies the controller operation by providing two different peak commands for the two inductor current peaks existing during one switching cycle of a three-level buck converter, as shown in Fig.5. The first peak, corresponding to the slope m_1 is set to a value $I_{CMD\_1} = I_{CMD} + \Delta I_{CMD}$, to a value larger than the steady state peak current command, and the second peak corresponding to the slope m_3 is set to smaller value, $I_{CMD\_2} = I_{CMD} - \Delta I_{CMD}$, where ΔI_{CMD} is a value set by a simple PI compensator comparing v_{Cfly} with $V_{in}/2$, i.e., with its desired value. As a result, the two peaks are offset symmetrically in opposite directions by a value of ΔI_{CMD} centered around I_{CMD}. The correction factor ΔI_{CMD} set by this additional control loop in steady-state is zero.

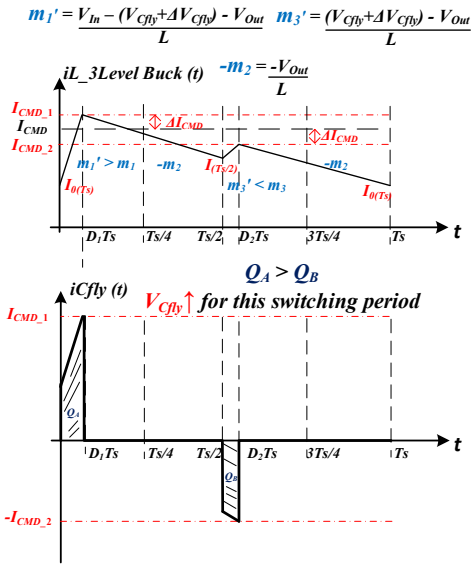

Fig. 5 Key current and control signal waveforms of the peak CPM controller with *Peak Offsetting Mechanism*.

Fig. 5, showing operation for a case when the initial value of the flying capacitor voltage is smaller than $V_{in}/2$, can be used to describe how setting the two peak commands offset symmetrically in opposite direction centered around I_{CMD} eliminates the runaway problem described in the previous subsection. By increasing the first peak and reducing the second one, Q_A and Q_B shown in Fig. 5 can now be expressed as

$$Q_A = \frac{[(I_{CMD} + \Delta I_{CMD})^2 - I_{0(Ts)}^2]}{2 \cdot m_1}, \qquad (13)$$

$$Q_B = \frac{-[(I_{CMD} - \Delta I_{CMD})^2 - I_{(Ts/2)}^2)]}{2 \cdot m_3}, \qquad (14)$$

the total capacitor charge can therefore be programmed to cause v_{Cfly} to ramp up to a higher value, and the problem of the runaway will be eliminated from cycle to cycle. Conversely, if v_{Cfly} is larger than $V_{in}/2$, ΔI_{CMD} will then be negative such that the first peak will be reduced, and the second peak increased; the total capacitor charge is therefore programmed to cause v_{Cfly} to ramp down to a lower value. Furthermore, burden on the output voltage loop generating I_{CMD} is reduced, due to the offset peak current commands averaging to the desired I_{CMD} itself over a complete switching cycle.

III. Practical Implementation

As it can be seen from Fig. 1, the conventional mixed-signal peak CPM controller [12] is modified. As in the conventional implementation the output voltage loop is digital, and, in this case, the analog current loop is modified, by adding a mixed-signal control loop (*Peak Offsetting Mechanism* loop) and providing two separate outputs for controlling the two current peaks within a switching period separately. As described before, the new loop compares the flying capacitor voltage, v_{Cfly}, to $V_{in}/2$ and, based on the digital error signal $e_{vcfly}[n]$, the digital *Peak Offsetting Mechanism PI compensator* produces a digital correcting current reference $\Delta I_{CMD}[n]$. This value is both added and subtracted from the steady-state peak current reference, $I_{CMD}[n]$, which is a command from the output voltage loop, to generate the two-separate current peak references, $I_{CMD\_1}[n]$ and $I_{CMD\_2}[n]$ for the first and second half of the switching cycle, respectively. The two digital peak commands are then converted into analog signals separately, depending on if the operation is during the first or second half of the switching cycle. In other words, during the first half of the switching period, $0 < t < T_S/2$, $I_{CMD\_1}[n]$ is converted into analog voltage signal equivalent, $rI_{CMD\_1}(t)$, through DAC_1, where r is the gain of current sensing circuit, whereas in the second half of the

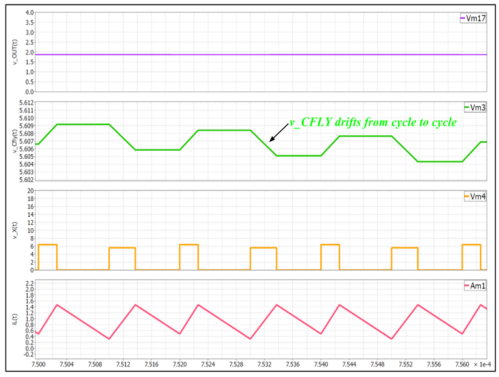

Fig. 6 Zoomed in view of V_{Cfly} perturbation in conventional peak CPM under the simulation condition of L = 1.2µH, C = 80µF, C_{Fly} = 75µF, f_{sw} = 500 kHz, $V_{in\ (nominal)}$ = 12 V, $V_{Cfly\ (nominal)}$ =6 V, V_{out} = 1.8 V, D = 0.15. Waveforms (top to bottom): output voltage $v_{Out}(t)$, flying capacitor voltage $v_{Cfly}(t)$, switching node voltage $v_x(t)$, and inductor current $i_L(t)$.

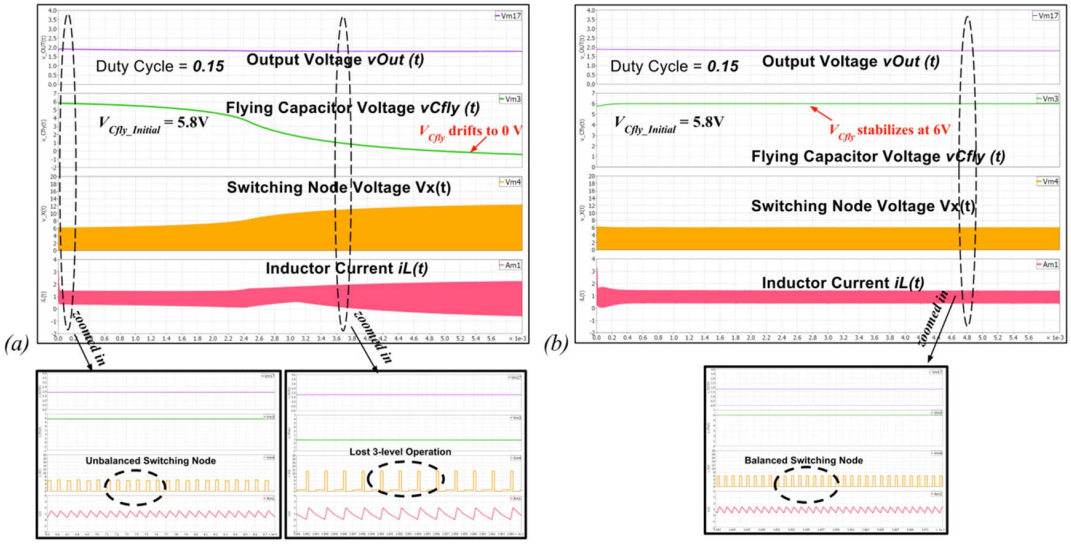

Fig. 7 Simulation Comparison between Peak CPM *(a)* without and *(b)* with *Peak Offsetting Mechanism* for V_{Cfly} stabilization under the simulation condition of L = 1.2µH, C = 80µF, C_{Fly} = 75µF, f_{sw} = 500 kHz, $V_{in\ (nominal)}$ = 12 V, $V_{Cfly\ (nominal)}$ =6 V, V_{out} = 1.8 V, D = 0.15. Waveforms in both *(a)* and *(b)* (top to bottom): output voltage $v_{Out}(t)$, flying capacitor voltage $v_{Cfly}(t)$, switching node voltage $v_x(t)$, and inductor current $i_L(t)$.

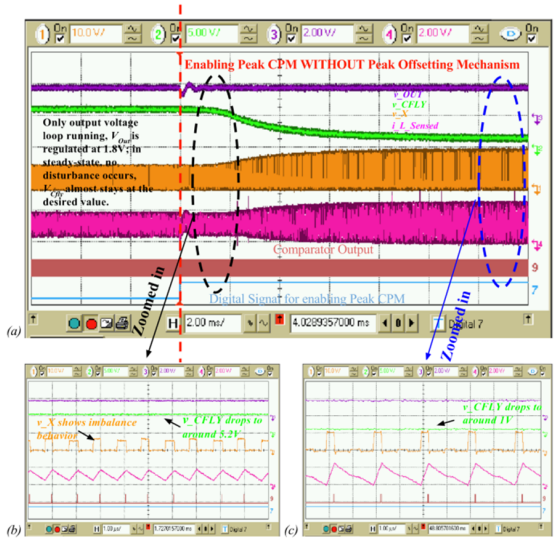

Fig. 8 V_{Cfly} runaway condition in conventional Peak CPM on a three-level buck converter for L = 1.2µH, C = 80µF, C_{Fly} = 75µF, f_{sw} = 500 kHz, $V_{in\ (nominal)}$ = 12 V, $V_{Cfly\ (nominal)}$ =6 V, V_{out} = 1.8 V, D = 0.15. (a)View of V_{Cfly} drifting in conventional Peak CPM. Time scale: 2 [ms]/div; at trigger point which is three horizontal divisions from the left, conventional Peak CPM is enabled. (b) shows zoomed-in view right after trigger point and (c) shows zoomed-in view of steady-state after trigger point; both (b) and (c) have time scale: 1[µs]/div; Ch1. 10[V]/div: V_x; Ch2. 5[V]/div: V_{Cfly}; Ch3. 2[V]/div: V_{out}; Ch4. 2[V]/div: i_{L_Sensed}.

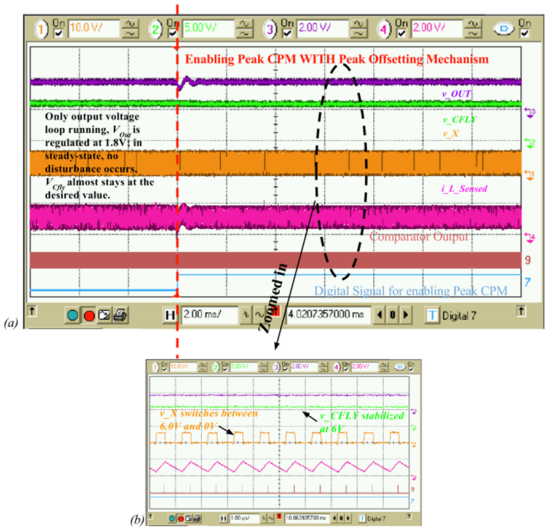

Fig. 9 Effect of *Peak Offsetting Mechanism* for V_{Cfly} runaway condition on a three-level buck converter for L = 1.2µH, C = 80µF, C_{Fly} = 75µF, f_{sw} = 500 kHz, $V_{in\ (nominal)}$ = 12 V, $V_{Cfly\ (nominal)}$ =6 V, V_{out} = 1.8 V, D = 0.15. (a)View of V_{Cfly} stabilized in Peak CPM with *Peak Offsetting Mechanism*. Time scale: 2 [ms]/div; at trigger point which is three horizontal divisions from the left, Peak CPM with *Peak Offsetting Mechanism* is enabled. (b) shows zoomed-in view of steady-state after trigger point; (b) has time scale: 1[µs]/div; Ch1. 10[V]/div: V_x; Ch2. 5[V]/div: V_{Cfly}; Ch3. 2[V]/div: V_{out}; Ch4. 2[V]/div: i_{L_Sensed}.

switching period, $T_S/2 < t < T_S$, $I_{CMD\_2}[n]$ will be converted into analog voltage signal, $rI_{CMD\_2}(t)$, also through DAC_1. The values $rI_{CMD\_1}(t)$ and $rI_{CMD\_2}(t)$ are compared with the sensed inductor current through the analog comparator, $Comp_1$, during the first and second half of the switching cycle, respectively. The comparator output is transferred back into digital domain, eventually generating the gating signals for the three-level buck converter.

IV. Simulaiton and Experimental Results

To verify operation of the introduced *Peak Offsetting Mechanism* based peak CPM controller both a simulation test bed and an experimental prototype were developed. The prototype converter is a 12 V to 1.8 V/ 1A 3-level FC buck.

Using PLECS simulation tool, the previous analytical derivation from Section II.A and the stability problem are verified, through demonstration of a cycle by cycle basis operation of conventional peak CPM. As shown in Fig. 6, there is a constant voltage drop of flying capacitor voltage, which translates in a continuous drift of v_{Cfly} from cycle to cycle once a perturbation occurs in the system.

Also, using PLECS, verification of the functionality of the introduced peak CPM with *Peak Offsetting* controller is performed, through a comparison with the operation of the conventional peak CPM controller. In Fig. 7, the operation of the new controller is demonstrated for the same runaway condition of v_{Cfly}.

By comparing Figs. 6 and 7, it can be seen that, the conventional peak CPM control scheme results in a drifting of v_{Cfly} while the *Peak Offsetting Mechanism*, not only prevents the drift but also forces the flying capacitor voltage to settle at the desired value of $V_{in}/2$. Since v_{Cfly} is stabilized at $V_{in}/2$, the 3-level mode of operation is maintained as observed in the inductor current waveform with benefits of frequency multiplication and reduced switch voltage stress [5].

Experimental system was built based on the diagram from Fig. 1. The digital part of the controllers was implemented using an FPGA development board, a custom-made board having the power stage, discrete current sensor, comparators, buffers, and digital-to-analog converters, and an interconnecting board having analog-to-digital converters. Due to the limitations of the discrete current sensing circuit the effective frequency of the converter, i.e. frequency of the current ripple, was set to be 1 MHz while the switches are operated at a frequency of 500

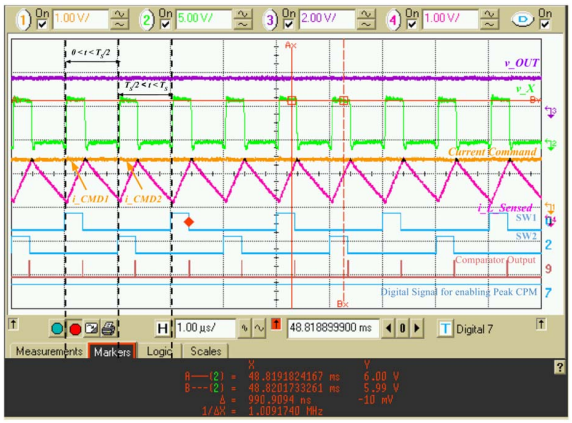

Fig. 10 Steady-state operation in peak CPM with *Peak Offsetting Mechanism* with stabilized $V_{Cfly\ and}$ V_{out} on a three-level buck converter for L = 1.2µH, C = 80µF, C_{Fly} = 75µF, f_{sw} = 500 kHz, $V_{in\ (nominal)}$ = 12 V, $V_{Cfly\ (nominal)}$ =6 V, V_{out} = 1.8 V, D = 0.15. Time scale: 1 [µs]/div; Ch1. 1[V]/div: *Current Command* ($I_{CMD\_1}(0<t<T_s/2)$ and $I_{CMD\_2}(T_s/2<t<T_s)$); Ch2. 5[V]/div: V_x; Ch3. 2[V]/div: V_{out}; Ch4. 1[V]/div: i_{L_Sensed}.

kHz. It should be noted that, as shown in [12], on-chip implementation of a low-power high-frequency (10 MHz) current sensor is possible. The experimental results of the conventional peak CPM controller in the presence of a flying capacitor voltage disturbance are shown in Fig. 8, and the results with peak offsetting controller are shown in Fig. 9.
Fig. 10 demonstrates a steady-state operation using peak CPM with *Peak Offsetting Mechanism* with peak command as well as gating signals showing. Experimental and simulation results are in complete agreement. Conventional peak CPM controller is not capable of recovering from a flying capacitor voltage perturbation, whereas in the case of a peak CPM with *Peak Offsetting Mechanism* control scheme, the flying capacitor voltage disturbance is eliminated, and v_{Cfly} is stabilized at the desired value of $V_{in}/2$.

V. Conclusions

This paper introduces a practical mixed-signal control method that enables use of peak current programmed mode (CPM) control in low-power dc-dc multi-level flying capacitor converters (ML-FC). The origin of the flying capacitor runaway problem is reviewed, and a method based on asymmetrical offsetting of the two current peaks within one switching period is introduced as a solution. The effectiveness of *Peak Offsetting Mechanism (POM)* is demonstrated with a 3-level FC buck converter prototype displaying stable operation of the flying capacitor voltage and at the same time implementing the desired peak CPM control strategy.

References

[1] T.A. Meynard, H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," *in Proc. IEEE PESC* '92, vol. 1. pp.397-403 July 1992.

[2] T.A Meynard, H. Foch, "Multilevel converters and derived topologies for high power conversion," *in Proc. 1995 IEEE 21st Int. Conf. Industrial Electronics, Control, and Instrumentation,* pp. 21–26. Nov. 1995.

[3] T.A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob and M. Nahrstaedt, "Multicell converters: basic concepts and industry applications," *IEEE Trans on Industrial Electron*., vol.49, no.5, pp. 955- 964, Oct 2002.

[4] Y. Lei and R. Pilawa-Podgurski, "An analytical method to evaluate flying capacitor multilevel converters and hybrid switched-capacitor converters for large conversion ratios," in *Control and Modeling for Power Electronics (COMPEL), 2015 IEEE 16th Workshop on*, pp. 1–7,July 2015

[5] N. Vukadinović, A. Prodić, B. A. Miwa, C. B. Arnold, M. W. Baker., "Volume and Efficiency Comparison Between Multi-level Dc-Dc Converters and Buck Converter for Low-Power Mobile Applications" *18th International Symposium on Power Electronics Ee 2015*, Novi Sad, Serbia, October 2015

[6] Meynard, T.A.; Fadel, M.; Aouda, N., "Modeling of multilevel converters," *Industrial Electronics, IEEE Transactions on*, vol.44, no.3, pp.356, 364, Jun 1997.

[7] Nenad Vukadinovic, Aleksandar Prodic, Brett A. Miwa, Cory B. Arnold, Michael W. Baker, "Discontinuous conduction mode of multi-level flying capacitor DC-DC converters and light-load digital controller", *Control and Modeling for Power Electronics (COMPEL) 2017 IEEE 18th Workshop on*, pp. 1-7, 2017.

[8] N. Vukadinovic, A. Prodic, B. A. Miwa, C. B. Arnold, and M. W. Baker. "Extended Wide-Load Range Model for Multi-Level DC-DC Converters and a Practical Dual-Mode Digital Controller". In *Proc. 31st Applied Power Electronics Conference and Exposition (APEC 2016)*, March 2016.

[9] D. Reusch, F. C. Lee and M. Xu, "Three Level Buck Converter with Control and Soft Startup," in *2009 IEEE Energy Conversion Congress and Exposition*, San Jose, CA, 2009.

[10] J. S. Rentmeister, C. Schaef, B. X. Foo, and J. T. Stauth, "A flying capacitor multilevel converter with sampled valley-current detection for multi-mode operation and capacitor voltage balancing," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–8, 2016.

[11] Jan S. Rentmeister, Jason T. Stauth, "A 48V:2V flying capacitor multilevel converter using current-limit control for flying capacitor balance", *Applied Power Electronics Conference and Exposition (APEC) 2017 IEEE*, *pp. 367-372, 2017, ISSN 2470-6647.*

[12] A. Parayandeh, B. Mahdavikkhah, S. M. Ahsanuzzaman, A. Radic, and A. Prodic, "A 10 MHz mixed-signal CPM controlled DC-DC converter IC with novel gate swing circuit and instantaneous efficiency optimization," *in Proc. IEEE Energy Conversion Congress and Exposition (ECCE), pp.1229,1235, 17-22 Sept. 2011*.