A Single-Stage 6.78 MHz Transmitter with the Improved Light Load Efficiency for Wireless Power Transfer Applications

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***Abstract*— A single-stage transmitter is reviewed, which directly converts a utility ac input to high frequency (6.78 MHz) ac output for wireless power transmission. By integrating two stages (totem-pole PFC rectifier and full bridge inverter) into a single stage, the topology achieves high efficiency and reduced component count. In this paper, a simple auxiliary circuit is added to allow the single-stage transmitter to operate in two modes. At heavy load, the transmitter operates as a totem-pole rectifier with PFC and achieves low distortion of the input current. At light load, the circuit operates as a voltage-doubler rectifier (VDR), extending the ZVS range of the transmitter. As a result, hard switching is avoided and efficiency is improved at light load. This improved single-stage transmitter is verified by a 100 W, GaN-based laboratory prototype.**

Keywords—WPT; single-stage transmitter; 6.78MHz;

I. INTRODUCTION

Wireless power transfer (WPT) attracts great attention in industrial and consumer applications due to high flexibility. However, current offerings are limited by low efficiency [1], [2]. To improve power efficiency, different approaches have been proposed to optimize transmitter, receiver and coils design. For transmitter design, reducing the number of cascaded conversion stages between the ac line and the transmitter coil is one approach with potential to increase overall efficiency.

Several single-stage transmitters have been proposed in the previous literature. The 6.78 MHz single-stage transmitter in [2] is not applicable for the system in which output power is larger than 75 W, where Power Factor Correction (PFC) is required according to IEC 61000-3-2 [3]. In [4] and [5], a single-stage transmitter with PFC is proposed, however, it is only suitable for low frequency (such as 20 kHz) WPT systems due to hard switching. The single-stage 6.78 MHz transmitter proposed in [6] converters line-frequency ac to 6.78 MHz ac output. By integrating totem-pole rectifier and high-frequency full bridge inverter, it achieves 92% power efficiency at full power, 15% THD of input current, and 0.99 power factor at 100 W output. However, losing ZVs operation at light load leads to the dramatic deterioration of power efficiency. In this paper, efforts are made to improve the performance and the efficiency at light load of the single-stage 6.78 MHz transmitter presented in [6].

The simplified schematic of the single-stage transmitter in [6] is illustrated in Fig. 1(a). L_b, D_1, D_2, S_1 and S_2, comprise a totem-pole PFC rectifier. S_1~S_4 form a full bridge inverter which generates a 6.78 MHz ac output. Zero voltage switching (ZVS) is achieved on switches S_1/S_2 and S_3/S_4 with assistance from resonant tank A (L_{auxA}, C_1, C_2), and tank B (L_{auxB}, C_3, C_4), respectively. Z_{load} represents the equivalent load at the output of inverter, including matching network, coils and the reflected load from the receiver side. According to the experimental results in [6], high power efficiency is achieved at heavy load.

The power efficiency of this single-stage converter drops dramatically at light load due to hard switching. As shown in Fig. 1, phase leg A (S_1 and S_2) provides functionality for both the rectifier and inverter. Phase leg A and B switch at constant 6.78 MHz to ensure low-harmonic sinusoidal 6.78 MHz ac current is delivered to the load. To obtain the desired bus voltage with fixed switching frequency (6.78 MHz), the PFC rectifier works in discontinuous conduction mode (DCM). Under this circumstance, to maintain a constant dc bus voltage at different loads, the duty cycle of phase leg A needs to decrease in accordance with the reduced load, as in a traditional boost rectifier. This reduced duty cycle causes hard switching at light load. Fig. 2(a) shows the gate signal of phase leg A (G_{S1} and G_{S2}) and ZVS tank current (I_{auxA}) at heavy load; Fig. 2(b) shows the same signals at light load. At light load, the reduced duty cycle leads to a corresponding decrease in the peak value of I_{auxA},

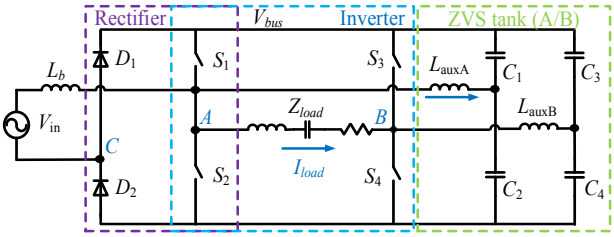


Fig. 1. Single-stage transmitter [6]

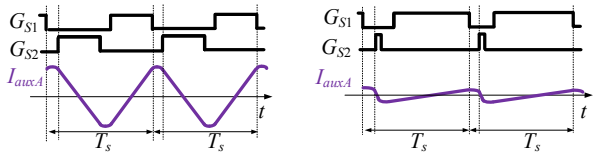


Fig. 2. ZVS tank current at heavy load (a) and light load (b)

eventually resulting in hard switching of S_1 and S_2. Once hard switching occurs, due to the high switching frequency and high bus voltage, power loss increase dramatically.

An auxiliary circuit is incorporated into the original single-stage transmitter to solve hard switching issue and therefore improve the power efficiency at light load. With this auxiliary circuit, two operation modes are configured. At heavy load, totem-pole PFC rectifier operates to ensure high PF and low THD. When the load decreases to the point that ZVS is no longer guaranteed, and below the power level where PFC is required, the circuit operates as a VDR [8-10]. Three benefits are achieved by this solution. First, when totem-pole operation is replaced by VDR at light load, hard switching is eliminated because S_1 and S_2 remain fully off. Second, once S_1 and S_2 stop switching, the ZVS tank current I_{auxA} drops to zero. That is, the power losses in phase leg A and ZVS tank A are eliminated. Third, the bus voltage under VDR operation is the same as it in totem-pole PFC rectifier. This feature facilitates a smooth transition between the two operating modes.

The improved single-stage 6.78 MHz transmitter with high efficiency across a full load range is described in Section II; the practical design consideration is detailed in Section III; experimental results are presented in Section IV; Section V concludes this paper.

II. Topology Description and Operation Principles

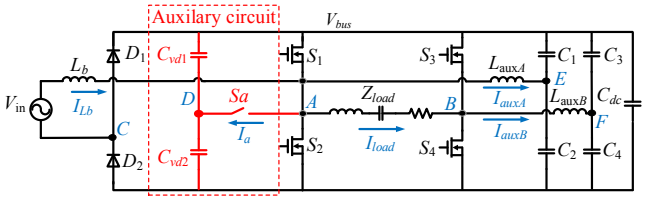


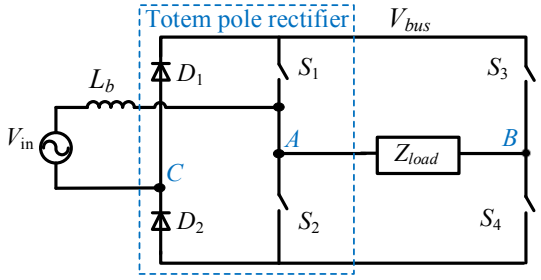
Fig. 3. The improved single-stage transmitter

Fig. 3 illustrates the improved single-stage transmitter. Based on the original one, an auxiliary circuit, including a bi-directional switch S_a and two capacitors C_{vd1} and C_{vd2}, is added. Two operation modes, heavy load mode and light load mode, are configured. The simplified equivalent circuits of each mode are given in Fig. 4(a) and Fig. 4(b), respectively.

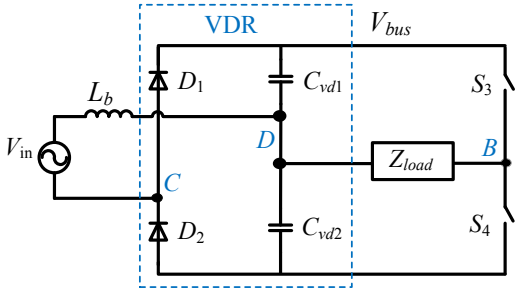
At heavy load mode where ZVS in phase leg A is assured by a large duty cycle, the ac input voltage is converted to dc voltage by totem-pole PFC rectifier. Meanwhile, high PF and low THD of input current are guaranteed in this mode. The full bridge formed by S_1~S_4 regulates 6.78 MHz ac output to drive the transmitter coil. This mode is achieved by turning off S_a. The detailed operation, analysis, and control algorithm of this mode are given in [6]. The voltage ratio is designed as m=V_{bus}/V_m=2, where V_{bus} is the bus voltage and V_m is the peak value of ac input voltage.

Light load mode is entered by turning on S_a and turning off S_1 and S_2. Under this circumstance, a VDR is formed and used to process ac line voltage to dc bus voltage. As long as this mode occurs only at power less than 75 W, PFC is not required. The rectifier output V_{bus} will be nearly twice V_{in_pk}. As a result, V_{bus} remains constant in both operating modes with smooth transition between each. C_{vd1}, C_{vd2}, S_3 and S_4 comprise a half bridge inverter to provide the 6.78 MHz ac output in this mode.

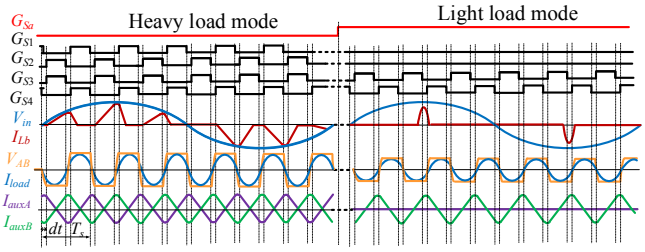
Fig. 4(c) gives the main waveforms of each operating mode. The detailed operation of heavy load mode and ZVS tank design have been detailed in [6], thus, this paper mainly focuses on the operation, analysis, design, and verification of the light load mode, as well as the transition between modes.



(a) The simplified circuit at heavy load mode



(b) The simplified circuit at light load mode



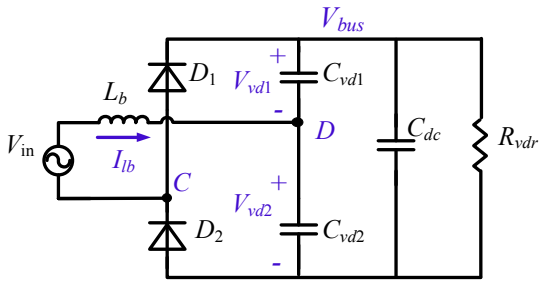
(c) The main waveforms in the two-operation modes

Fig. 4. Two-operation modes of single-stage transmitter

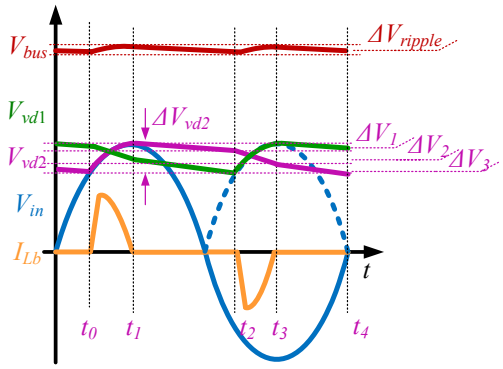
III. Considerations In Practical Design

A. The Impact of Practical Design on the Bus Voltage

In practice, the average bus voltage in VDR operation depends on load, C_{vd1}, C_{vd2} and C_{dc}. The schematic and waveforms of the VDR are illustrated in Fig. 5. The load of the VDR is modeled as a resistive load R_{vdr}. Without loss of generality, it is assumed that C_{vd1} = C_{vd2} = C_{vd}.



(a)



(b)

Fig. 5. Operational waveforms of VDR

The operation of the VDR is classified into four modes. The input voltage V_{in} is

$$V_{in} = V_m \cdot \sin(\omega t) \tag{1}$$

where $\omega=2\pi \cdot f_{line}$. f_{line} is the line frequency of input voltage, 60 Hz in this work.

Mode 1 ($t_0 \le t \le t_1$): during this time, D_2 is forward biased and conducts current I_{Lb}. The voltage on C_{vd2} is changed by

$$\Delta V_{vd2} = V_m \cdot (1 - \sin(\omega t_0)) \tag{2}$$

Mode 2 ($t_1 \le t \le t_2$): when V_{vd2} reaches V_m, D_2 becomes reverse biased, C_{vd2} is discharged through C_{vd1}, C_{dc} and R_{vdr}. The decreased voltage is ΔV_1.

$$\Delta V_1 = V_m \cdot (1 - \exp(\frac{-(t_2 - t_1)}{R_{load} \cdot (0.5C_{vd} + C_{dc})})) \tag{3}$$

Mode 3 ($t_2 \le t \le t_3$): during this period, the voltage on C_{vd1} is changed by ΔV_{vd1} through C_{vd2} and C_{dc}. Since $C_{vd1} = C_{vd2}$, ΔV_{vd1} is equal to ΔV_{vd2} in (2). So, the voltage change on C_{vd2} during this time is ΔV_2.

$$\Delta V_2 = \Delta V_{vd1} \cdot \frac{C_{dc}}{C_{vd} + C_{dc}} = \Delta V_{vd2} \cdot \frac{C_{dc}}{C_{vd} + C_{dc}} \tag{4}$$

Mode 4 ($t_3 \le t \le t_4$): ΔV_3 is the voltage change of C_{vd2} during this time

$$\Delta V_3 = \Delta V_1 \tag{5}$$

According to

$$\Delta V_{vd2} = \Delta V_1 + \Delta V_2 + \Delta V_3 \tag{6}$$

And

$$\frac{T_{line}}{2} = t_2 - t_0 \tag{7}$$

ΔV_1, ΔV_2, ΔV_3 and ΔV_{vd2} are obtained by solving equations (2) ~ (7). The average bus voltage is

$$V_{bus} = 2 \cdot (V_m - 0.5\Delta V_{vd2}) \tag{8}$$

According to this derivation, the value of the average voltage V_{bus} depends on R_{vdr}, C_{vd1}, C_{vd2} and C_{dc}.

To suppress double line frequency voltage ripple on the dc bus, the required energy storage ΔE at full power (100 W) is

$$\Delta E = \int_{\frac{T_{line}}{4}}^{\frac{3T_{line}}{4}} (P_{ave} - P_{ac}(t))dt = \frac{P_{ave}}{\omega} = 265\ mJ \tag{9}$$

As an example, if allowed maximum ripple voltage at full power is 5 V and V_{bus}=340 V, the required capacitance across the dc bus is

$$C_{eng} = \frac{\Delta E}{V_{bus} \cdot \Delta V_{bus}} = 0.5C_{vd} + C_{dc} = 155\ uF \tag{10}$$

By combining equations (8) and (10), the relation between V_{bus} and $k_c=C_{dc}/C_{vd}$ is solved and plotted in Fig. 6. Smaller k_c results in the average bus voltage V_{bus} closer to the ideal value $2V_m$ = 340 V. In terms of performance, small k_c is preferred.

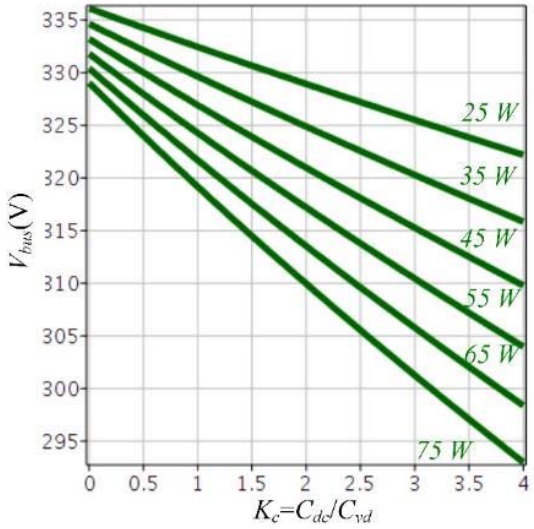


Fig. 6. Average bus voltage V_{bus} vs C_{dc}/C_{vd}.

B. The Selection of S_a

In practice, two identical back-to-back MOSFETs (M_{a1} and M_{a2}) implement the bi-directional switch S_a, as shown in Fig. 7. C_{ma} is the junction capacitors of M_{a1}/M_{a2} while C_q is the junction capacitance of S_1/S_2. When M_{a1} and M_{a2} are off (at heavy load mode), two C_{ma} are connected in series to switching node A. To perform ZVS in phase leg A, the total capacitance that needs to be fully charged/discharged now becomes C_{tot} =2 C_q +0.5 C_{ma}, where $C_{ma} \ll 4 \cdot C_{vd}$. The additional capacitance coming from the auxiliary circuit requires higher ZVS tank current for soft switching. Consequently, higher conduction loss is incurred. To limit this impact, MOSEFTs with small junction capacitance are preferred for M_{a1} and M_{a2}.

In addition, the current flowing through M_{a1} and M_{a2} (I_a), should remain within the maximum current of devices. I_a is the sum of input current I_{Lb} and the load current I_{load}. In this system, the maximum power is 100 W, and bus voltage is 340 V, so, I_{load} is quite small. Devices M_{a1} and M_{a2} only conduct current at light load, I_{load} is negligible under this condition. Therefore, I_a is approximated to I_{Lb}. At heavy load, $I_a \approx 0$. At light load, when M_{a1} and M_{a2} are turned on, there are two situations. When the diode is reverse biased ($t \le t_0$, $t_1 \le t \le t_2$ and $t_3 \le t \le t_4$), I_a=0. When the diode forward biased ($t_0 \le t \le t_1$ and $t_2 \le t \le t_3$), I_a is

$$I_a = \frac{V_{in}}{Z_c} \tag{11}$$

where Z_c is the output impedance of V_{in}.

$$Z_c = \frac{(Z_{vd} + Z_o)Z_{vd}}{2Z_{vd} + Z_o} \tag{12}$$

where Z_{vd}=1/$j\omega C_{vd}$, and

$$Z_o = \frac{R}{1 + j\omega C_{dc} R} \tag{13}$$

Considering the output capacitance and current capability of M_{a1} and M_{a2}, MOSFET IPD50R3K0CE is chosen in this application. The calculated energy-based equivalent junction capacitance is C_{ma} = 11 pF. Only a negligible 5.5 pF of capacitance is added to switching node A.

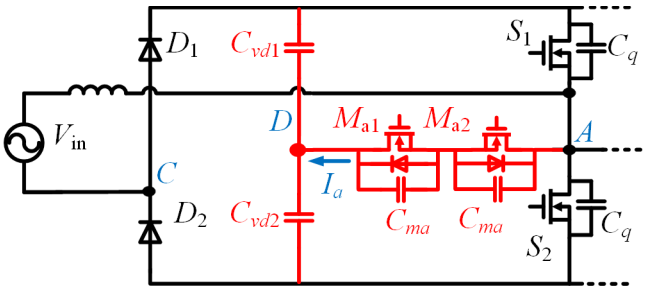


Fig. 7. Practical auxiliary circuit

IV. Experimental Verification

A GaN-based prototype has been built to verify this improved single-stage transmitter. The design parameters of this prototype are summarized in Table I. The prototype picture is shown in Fig. 8.

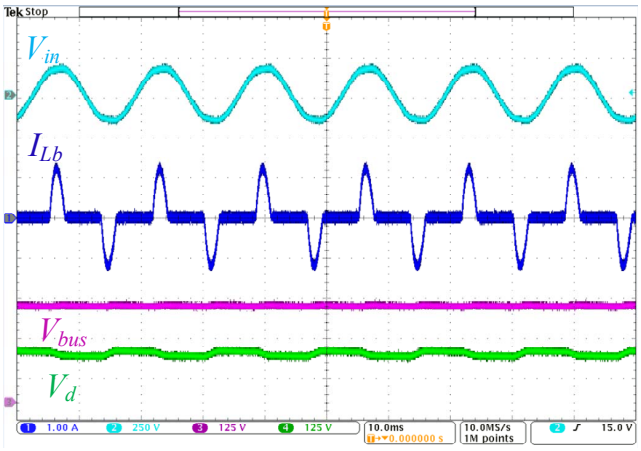
TABLE I
DESIGN PARAMETERS OF THE PROTOTYPE

Parameter	Symbol	Value
Input voltage	V_{in}	120 V/60 Hz
Bus voltage	V_{bus}	340 V
Output power	P_o	100 W
Switching frequency	f_s	6.78 MHz
Capacitors in VDR	C_{vd1}/ C_{vd2}	70 µF
dc capacitors	C_{dc}	120 µF
Input inductor	L_b	4.5 µH
Power switches	S_1–S_4	GaN FETs
Diodes	D_1–D_2	SiC Diodes
Auxiliary switches	M_{a1}/ M_{a2}	IPD50R1K4CE

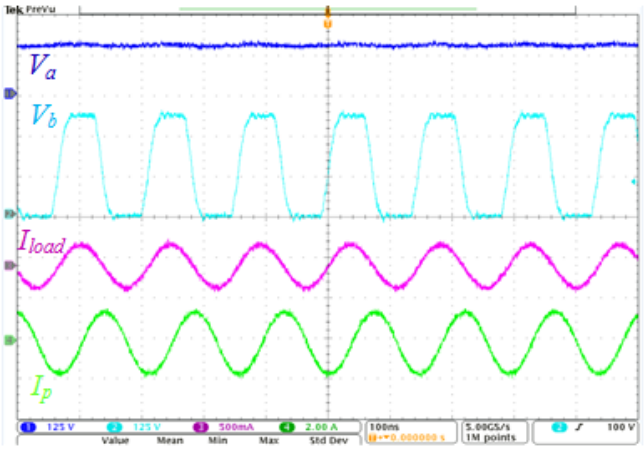
Fig. 8. Prototype picture

The experimental waveforms in light load mode (V_{in}=120 V rms/60 Hz, Po=50 W, f_s=6.78 MHz) are illustrated in Fig. 9. Fig. 9(a) shows the waveforms of the input voltage (V_{in}), inductor current (I_{Lb}), bus voltage (V_{bus}), the voltage on C_{vd2} (V_d). I_{in} and I_{Lb} have the same waveform under this operation mode. The waveform of V_d shows the expected line frequency ripple while V_{bus} has a small double line frequency ripple. The measured V_{bus}=307 V, which matches with the estimated value shown in Fig. 6. Fig. 9(b) illustrates the switching node voltage of phase leg A and B (V_a and V_b, respectively), and inverter output current (I_{load}). V_a is half of V_{bus}. The turn on and turn off transition at V_b shows resonant waveshape which validates the ZVS operation.

A filter network is placed at the output of the transmitter to suppress harmonic current and accomplish impedance matching. Since this paper mainly focuses on the operation and design of the improved transmitter, this network which has been detailed in [7], will not be discussed here. The output current of network I_p is used to directly drive transmitter coil. From the waveform in Fig. 9(b), I_p exhibits low harmonic content.

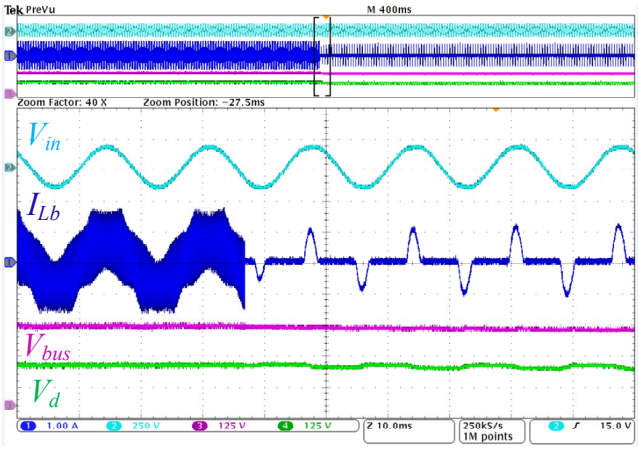


(a)



(b)

Fig. 9. Waveforms at light load mode (P_o=50 W).



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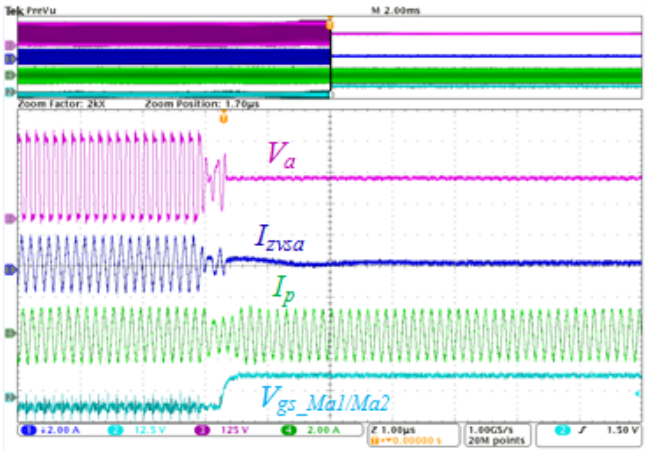
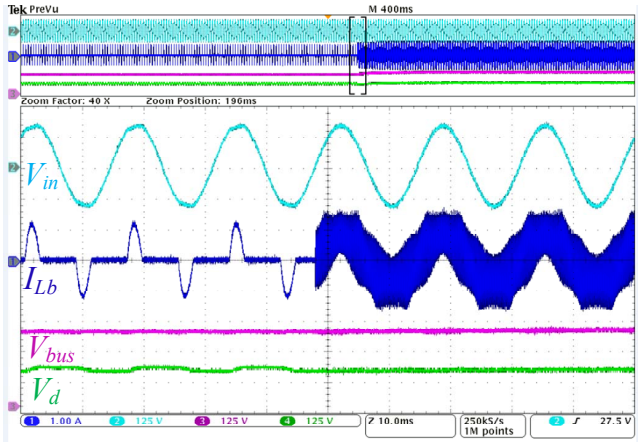


(b)

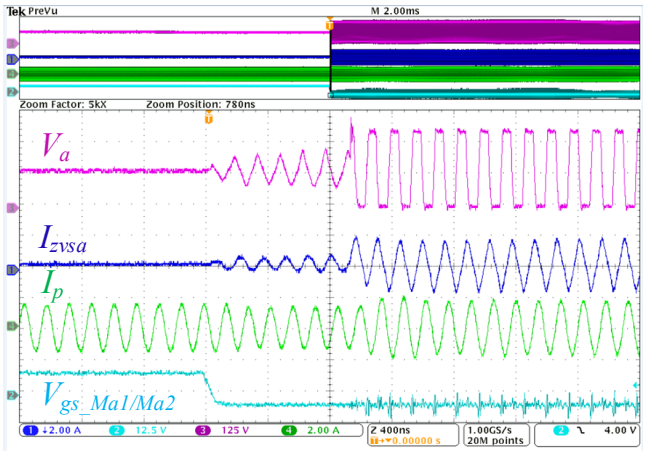
Fig. 10. The transition from heavy load to light load mode.

Fig. 10 shows the waveforms during the transition from heavy load mode to light load mode. The transition starts with turning off S_1 and S_2. To smooth the transition, S_1 and S_2 are turned off during their dead time, then M_{a1} and M_{a2} are turned on after hundreds of nanoseconds. From Fig. 10(a), the rectifier performs a smooth transition. According to Fig 10(b), a few switching cycles of resonant behavior occur on switching node A after turning off S_1 and S_2 and before M_{a1} and M_{a2} on. This is caused by the load current charging/discharging the output capacitors of S_1 and S_2. This phenomenon is expected and will not impact operation. I_p has negligible disturbance during this transition.

Fig. 11 shows the transition from light load mode to heavy load mode. This transition begins with turning off M_{a1} and M_{a2}. To avoid cross-conduction between M_{a1}, M_{a2} and S_1/ S_2, a delay of hundreds of nanoseconds is implemented before turning on S_1/ S_2. From Fig. 11(a), the rectifier achieves a smooth transition. In Fig. 11(b), the expected resonant behavior due to charging/discharging output capacitors of S_1 and S_2 is present during the delay time. Since ZVS tank A has nearly zero current, there is at least one hard switching event in the first turn-on of the either S_1 or S_2. To reduce the chance of hard switching, two methods are adopted. (1) Since I_{load} periodically charges/discharge output capacitors of S_1 and S_2 in every switching period. It is better to turn on S_1 when V_a resonates to the positive peak value or turn on S_2 when V_a reaches the smallest value. (2) The first turning on pulse for S_1/ S_2 is set to be half of the normal on time. Thus, the ZVS tank current will reach the steady-state after the first PWM pulse. These two methods are verified by the waveform in Fig. 11(b). S_1 is turned on with small voltage stress. S_1 and S_2 achieve soft switching starting with the second switching period. I_p has negligible disturbance during this transition.



(a)



(b)

Fig. 11. The transition from light load to heavy load mode.

Fig. 12 gives the measured and calculated power loss. The blue curve represents the estimated power loss under heavy load mode while the green curve indicates light load mode. The blue squares show the measured power loss under heavy load and green circles demonstrate the results from light load mode. As seen, experimental power loss under heavy load mode matches well with mathematical expectation. For light load mode operation, there is a small discrepancy between measured loss and estimation. To get the maximum power efficiency, the single-stage transmitter should operate at heavy load mode when $P_o > 50$ W, and work at light load mode when $P_o < 50$ W. Fig. 13 shows the power efficiency curve of this proposed single-stage transmitter. High power efficiency is obtained across the full load range.

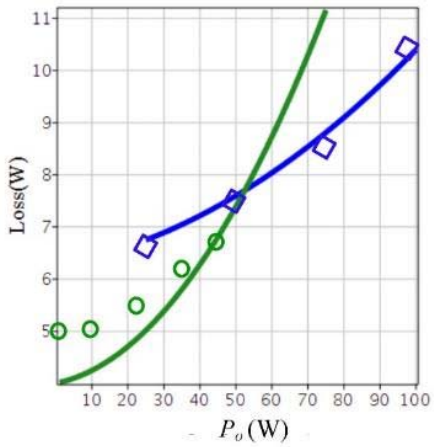


Fig. 12. Measurement power loss

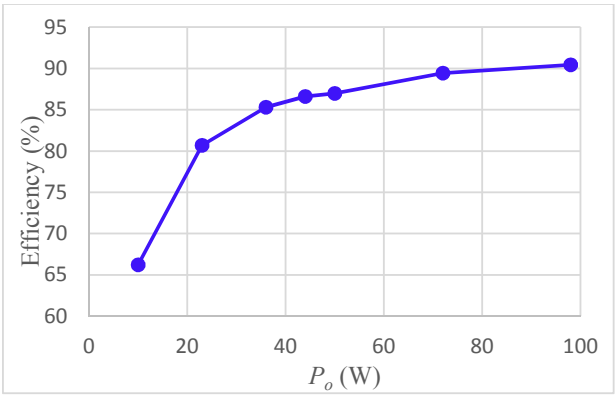


Fig. 13. Measurement power efficiency curve

V. Conclusion

This paper proposes a solution to improve the power efficiency of the single-stage transmitter at light load. By adding an auxiliary circuit, the single-stage transmitter is designed to operate under two configurations according to the different load condition. The operation principle, theoretical analysis and design consideration of this improved single-stage transmitter have been discussed in this paper. A 100 W prototype was built to verify this solution. The main waveforms at light load mode under steady state have good agreement with the theoretical analysis. Smooth transitions between light load mode and heavy load mode are obtained from the experiment. This improved single-stage transmitter achieves high power efficiency at a full range of load.

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