Single-Phase Dual-Mode Four-Switch Buck-Boost Transformerless PV Inverter with Inherent Leakage Current Elimination

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Abstract—**This paper proposes a single-phase dual-mode four-switch Buck-Boost transformerless PV inverter with inherent ground leakage current elimination. Via directly connecting the grid neutral point to the PV positive terminal, the common mode (CM) voltage is clamped to be constant by the DC link capacitor. Thus, the CM leakage currents are eliminated completely. Moreover, the DC link voltage for the proposed inverter is required to be only higher than the amplitude of the grid voltage, instead of higher than twice of the amplitude of the grid voltage for the half-bridge-based inverter. There are two operation modes for the proposed inverter: Buck mode for the negative half line cycle and Buck-Boost mode for the positive half line cycle. Single stage energy process is achieved in both two operation modes for achieving high efficiency. The smooth mode transition is realized by the proposed dual-mode dual-carrier unipolar sinusoidal pulse-width-modulation (SPWM). Besides, since this PV inverter only uses four switches and one main inductor, low cost is achieved by this inverter. In summary, the proposed PV inverter achieves low leakage current, high efficiency, high density, low cost, and non-unity power factor capability. Finally, the simulation results verify the concepts and demonstrate the performance of the topology, the modulation and the control strategy.**

Keywords—Single-phase transformerless PV inverter; leakage current elimination; four-switch; dual-mode dual-carrier SPWM

I. INTRODUCTION

The single-phase photovoltaic (PV) inverters for residential applications are drawing more and more interests recently [1]-[10]. There are two types of single-phase PV inverters: the isolated PV inverters and the transformerless PV inverters [1]-[10]. Compared with the isolated PV inverters, the transformerless PV inverters have lower cost, higher efficiency, higher power density, and lower complexity [1]-[10]. However, due to removing the transformers, the transformerless PV inverters may introduce the issue of the common mode (CM) ground leakage currents, which flow through the parasitic capacitors between the PV terminals and the ground [11~12]. To satisfy the safety requirements and standards, various transformerless topologies are reported for eliminating or reducing the leakage currents.

The H-bridge inverter with bipolar sinusoidal pulse width modulation (SPWM) is the simplest single-phase transformerless PV inverter [7]-[10]. However, the poor utilization of the inductors caused by the bipolar SPWM significantly reduces the efficiency and power density. H5 inverters [13], H6 inverters [14]-[15], and HERIC inverter [16] are developed by adding additional switches or diodes to the H-bridge inverter. Improved utilization of the inductor is realized for these inverters via using unipolar SPWM. However, the additional active switches increase the cost and the complexity. Moreover, for all the above mentioned H-bridge-based inverters [7]-[16], the leakage currents cannot be eliminated completely, due to the parasitic capacitances of the switches [17]-[18].

Several half-bridge-type PV inverters, which directly connect the grid neutral point or the line point to the middle points of the DC links, are discussed in [19]-[20]. These inverters eliminate the leakage currents, since the CM voltages are clamped to be constant by the DC link capacitors. However, the DC link voltages of the half-bridge inverters should be higher than twice of the grid voltage. Thus, the utilizations of the DC link voltages are reduced.

Several common grounded PV inverters also eliminate the leakage currents inherently, since they connect the grid neutral point or the line point to the negative terminals of the DC links [21]-[24]. However, these common grounded inverters also introduce some weaknesses. The virtual-DC-bus-based common grounded PV inverter requires a large virtual DC bus capacitor and an additional switch [21]-[22]. The common grounded PV inverter with active power decoupling capability [23], has low efficiency since the topology uses two stages to transfer the energy. And it also has low power density due to the additional large inductor. The "Siwakoti-H" inverter discussed in [24] introduces high conduction loss due to the utilization of the reverse-blocking IGBTs. By connecting the grid neutral or the line point to the positive terminal of the DC link, the SEPIC-converter-based inverter also eliminates the leakage

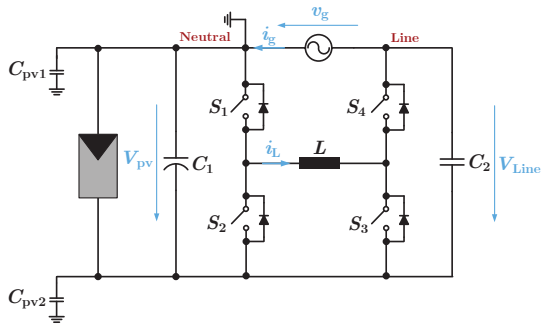

Fig. 1. Topology of the proposed single-phase transformerless PV inverter

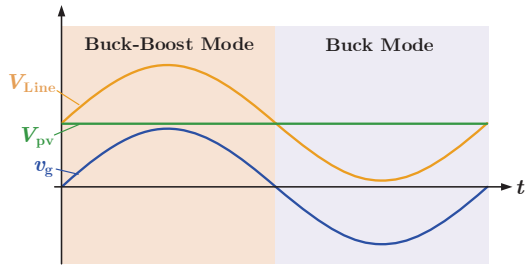

Fig. 2. Dual-mode operation waveforms of the grid line point voltage v_{Line}, the PV voltage V_{pv}, and the grid voltage v_g

current due to the constant CM voltage [25]-[26]. However, this inverter has the intrinsic disadvantages of the SEPIC converter, such as the low efficiency and the additional passive components.

In this paper, a single-phase dual-mode four-switch Buck-Boost transformerless PV inverter is proposed as shown in Fig. 1. In the proposed inverter, the grid neutral point is directly connected to the PV positive terminal. Thus, the proposed PV inverter eliminates the leakage currents inherently, since the CM voltage is clamped to be constant by the DC link capacitors. In addition, the DC link voltage for the proposed inverter is required to be only higher than the amplitude of the grid voltage, instead of higher than twice of the amplitude of the grid voltage for the half-bridge-based inverter. There is also no requirement for extra DC link capacitors compared with the virtual-DC-bus-based common grounded PV inverter. Besides, the proposed inverter achieves low cost and high power density, since the proposed inverter contains only four switches and one inductor. The proposed inverter has two operation modes: Buck mode for the negative half line cycle and Buck-Boost mode for the positive half line cycle. The proposed inverter realizes high efficiency, since the single-stage energy process is achieved in both two operation modes. The proposed inverter also provides the non-unity power factor operation capability. Moreover, with the proposed dual-mode dual-carrier unipolar SPWM, the smooth mode transition is realized. Therefore, the proposed PV inverter not only eliminates the leakage currents, but also achieves high efficiency, high density, low cost, and non-unity power factor operation simultaneously.

II. Description of The Proposed Topology

The topology of the proposed four-switch Buck-Boost PV inverter is shown in Fig. 1. An inductor L is placed between the middle nodes of the two half-bridges. The grid neutral point is directly connected to the positive terminal of the DC link. Therefore, both the voltages over the PV parasitic capacitors are always DC voltages which may only contain negligible double line frequency ripples. The leakage currents from the PV terminals to the ground are eliminated inherently.

The grid line point voltage v_{Line} is the voltage from the grid line point to the PV negative terminal. To achieve the grid connection, the grid line point voltage v_{Line} should be the PV voltage V_{pv} plus the grid voltage v_g as expressed in (1).

$$v_{Line} = v_g + V_{pv} = V_{gm}\sin(\omega_g t) + V_{pv}, \tag{1}$$

where V_{gm} is the amplitude of v_g, and ω_g is the angular frequency of v_g. The waveforms of v_{Line}, V_{pv} and v_g are shown in Fig. 2.

This inverter can work under either hard-switching or soft-switching conditions. When this inverter works under hard-switching condition, S_1-S_4 cannot use the super-junction (SJ) Si MOESFETs due to the severe reverse recovery issues. Thus, S_1-S_4 can be the IGBTs with anti-parallel fast-recovery diodes. S_1-S_4 also can use the wide-band-gap (WBG) devices, such as the GaN and SiC MOSFETs, which have much less switching loss compared with the IGBTs and SJ Si MOSFETs [27]-[31].

The proposed inverter also can work with quasi-square-wave mode to achieve soft-switching. Under soft-switching condition, S_1-S_4 can use not only IGBTs and WBG devices, but also SJ Si MOSFETs.

Since all the above-mentioned devices have the capability of bidirectional current flow, this inverter can achieve non-unity power factor operation, under both the hard-switching conditions and the soft-switching conditions.

III. Operation Modes and Steady State Analysis

As shown in Fig. 2, there are two operating modes: Buck-Boost mode; and Buck mode. In this section, the detailed operation modes and the steady state analysis are included.

A. Buck-Boost mode

During the positive half line cycle (v_g>0), v_{Line} should be higher than V_{pv} as shown in Fig. 2. Hence, the inverter works in Buck-Boost mode as shown in Fig. 3 (a). In Buck-Boost mode, S_3 and S_4 operate with high switching frequency, while S_1 is always on and S_2 is always off. In the steady state of this mode, the steady state duty cycle $d_{BB} \in [0,1]$ of S_3 for Buck-Boost mode is formulated as

$$d_{BB} = \frac{v_g}{v_g \mid V_{pv}}, \qquad v_g > 0. \tag{2}$$

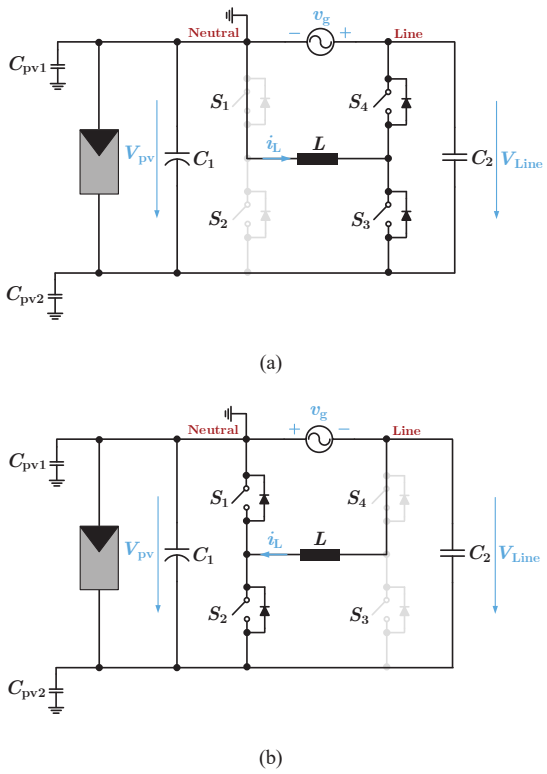

Fig. 3. Equivalent circuits: (a) Buck-Boost mode for the postive half line cycle; (b) Buck mode for the negative half line cycle.

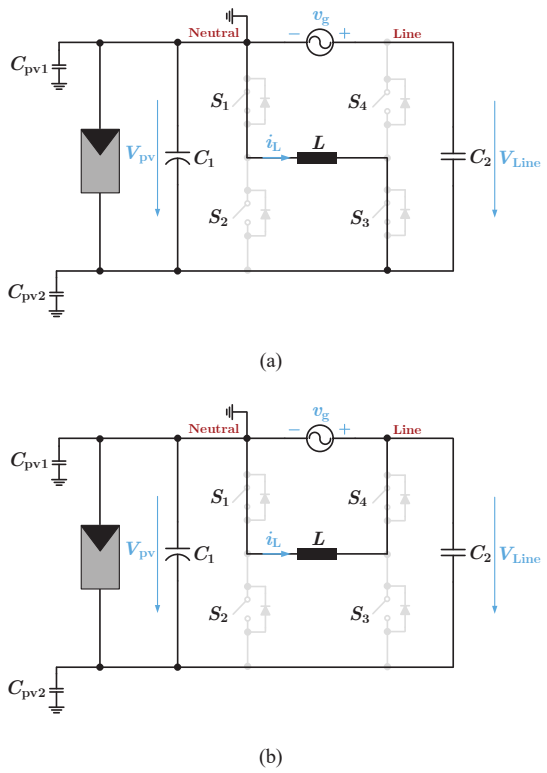

Fig. 4. Detailed equivalent circuits: (a) charging the inductor in Buck-Boost mode; (b) discharging the inductor in Buck-Boost mode; (c) charging the inductor in Buck mode; (d) discharging the inductor in Buck Mode.

Fig. 4 (a)-(b) show the detailed equivalent circuits in the Buck-Boost mode. To simplify the analysis in this section, only active power is delivered. When S_1 and S_3 are on, and S_2 and S_4 are off, the circuit charges the inductor, as shown in Fig. 4 (a). When S_1 and S_4 are on, and S_2 and S_3 are off, the circuit discharges the inductor, as shown in Fig. 4 (b).

B. Buck mode

During the negative half line cycle ($v_g \leq 0$), v_{Line} should be lower than V_{pv} as shown in Fig. 2. Hence, the inverter works in Buck mode as shown in Fig. 3 (b). In Buck mode, S_1 and S_2 operate with high switching frequency, while S_4 is always on and S_3 is always off. In the steady state of this mode, the duty cycle $d_{BK} \in [0,1]$ of S_2 for Buck mode is formulated as

$$d_{BK} = -\frac{v_g}{V_{pv}}, \qquad v_g \leq 0. \tag{3}$$

Fig. 4 (c)-(d) show the detailed equivalent circuits in the Buck-Boost mode. To simplify the analysis in this section, only active power is delivered. When S_2 and S_4 are on, and S_1 and S_3 are off, the circuit charges the inductor, as shown in Fig. 4 (c). When S_1 and S_4 are on, and S_2 and S_3 are off, the circuit discharges the inductor, as shown in Fig. 4 (d).

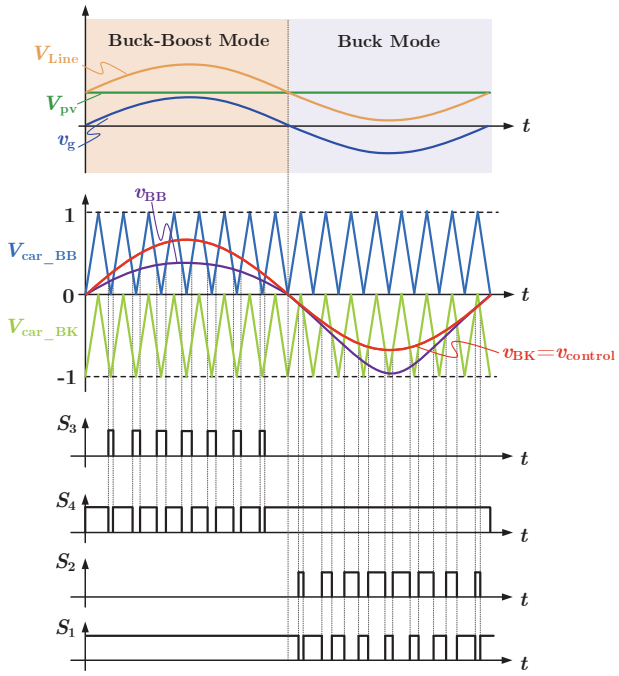

Fig. 5. Waveforms of the proposed dual-mode dual-carrier unipolar SPWM

IV. Dual-Mode Dual-Carrier Unipolar SPWM

To achieve the dual-mode operation and smooth transition between the two modes, a dual-mode dual-carrier unipolar SPWM is proposed in this paper. As shown in Fig. 5, the Buck-Boost mode carrier V_{car_BB} is from 0 to 1; the Buck mode carrier V_{car_BK} is from -1 to 0. In addition to the carriers, there are two modulation control signals: the Buck mode modulation control signal $v_{BK} \in [-1,1]$ and the Buck-Boost mode modulation control signal $v_{BB} \in [-1,1]$. The Buck mode carrier V_{car_BK} and the modulation control signal v_{BK} are for S_1 and S_2. The Buck-Boost mode carrier V_{car_BB} and the modulation control signal v_{BB} determine S_3 and S_4. The implementation of the modulation is illustrated in Fig. 6. The two modulation control signals are calculated as

$$v_{BK} = v_{control}, \tag{4}$$

$$v_{BB} = \frac{v_{control}}{v_{control}+1}. \tag{5}$$

where the control signal $v_{control}$ is the output of the current controller.

With the proposed modulation, the duty-cycles d_{BB} and d_{BK} can be expressed as

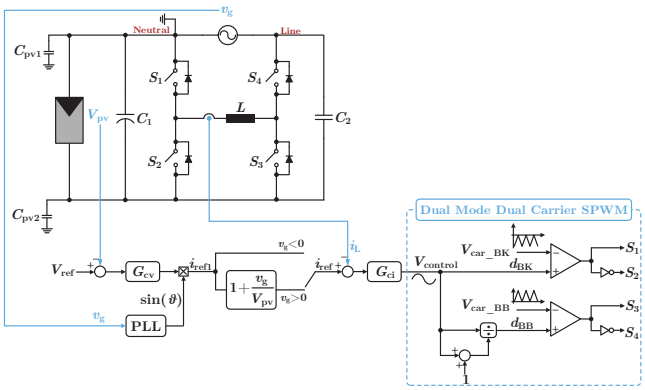

Fig. 6. Implementation of the proposed control strategy and dual-mode dual-carrier unipolar SPWM

$$d_{BB} = \begin{cases} 0 & v_g \le 0 \\ v_{BB} & v_g > 0 \end{cases} \tag{6}$$

$$d_{BK} = \begin{cases} -v_{BK} & v_g \le 0 \\ 0 & v_g > 0 \end{cases}. \tag{7}$$

V. Control Strategy

In Buck-Boost mode, it is hard to directly control the grid current due to the right half plane zero issue of the Buck-Boost converter. This paper proposes to control the grid current i_g by regulating the middle inductor current i_L. This current control method can eliminate the right half plane zero of the Buck-Boost system plant. The structure of the proposed system control strategy is shown in Fig. 6. The production of the voltage controller's output and the phase-lock-loop's output is the grid current reference i_{g_ref} as

$$i_{g\_ref} = I_m \sin(\omega_g t + \vartheta), \tag{8}$$

where I_m is the amplitude of i_{g_ref}, and ϑ is phase angle of i_{g_ref}. As described in the following equation, in the Buck mode for the negative half line cycle ($v_g \le 0$), the inductor current reference i_{ref} is the grid current reference i_{g_ref}; in the Buck-Boost mode for the positive half line cycle ($v_g > 0$), i_{ref} is calculated with i_{g_ref}, v_g, and V_{pv}.

$$i_{ref} = \begin{cases} I_m \sin(\omega_g t + \vartheta) & v_g \le 0, \\ I_m \sin(\omega_g t + \vartheta)(1 + \frac{v_g}{V_{pv}}) & v_g > 0. \end{cases} \tag{9}$$

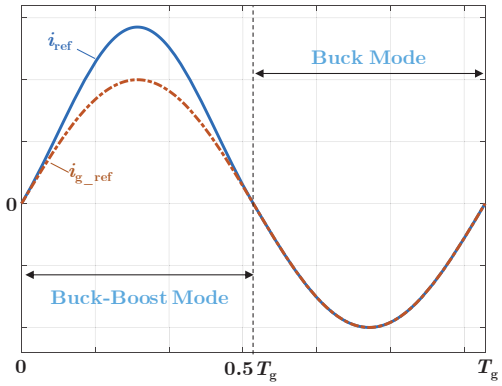

Fig. 7. Theoritical waveforms of the grid current reference and the middle inductor current reference.

The generation of the middle inductor current reference is implemented as shown in Fig. 6. Besides, the theoretical waveforms of the grid current reference and the middle inductor current reference are shown in Fig. 7.

VI. Simulation Results

To verify the proposed topology, operation principles, dual-mode dual-carrier modulation and control strategy, the simulations are conducted in PSIM 11.0.

The simulation parameters are listed in Table I. The simulation waveforms under different power factor conditions are shown in Fig. 8~10. In Fig. 8, the power factor is 1. In Fig. 9, the power factor is 0.9 (lagging). In Fig. 10, the power factor is 0.9 (leading).

Based on the simulation results in Fig. 8~10, the proposed inverter topology achieves grid connection under different power factors. In the proposed topology, since the grid neutral point is directly connected to the PV positive terminal, the voltage V_{neu} from the grid neutral point to the PV negative terminal is always the same as the PV voltage V_{pv} under different power factors. The leakage currents are eliminated due to the constant CM voltage. Besides, with the proposed dual-mode dual-carrier unipolar SPWM, the smooth mode transition is achieved under different power factors as shown in Fig. 8~10. Moreover, with the proposed control strategy, the grid current is controlled as pure sinusoidal under different power factor conditions.

TABLE I. Simulation Parameters

Parameters	Value	Unit
PV voltage V_{pv}	200	V
Grid voltage RMS v_g	120	V
Rated power P	500	W
Line Frequency f_g	60	Hz
Switching frequency f_s	100	kHz
Inductor L	400	μH
DC capacitor C_1	300	μF

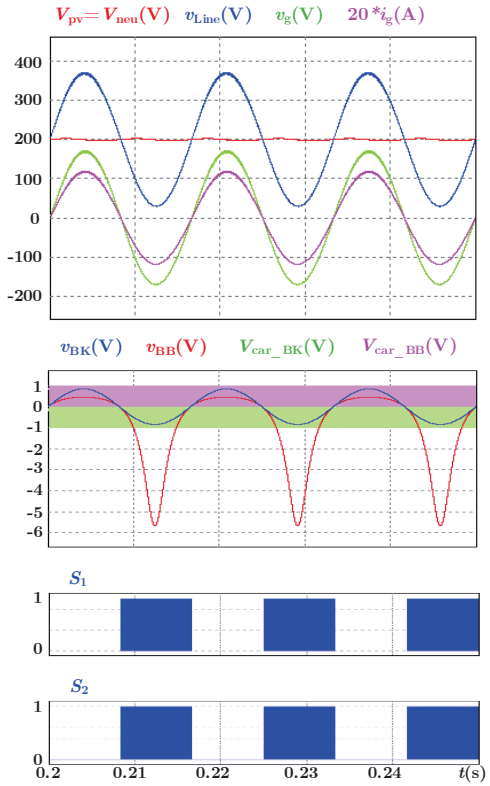

Fig. 8. Simulation results with PF=1.

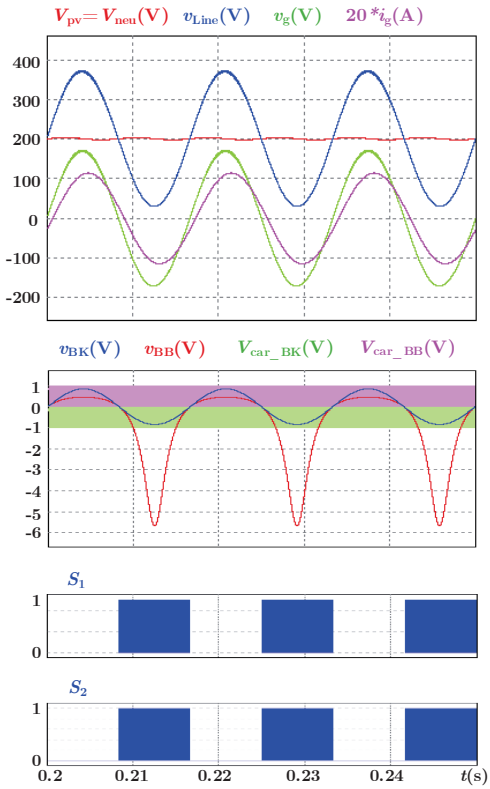

Fig. 9. Simulation results with PF=0.9 (lagging).

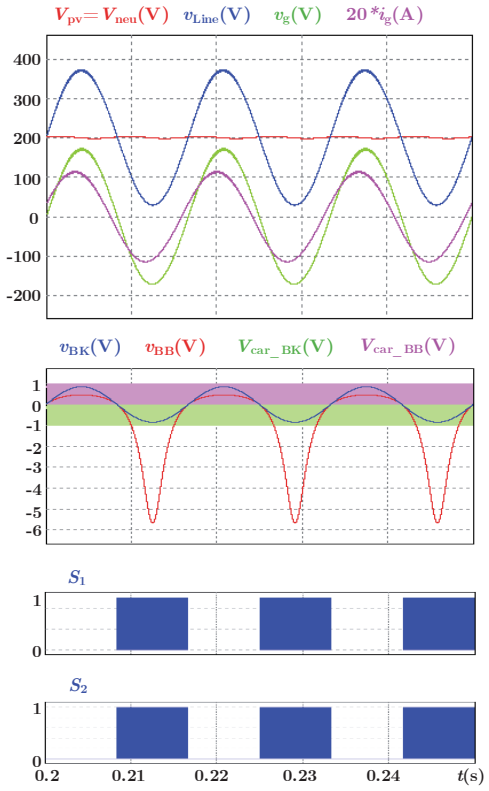

Fig. 10. Simulation results with PF=0.9 (leading).

VII. Conclusions

In this paper, a single-phase dual-mode four-switch Buck-Boost transformerless PV inverter is proposed, analyzed and verified. By directly connecting the grid neutral point to the PV negative terminal, the leakage currents are eliminated inherently due to the constant CM voltage. The DC link voltage for the proposed inverter is required to be only higher than the amplitude of the grid voltage, instead of higher than twice of the amplitude of the grid voltage for the half-bridge-based inverter. There are two operation modes: Buck-Boost mode for the positive half line cycle; and Buck mode for the negative half line cycle. The efficiency is high, since in both Buck and Buck-Boost modes, the power is processed by single stage. The smooth mode transition is realized by the proposed dual-mode dual-carrier unipolar SPWM. This topology also provides the capability of non-unity power factor operation. Besides, with the proposed control strategy, the grid current is controlled as pure sinusoidal under different power factor conditions. Moreover, since the proposed inverter requires only four switches and one main inductor, the proposed inverter realizes low cost. Finally, this inverter can achieve high power density due to the high efficiency, the low leakage currents, and the minimum counts of the switches and the main passive components.

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