Active Gate Driver for SiC MOSFET based PV Inverter with Enhanced Operating Range

Sayan Acharya*+, Xu She+, Fengfeng Tao, Tony Frangieh, Maja Harfman Todorovic+, Rajib Datta+.
*FREEDM System Center, NCSU, Raleigh, NC-27606, USA
+GE Global Research, Niskayuna, NY-12309, USA

***Abstract* –For photo-voltaic (PV) inverter applications, the grid code mandates reactive power support to the grid, and the amount of reactive power injection may be limited by the voltage overshoot during the switching transients. For SiC-MOSFET based PV inverters this problem is more pronounced since the voltage and current gradient during switching transitions are much higher than a Si-based power devices. During a gloomy day when the inverter has to operate at PV panel's open circuit voltage, it becomes harder to push higher currents through the device but also keeping the device within its SOA and low the switching loss at all operating conditions. Slowing down the switching transient could be a remedy but this also increases the converter switching loss. This paper demonstrates an application of dynamic gate resistance modulation technique to keep the SiC-device inside its safe operating area (SOA) while maintaining a low switching loss with minimum voltage and current overshoots. The proposed implementation is verified with hardware test results at high junction temperatures (up to 150^{0}C).**

***Index Terms*— Gate Driver, Safe Operating Area (SOA), Silicon Carbide (SiC), Power Block, Wilde Band Gap (WBG).**

I. INTRODUCTION

Fast switching capability, low losses, higher thermal capacity make SiC based power devices potentially great for various application areas such as solar converter, drives etc. [1]. However, high dv/dt and di/dt during switching transients poses several challenges in a converter system design. The parasitic in the circuit layout becomes much more prominent. The hardware set up can be optimized to a certain degree which may not be enough to get the optimum performance out of SiC-devices. For instance, the GE LV5+ solar inverter uses 1.7 kV SiC MOSFET (Fig.1) in a two-level converter structure module [2]-[3]. The MPPT range is 875-1500V with full power operation. However, it may still need to provide reactive power at its open circuit voltage which is 1500V. In a cloudy morning the active power output is expected to be less. But typically, the converter is required to provide reactive power support to the AC grid for voltage regulation. However, the amount of the reactive power injection is limited by the device transient voltage overshoot during switching from ON stage to OFF or vise-versa. Since the DC voltage is already at 1.5 kV, only 200 V overshoot (around 13%) is permissible to keep the SiC-device within SOA. This poses a severe limitation on the amount of current that can be pushed through the SiC-MOSFET. To solve this problem the converter can be operated with high gate resistances, making the switching transients slower. This affects the overall system efficiency adversely. It is desired to minimize the switching loss but keeping the voltage overshoot across the SiC-MOSFET limited. This can be achieved to a great extent by modulating the gate resistance dynamically during every switching instant [4]. This paper delves into the dynamic gate resistance technique and proposes a simple implementation method of the active gate driving technique by changing the gate resistance dynamically during turn ON and OFF transition periods to push more reactive power.

Fig. 1 A 1.7 kV, 450 A Low Inductance GE- SiC MOSFET module from GE with smart gate drive and interface board on top

The paper has been organized in the following way: Section II proposes the ideal of the dynamic gate resistance changing. Section III focuses on Turn OFF transition and Section IV shows the turn ON transition. The operation at high temperature is demonstrated in Section V. Extension of reactive power injection is demonstrated in Section VI. Finally conclusion has been drawn in Section VII.

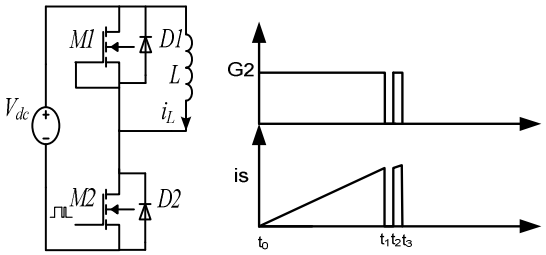
II. PROPOSED IDEA OF ACTIVE GATING

Double pulse test (DPT) method is used to evaluate the losses of a MOSFET as shown in Fig.2. The upper switch is always in off state, and a double pulse gate is applied to the bottom switch. With this specific circuit configuration, the switching loss of MOSFET M2 and body diode D1 can be evaluated. DPT starts at t_0. During [t_0, t_1], the inductor current keeps increasing to the value needed as shown in Fig. 3(a). At t_1, M2 is turned off and the current transitions to D1, as shown in Fig.

3(b). During this process, the turn-off loss of M2 is characterized. In [t_1, t_2]: The inductor current freewheels in the diode D1, as shown in Fig.3(c). This pulse is relatively narrow but kept to be enough to ensure that the switching transition is fully completed. At t_2, M2 is turned on and the current transits from D1 back to M2, as shown in Fig. 3(d). During this process, the turn-on loss of M2 and turn-off loss of D1 is characterized. Since SiC MOSFET switches are considerably faster than Si-IGBT, the impact of the parasitic parameters to the switching transient becomes critical. Fig. 4 shows the equivalent DPT setup with consideration of key parasitic parameters. It is to be noted that the total loop inductance during the switching transition is represented as L_{stray} for simplicity

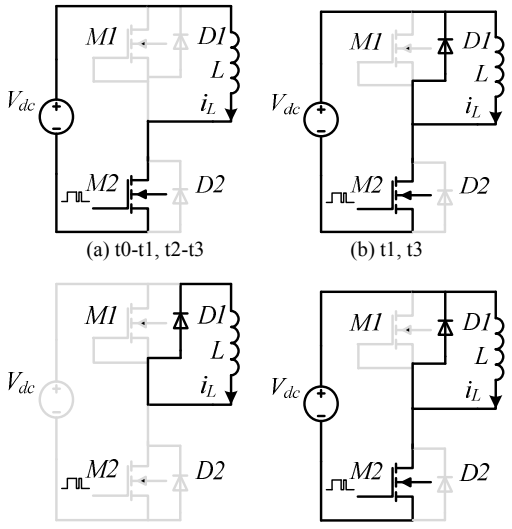
A. Turn-ON process of the SiC MOSFET

The turn-on process of SiC MOSFET can be illustrated in different stages as shown in Fig. 5. In [0, t_0]: Current flows through the body diode of the upper switch M1, and M2 blocks the full DC voltage. This stage ends when the ON gate signal is applied to the gate driver. In [t_0, t_1]: M2 is turned on at t_0 and the gate voltage V_{gs} increases due to the charging of input capacitor C_{gs}. Since the gate voltage is lower than the required threshold voltage of SiC MOSFET, there is no current in M2. This stage ends when the gate voltage V_{gs} increases to the threshold voltage V_{th} at t_1. In [t_1, t_2]: V_{gs} continues to increase and M2 begins to conduct current. As V_{gs} becomes larger, the channel resistance of M2 decreases and more current flows through M2. V_{ds_M2} decreases a little because of the voltage drop across stray inductor due to the current change. However, M2 still blocks the full voltage as body diode of M1 continues conducting current. This stage ends when the full current has been transferred from body diode of M1 to MOSFET M2 at t_2. As mentioned earlier, since the body diode has reverse recovery current, the lower switch current become more than inductor current as shown in Fig. 5. The maximum current overshoot depends on the peak reverse recovery current. This causes increase in turn ON loss. At higher temperatures, the situation becomes worse as the peak reverse recovery current of the body diode increases. The peak reverse recovery current is decided by the amount of charge stored in the diode and the di/dt of the circuit current, in this case the lower MOSFET



(a) DPT circuit diagram, (b) Gate and current in DPT

Fig. 2 Double pulse test for switching loss characterization



(a) t0-t1, t2-t3 (b) t1, t3

(c) t1-t2 (d) t2

Fig. 3 Equivalent circuits of double pulse test in different modes

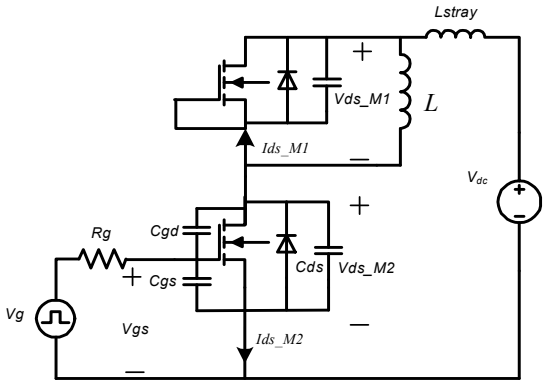


Fig. 4 DPT circuit with parasitic components

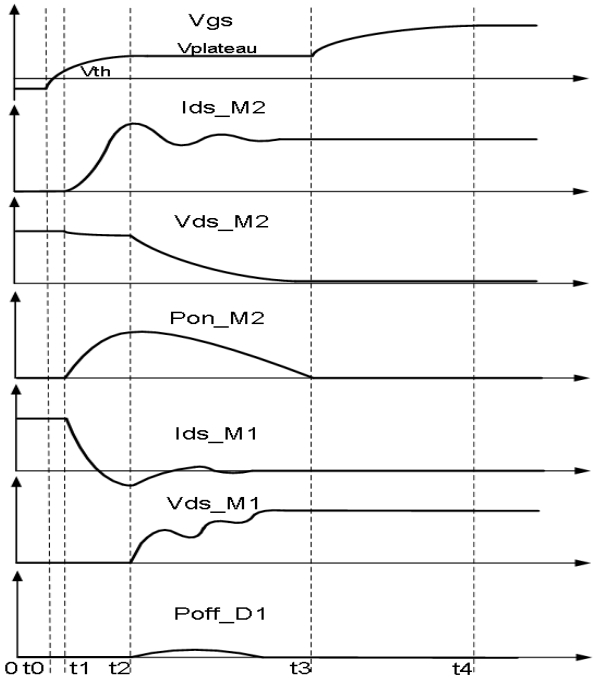


Fig. 5 Turn-ON process of SiC MOSFET

current. The lower is the turn ON gate resistance of the lower MOSFET, higher is the peak reverse recovery current and the opposite is true as well. Therefore, manipulating the turn ON resistance during turn on process can influence the MOSFET turn on loss as well as the current and voltage overshoot. In [t_2, t_3]: V_{gs} stays at plateau voltage $V_{plateau}$ since it still operates in the saturation region. V_{ds_M2} begins to decrease and V_{ds_M1} begins to increase. There is a current overshoot in I_{ds}, and this includes two parts: (a) the reverse recovery current of the body diode of M1, and (b) the current to discharge output capacitor C_{ds} of M2 during the transition. Due to the resonance between the stray inductor L_{stray} and the output capacitor C_{ds} of switch, a ringing can be observed in both V_{ds_M1} and I_{ds_M2}. This stage ends when V_{ds_M1} equals to V_{dc} and V_{ds_M2} equals to the voltage drop of M2 in the conduction state. In [t_3, t_4]: V_{gs} continues to increase from plateau voltage to the full turn-on voltage, minimizing the on-state resistance of the switch.

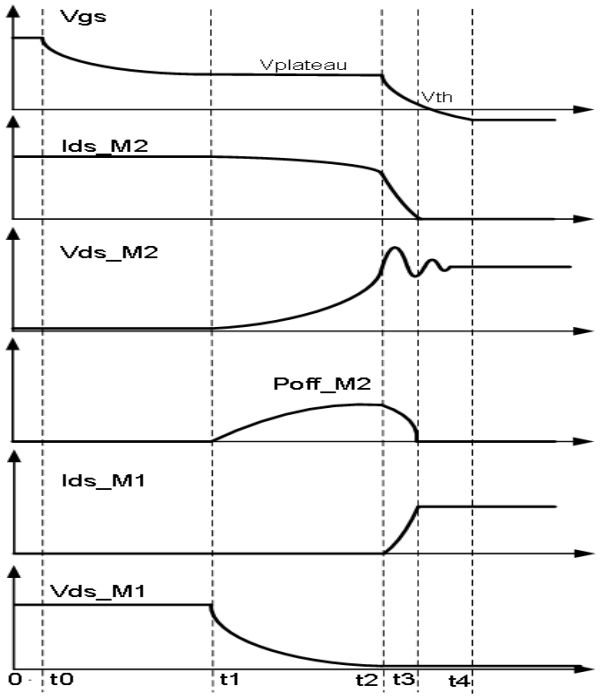


Fig. 6 Turn-OFF process of SiC MOSFET

B. Turn-OFF process of the SiC MOSFET

The turn-off process of SiC MOSFET can be divided into five stages as shown in Fig. 6. In [0, t_0]: Current flows through M2, and M1 blocks the full DC voltage. This stage ends when the gate turn-off signal is applied to M2 at t_0. In [t_0, t_1]: V_{gs} begins to decrease due to the discharging of C_{gs} and V_{ds_M2} increases a little due to the higher channel resistance. In this stage, M2 transits from linear region to the saturation region, and ends when V_{gs} decreases to the plateau voltage $V_{plateau}$. In [t_1, t_2]: V_{gs} stays at the plateau voltage in order to hold current of M2. Ideally I_{ds} should not change since the body diode of upper switch is reverse biased. However, it drops a little since part of the load current is used to discharge the output capacitor C_{ds} of M1. In this stage, V_{ds_M2} increases and V_{ds_M1} decreases until M2 blocks the full DC voltage at t_2. In [t_2, t_3]: Body diode of M1 begins to conduct current I_{dsM1} and I_{dsM2} decreases to 0. Due to the change of the current, an overshoot is observed at V_{ds_M2}. This stage ends until V_{gs} drops below the threshold voltage V_{th} and M2 is fully off. In [t_3, t_4]: V_{gs} continues decreasing until it reaches the gate driver turn-off voltage. Tables I and II summarize the parameters that impact performance in operation. In the table, "+" means that the parameter has a positive correlation to the performance, and "-" indicates that the parameter has a negative correlation to the performance.

Table I Parameters that affect the turn-on performance

	Turn-on delay	Current rise time	Voltage fall time	Diode reverse recovery
Turn on resistance	+	+	+	-
Turn off resistance				
Stray inductance				+
Turn on gate voltage	-	+	-	

Table II Parameters that affect the turn-off performance

	Turn-off delay	Voltage rise time	Current fall time	Turn off voltage overshoot
Turn on resistance	+			
Turn off resistance		+	+	-
Stray inductance				+
Turn on gate voltage	+			

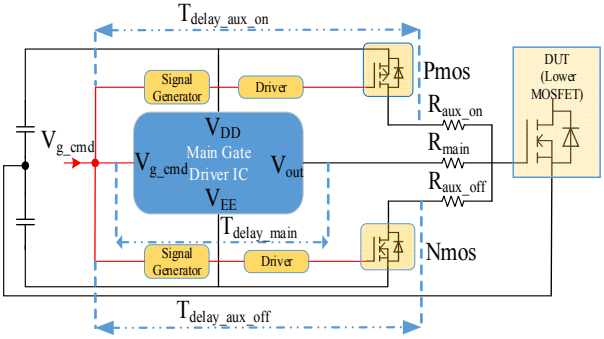


Fig. 7 Schematic of implemented circuit.

It is evident from the turn ON and turn OFF process that the transients can be controlled by controlling the gate charge. Gate charge can be controlled by dynamically changing the

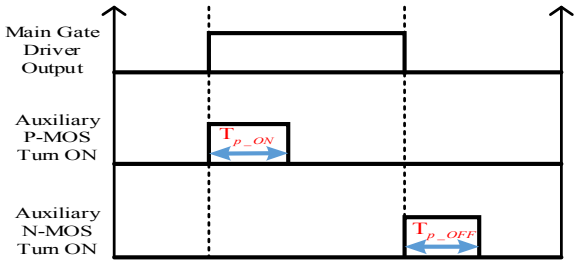


Fig. 8 Ideal timing diagram of the Active gating technique.

gate resistance during turn ON and OFF transients. The proposed active gate driver (AGD) technique modulates the gate resistance in two stages. The objective is to achieve a fast transient with minimum voltage and current overshoots but without sacrificing too much on the switching losses. For the proposed AGD technique, the gate resistance is kept low to start with and then it is turned high after certain period of time for both turn ON and turn OFF process. This time period when the effective gate resistance remains low is designated as T_p. As will be illustrated later, this provides a control over the voltage and current overshoot along with the turn ON and OFF losses of the device during the switching transients. Hence, T_p is the control variable for the proposed AGD technique. Fig. 7 shows the proposed gate active driver circuit functional diagram. As can be seen, that the main gate driver is connected to the device under test (Lower MOSFET) via R_{main}. During turn ON process when the main gate driver is turned on, the effective gate resistance can be made $R_{main}||R_{aux}$ by turning on the P-MOS. On the other hand, for the turn OFF case when the main gate driver is off, the effective gate resistance can be made $R_{main}||R_{aux}$ by turning on the N-MOS.

Since the turn ON and turn OFF transients for the SiC-MOSFET are ten-fold faster than the Si devices, the AGD implementation becomes a challenge. Normally, the switching transients for the SiC-devices span only few tens of nSecs. Hence, all the circuit delays have to be carefully estimated and

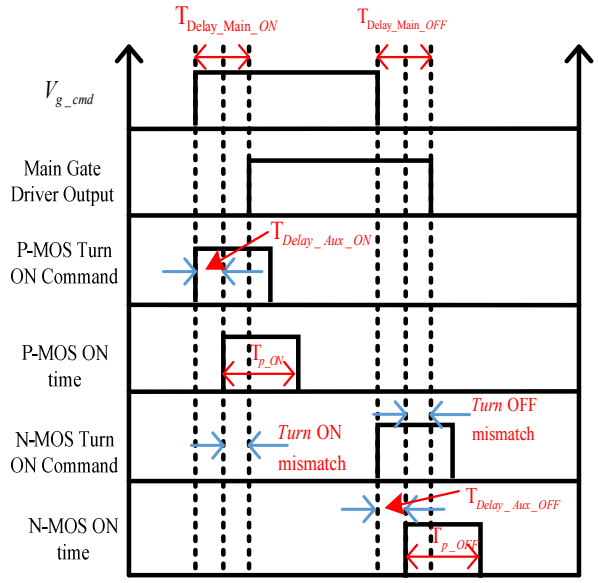


Fig. 9 Different circuit delays

compensated. As can be seen in Fig. 7, various circuit delays comes into the play. The auxiliary P-MOS and N-MOS have to be precisely turned on to have accurate control over the implemented T_{p_ON} and T_{p_OFF}. Ideally, the turn on of the P-MOS has to be synchronized with the positive edge of the main gate driver output for active turn ON and the turn on of the N-MOS has to be synchronized with the negative edge of the main gate driver output for active turn OFF. This is clearly indicated in the Fig. 8. However, due to the different circuit propagation delays, the time synchronization may not happen, if these delays are not compensated properly. As indicated in Fig. 7 there are three paths for propagation delays. They are:

1. Propagation Delay in the main gate driver chip: T_{delay_main}
2. Propagation delay from the V_{g_cmd} to the actual turn on of the P-MOS. This includes the delays from the signal generation circuit for P-MOS gating, the gate driver for P-MOS and the P-MOS turn on and off delays: $T_{delay\_Aux\_ON}$.
3. Propagation delay from the V_{g_cmd} to the actual turn on of the N-MOS. This includes the delays from the signal generation circuit for N-MOS gating, the gate driver for N-MOS and the N-MOS turn on and off delays: $T_{delay\_Aux\_OFF}$.

If the positive edge of the actual command signals V_{g_cmd} and P-MOS turn on command are matched, the aforementioned delays will make the implemented T_{p_ON} different than intended. Similarly, if the negative edge of the actual command signals V_{g_cmd} and N-MOS turn on command are matched, the delays will make the implemented T_{p_OFF} different than intended. This is illustrated in the Fig. 9. As can be seen, for the turn ON case due to the difference between $T_{Delay\_main\_ON}$ and $T_{Delay\_Aux\_ON}$, the positive edge of the main gate driver chip output is not synchronized with the turn on instance of the P-MOS. For the turn off case, the difference between $T_{Delay\_main\_OFF}$ and $T_{Delay\_Aux\_OFF}$ causes the

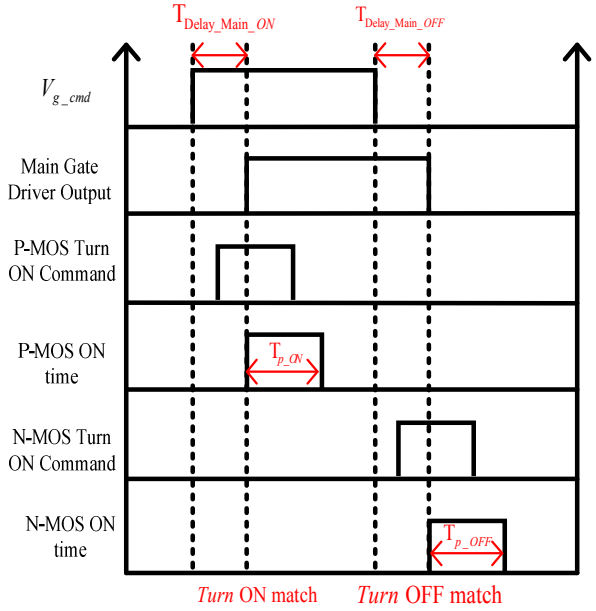


Fig. 10 Delay Compensated timing diagram

mismatch between the negative edge of the main gate driver chip output and the turn on of the N-MOS. Therefore the delay compensations have to be accommodated in the P-MOS and N-MOS turn on commands. After all these delay compensations, the timing diagram should look like the waveforms shown in Fig. 10. It is evident that now the positive edge of the main gate driver output and the turn on of P-MOS

are synchronized and so are the negative edge of the main gate driver output and the turn on of N-MOS.

C. *Proposed Turn OFF active gating process.*

In this case, the lower MOSFET is turned OFF and the upper device anti-parallel diode turns ON. The transition starts when the V_{g_cmd} is pulled down by turning off the main gate driver chip as shown in the Fig. 11. At the same time, the N-MOS is turned on. The propagation delays between the main gate command and the auxiliary N-MOS turn on command have to be adjusted to make sure that the main gate driver turn off and N-MOS turn on are synchronized. Hence, the effective gate resistance becomes $R_{main}||R_{aux}$. As shown in the Fig. 11, when the voltage across the device reaches about the DC bus voltage, the N-MOST is turned off, making the gate resistance value as R_{main}. In all cases, $R_{main} > R_{aux}$. The overlapping period is called T_{p_OFF}. It can be pointed out that during this period the rate of rise of voltage (dv/dt) is higher than the other time instants when the gate resistance is R_{main}. In this case the amount of the voltage and current overshoot can be controlled by controlling the T_{p_OFF} time. The challenging part is that normally the SiC-MOSFET turn ON and OFF transient lasts only for tens of nSec. Therefore, the precise implementation of the T_{p_OFF} is the key to achieve good results.

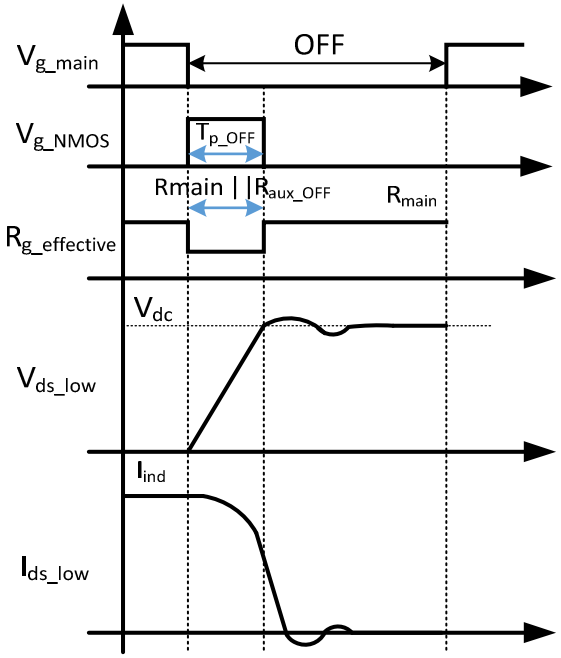


Fig. 11 Proposed active turn-off process

D. *Proposed Turn ON active gating process*

Turn ON is trickier to deal with because the upper MOSFET body diode turns off during this process. The reverse recovery current of the upper MOSFET body diode does influence the turn ON loss as well as the lower device current overshoot and the upper device voltage overshoot. Also, since the body diode reverse recovery current has a dependence on the operating junction temperature, this process is sensitive to the operating temperature. At higher temperatures, the reverse recovery current of the MOSFET body diode increases which increases the turn ON loss of the lower device. Fig. 12 depicts the proposed active gating technique during the turn ON period. The turn ON process starts when the main gate driver chip is turned on. It is demonstrated in Fig. 12 that the P-MOS is also turned on at this time to make sure the turn ON starts with an effective gate resistance of $R_{main}||R_{aux}$. When the lower MOSFET gate voltage crosses its threshold voltage, the lower MOSFET starts conducting current and the point at which the device current reaches close to the steady state current (about 90%) (which is also the time instant when the upper MOSFET body diode current goes close to zero) the auxiliary P-MOS in

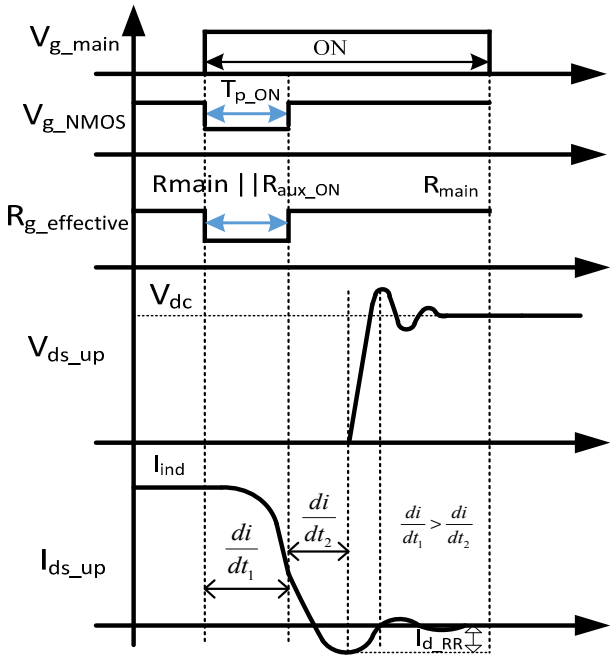


Fig. 12 Proposed active turn-ON process

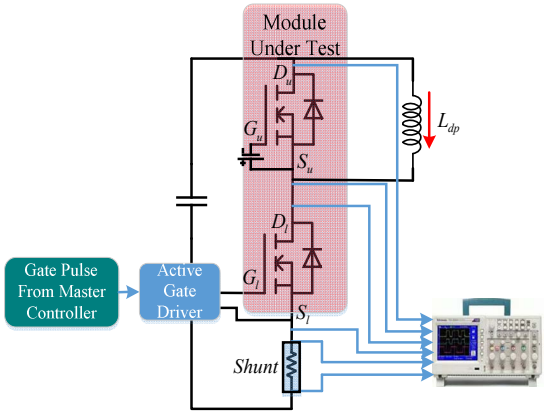


Fig. 13 Schematic of the double pulse setup

the gate driver circuit is turned off resulting in the effective gate resistance of R_{main}. The duration in which the auxiliary P-MOS is turned on is called as T_{p_ON}. It can be pointed out

Fig. 14 Implemented T_{p_OFF} time during turn OFF

that after T_{p_ON} time, the slope of the lower device current (di/dt) reduces as shown in Fig. 12. This causes reduction in the peak reverse recovery current I_{d_RR} which also helps to reduce the peak voltage overshoot of the upper MOSFET body diode voltage. It is proposed to control the T_{p_ON} time to control the voltage and current overshoots. Again, the implementation should be precise. For all the implementations proposed in this paper are done in the analog domain. But digital implementation can also be an option with much more

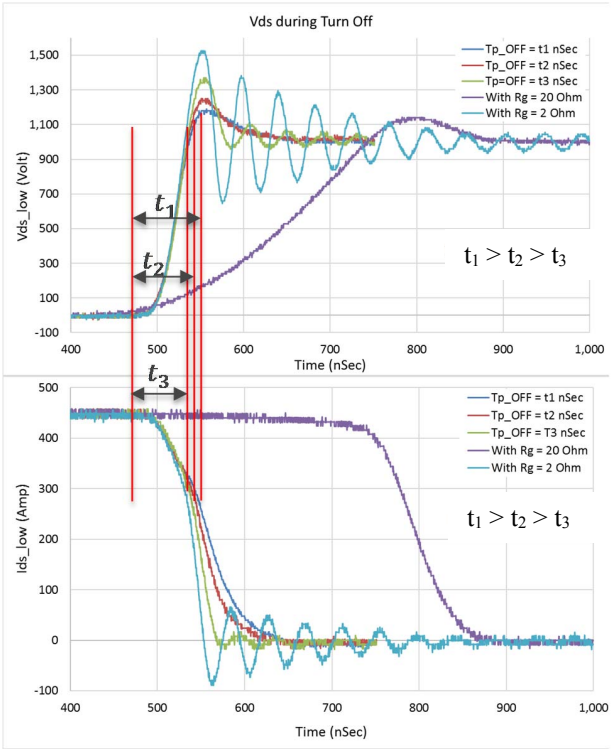


Fig. 15 Active Turn OFF.

flexibility. But this also needs very high clock frequency for the digital controller to get very good resolution of the implemented T_{p_ON} *and* T_{p_OFF} times.

III. Hardware Results: Active Gating during Turn OFF

The proposed AGD methods are implemented in a prototype hardware to prove the effectiveness of the proposed theory. All the implementations are done in a double pulse setup and the active gating is implemented in the lower MOSFET. The schematic diagram of the prototype is shown in the Fig. 13. For all the cases, shunt has been used to sense the lower device current. In all the test procedures, DC bus voltage is kept at 1000V and the R_{main}=20 Ohm and R_{aux}=2 Ohm. Even though the results are shown at 450A current level, the method is also tested with other current levels which revealed similar results.

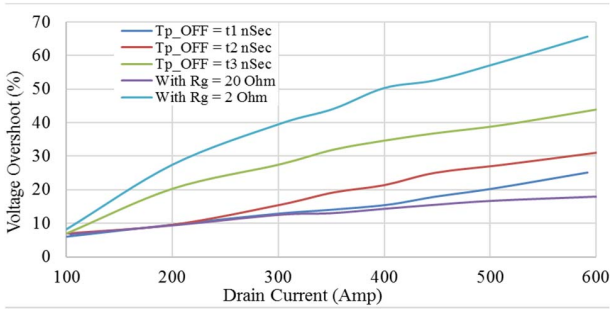


Fig. 16 Voltage overshoot with active gating as a function of MOSFET current.

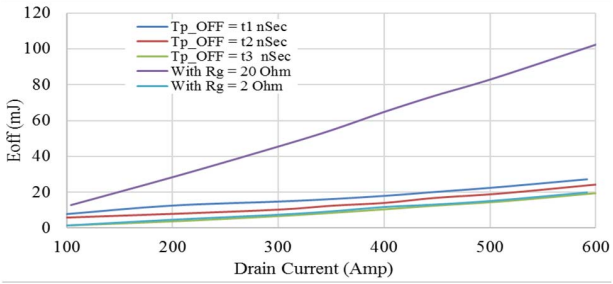


Fig. 17 E_{OFF} with active gating as a function of MOSFET current.

For the base case, the turn OFF waveforms are captured with fixed 2 Ohm and 20 Ohm gate resistance. Then the active gating method was tested at different values of T_{p_OFF} times. Fig. 14 shows the implemented T_{p_OFF} time. As can be seen during the T_{p_OFF} time when the effective gate resistance is low, the slope of the gate voltage is much faster than the slope after T_{p_OFF} time. The test results are presented in the Fig. 15. As can be pointed out that the voltage and current overshoot wise the best results are obtained when the gate resistance is fixed at 20 Ohm. But this is also the case where the turn OFF loss is the highest. Fixed 2 Ohm gate resistance produces the lowest device turn OFF with highest voltage overshoot. The lower device voltage overshoot goes to 1500V. With active gate driving techniques intermediate solutions are attained. Three separate values of T_{p_OFF} have been implemented. They are t_1, t_2*and* t_3 where $t_1 > t_2 > t_3$. The highest value of

T_{p_OFF} produces the results closer to the case with fixed 2 Ohm gate resistance but with much less voltage and current overshoots. On the other hand, the minimum value of T_{p_OFF} gives the lowest voltage overshoot among all the implemented T_{p_OFF} values but at the expense of higher E_{OFF}. To compare the active gating performance the voltage overshoot and the energy loss during turn OFF are plotted as a function of MOSFET current in Figs. 16 and 17 respectively. As can be seen that active gating provides intermediate solutions with slightly more E_{OFF} than with fixed 2 Ohm gate resistance but it also reduces the voltage overshoot quite significantly. In fact, it can be seen with T_{p_OFF}= t_2 nSec the voltage overshoot is significantly reduced without sacrificing much on E_{OFF}. This definitively provides evidence that with the proper selection of T_{p_OFF} the device can be operated at higher current levels but keeping the SiC-MOSFET inside its SOA.

IV. Hardware Results: Active Gating During Turn ON

For the turn ON case, the active gate driving performance has been evaluated by measuring the upper diode current and voltage. As explained earlier the upper body diode reverse

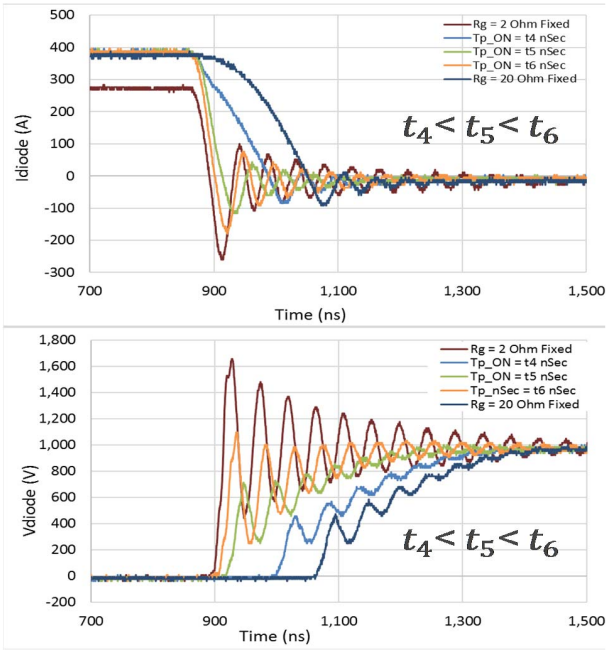


Fig. 18 Active turn ON at room temperature.

recovery current has the highest impact on the device losses in the bottom device turn ON loss. Again, the series of tests are done with similar system set up as the turn OFF case except that in this case the gate resistance has been varied dynamically during turn ON process. For the base case two tests were done one with fixed 2 Ohm gate resistance and other one with fixed 20 Ohm gate resistance. The results are presented in Fig. 18 are all done at room temperature. All the results are captured at 400 A current level except for the fixed 2 Ohm gate resistance since in that case the voltage overshoot in the upper device hits 1600V at around 280A. Further increasing current with 2 Ohm gate resistance would exceed the device voltage safe operating area limits. Three active gate driving cases each with separate T_{p_ON} values are presented. It can be clearly observed in Fig. 18 that the increase in T_{p_ON} value, increases the peak of the upper diode reverse recovery current. The lowest peak reverse recovery current is obtained when the gate resistance is kept 20 Ohm. But in that case the turn ON transition times are the slowest which makes the lower device switching loss higher. For the case with 2 Ohm gate resistance, the diode reverse recovery current and voltage overshoot is at highest level. The active turn ON provides results which are intermediate. As can be seen from Fig. 18 that three separate

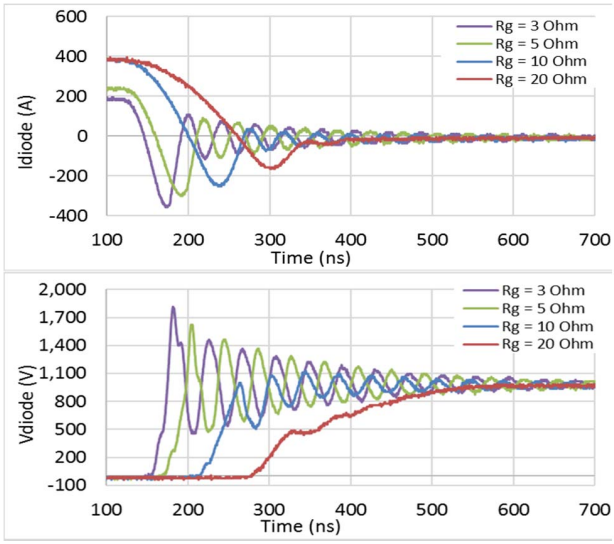


Fig. 19 Upper body diode Turn ON transients with fixed gate resistances at 150°C junction temperature

values of T_{p_ON} are implemented. They are t_4, $t_5 and\ t_6$ where $t_4 < t_5 < t_6$. As expected and illustrated in Fig. 18 the diode peak reverse recovery current increases with the increase in T_{p_ON}. With all these results, it is evident that controlling T_{p_ON} can provide a control over the upper diode peak reverse recovery current and voltage overshoot. Therefore, it can be concluded that higher is the T_{p_ON} value, lower is the effective gate resistance and in effect higher voltage and current overshoots are obtained.

V. Hardware Results: Performance at Elevated Temperatures

To measure the sensitivity of the proposed active gating method on the turn ON process, the turn ON tests are repeated at 150°C junction temperature. A heating pad with temperature controller is used to heat up the module junction temperature to 150°C. To demonstrate the effect of the elevated junction temperature a series of double pulse tests are done with various values of fixed gate resistances. Fig. 19 shows some series of results with varied fixed gate resistances. It is demonstrated that lower the gate resistance higher the diode peak reverse recovery current and the voltage overshoots across the upper

device body diode. With fixed gate resistances 3 and 5 Ohm the current could not be pushed beyond 200 A and 236 A respectively, since the diode voltage overshoots had already crossed SOA of the device. It can be pointed out that at higher junction temperatures the body diode performance becomes much worse. At the same operating junction temperature, the active gating with the combination of 2 and 20 Ohm is implemented with three separate values of T_{p_ON} i.e. t_7, $t_8 and\ t_9$ where $t_7 < t_8 < t_9$. The obtained results are presented in Fig. 20. It can be pointed out that with active

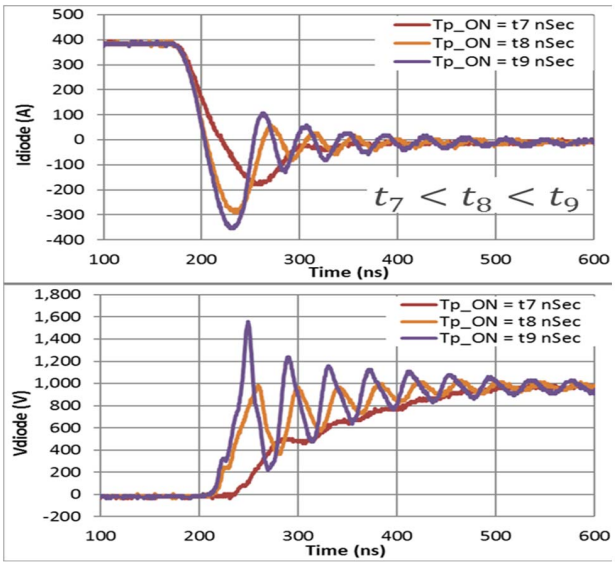


Fig. 20 Active gating performance during turn ON at 150ºC junction temperature

gating the module could conduct 400 A of peak current keeping the upper diode voltage well below the SOA limit of the SiC-MOSFET. Furthermore, Fig. 20 shows the similar trends as turn OFF case, the diode peak reverse recovery current increases with the increase in T_{p_ON}. With all the presented results, it can be concluded that by controlling the injected gate current into the input capacitance of the device by modulating the gate resistance dynamically during every switching instants the SiC-MOSFET can be operated within its SOA at all operating conditions. This becomes particularly helpful when voltage margin in an application is very narrow and it is desired to have low switching losses with minimum possible device voltage and current overshoots.

VI. Reactive Power Injection Enhancement

Fig. 21 shows the plot of reactive power injection with and with out AGD. As mentioned earlier, AGD helps to push more current through the MOSFET module at much lower votlage and current overshoots. As shown, with this technique the PV inverter is operated at DC bus voltage of 1500V. The advantages are evident and converter now is able to operate at double the current level than the fixed gate resistance case. Hense, the PV inverter can now inject double reactive power to the AC grid enabling grid voltage support.

VII. Conclusion

Due to fast transient characteristics, the SiC based converter layout plays a crucial role. For PV inverters when the voltage, current overshoot margin is considerably small, the system layout is not enough to push the device limits at the same time operate the device within SOA. Active Gating can provide suitable solution. In this paper, it is demonstrated that by actively controlling the effective gate resistance, the voltage

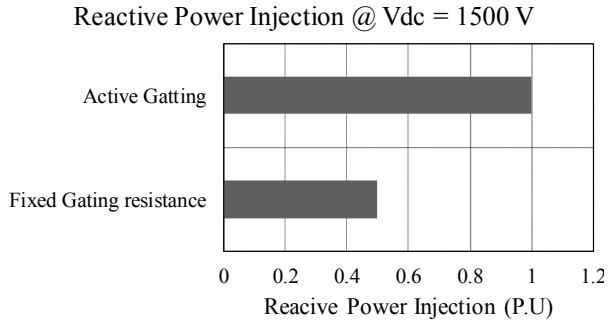


Fig.21 Reactive power injection improvement with AGD

and current overshoots during both turn ON and turn OFF transients can be controlled and SiC MOSFET can operate at higher current level and hence the PV inverter can provide much higher reactive power support to the AC grid. The proposed method produces good control over device voltage and current overshoots during the turn ON and OFF transitions. Moreover, the proposed method is equally effective at higher operating junction temperatures.

References

[1] X. She, A.Q. Huang, O. Lucia, and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," IEEE Trans. Ind. Electron., vol. 64, no. 10, pp.8193-8205, Oct. 2017.

[2] L. Stevanovic; B. Rowden; M. H.Todorovic; P. Losee; A. Bolotnikov; S. Kennerly; T. Schuetz; F. Carastro; R. Datta; F. Tao; R. Raju; P. Cioffi, "High performance SiC MOSFET module for industrial applications," in Proc. IEEE ISPSD, pp. 479 – 482.

[3] M. H. Todorovic; F. Carastro; T. Schuetz; R Roesner; L. Stevanovic; G. Mandrusiak; B. Rowden; F.F. Tao; P. Cioffi; J. Nasadoski; R. Datta,"SiC MW PV Inverter," in Proc. PCIM, 2016, pp.1 – 8.

[4] P. Nayak and K. Hatua, "Active gate driving technique for a 1200 V SiC MOSFET to minimize detrimental effects of parasitic inductance in the converter layout," in Proc. IEEE ECCE, 2016, pp. 1-8.

[5] S. Acharya, X. She, R. Datta, M. H. Todorovic and G. Mandrusiak, "Comparison of 1.7kV, 450A SiC-MOSFET and Si-IGBT based modular three phase power block," in Proc. ECCE, 2017, pp. 5119-5125.